

American Competitiveness Institute

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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government center and laboratories in the U.S.

EMPF Director

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In This Issue

- Page 1: Silicon-Germanium Flip Chip for RF Applications
- Page 3: Migration of Wirebonding to Flip-Chip
- Page 4: Ask the EMPF Helpline!
- Page 5: RF Modules Technology Roadmap
- Page 6: IPC 610 Electronic Assembly Acceptability
- Page 9: Tech Tips...S Parameter Testing for RF Applications
- Page 10: Manufacturer's Corner: Seica Functional Test Equipment
- Back Cvr: Upcoming Training Center Courses



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Silicon-Germanium Flip Chip for RF Applications

The traditional Transmit/Receive (T/R) module for an Active Electronically Steered Array (AESA) radar, or a transmit or receive module for any phased array antenna-based communications system, consists of an assembly of several chips per antenna element. There are typically thousands of elements needed for a single radar or communications antenna system. At the minimum, a Low Noise Amplifier, a Power Amplifier, a phase shifter, and a circulator are needed for the T/R module, usually with additional components such

The EMPF is engaged in a ManTech effort, in partnership with Boeing (an IAB member company), to improve on the current state-of-the-art in T/R and other RF electronic modules by integrating the communications functions into a single chip, saving significantly by reducing component count for the module. The technology is scheduled to be inserted into the MMA (Multi Mission Aircraft) within NAVAIR and the DDG 1000 within NAVSEA. Future applications in the Navy such as U-CAS unmanned vehicles and others are also under consideration.

Flip Chip processes

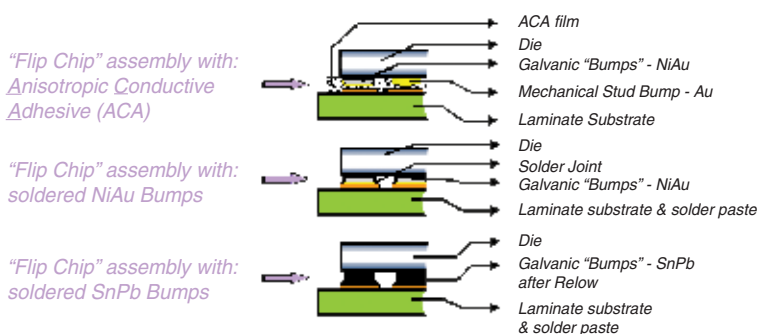


Figure 1-1 Several types of flip chip on board (FCOB) processes.

as capacitors, resistors, and inductors. Phased array antennas replace and vastly improve upon the legacy mechanically steered arrays, the moving dish or bar-type assembly commonly seen on older radar installations. Communications antennas benefit from the phased array in a similar fashion.

chip is SiGe or silicon-germanium. Chips made of this material can be fabricated using a semiconductor process known as Bi-CMOS which is much less expensive than the GaAs processing used to fabricate the MMIC (Monolithic Microwave Integrated Circuit) chips used in the RF assemblies today.

continued on page 2

Si-Ge Flip Chip for RF Applications (Continued from page 1)

The SiGe chip will be mounted on an organic multilayer substrate using the principles of flip chip. Further cost will be saved by utilizing an organic based printed wiring board substrate instead of the expensive and heavy ceramic currently used. This packaging technique, known as Flip Chip On Board (FCOB), employs “bumps” that are applied to the chip I/O pads either by electroplating, evaporation, attachment of individual solder spheres, or by a technique called “stud bumping.” These flip-chip processes are shown in Figure 1-1. FCOB will be used to limit the

parasitic effects of inductance and capacitance that would be incurred using the conventional wire bond interconnections most often used in modules for current phased array antenna systems. The EMPF will help select the process to be used for SiGe SoC.

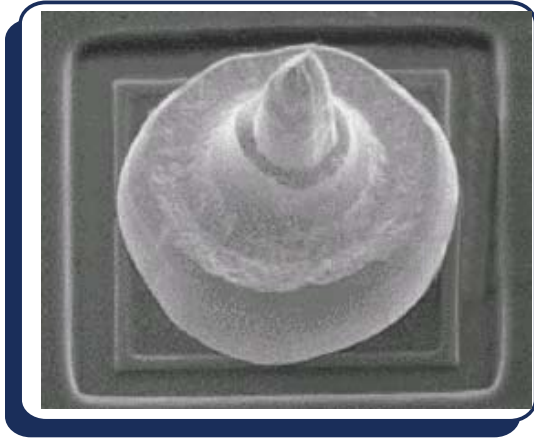


Figure 1-2 Typical gold “stud bump” for flip chip applications. The bump is formed by breaking off a gold wire after the gold ball bond is made to the chip pad. Photo courtesy of Valtronic USA.

For low volumes of bumps per month, such as are predicted for this application (relative to a commercial use), the stud bump is the least expensive way to apply bumps to a chip. In the stud bumping process, a ball bonder using gold wire, forms a ball bond on the pad of a chip and then is broken off. This leaves the ball bond attached to the chip pad as a bump that can be

used in the flip chip process to connect the I/O pads of the chip to the bond pads of the circuit.

Figure 1-2 shows a typical stud bump, as applied on the I/O pad of a chip using a standard ball bonding tool. The chip pad is roughly 4x4 mils (thousandths of an inch) and the ball is formed from 1 mil diameter gold wire.

The final assembly, using the FCOB method is shown in detail in Figure 1-3. The other types of bumps will be compared during this project by the EMPF.

Since SiGe is inherently more compatible with future communications and radar applications that will operate at higher frequencies, the SiGe SoC modules will show improved performance over the currently use GaAs MMIC-based RF modules.

To summarize, the primary technology objectives driving the SiGe SoC material/packaging solutions are:

- Better high frequency response
- Lighter weight
- Lower cost
- Smaller devices

The solutions being addressed by this ManTech effort at the EMPF, along with industry partners are to:

- Develop Transmit and Receive RF Modules that utilize System On Chip (SoC) Silicon-Germanium Bi-CMOS technology.
- Substitute lower cost SiGe for existing GaAs.
- Utilize the SoC higher integration level to limit component count/module cost.
- Utilize FCOB packaging technology to minimize cost while maximizing performance of phased array antennas.

The partnership between the EMPF and Boeing on this ManTech project represents a typical arrangement to leverage the strengths and resources of both organizations on this critical technology development.

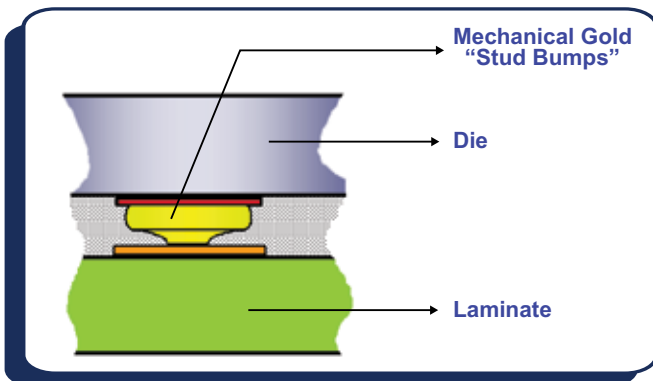


Figure 1-3 Typical FCOB assembly, as planned for the SiGe SOC application, after bonding of the die to the substrate. Illustration courtesy of Valtronic USA.



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Migration of Wirebond to Flip Chip RF

Since the invention of the transistor in 1947, researchers have been working to make the transistor smaller. Their success has resulted in ever-smaller devices, faster processing speeds, and enhanced performance. As operating frequencies increased, the traditional wirebond package became a limiting factor in performance for large devices. At the same time, chip designers were finding it harder and harder to create high yield, first pass silicon devices containing millions of transistors, and imbedded passives for System on Chip (SOC) radio transceivers. This opened the door for System in Package applications (SiP). SiP integrates surface mount components and silicon devices on a package substrate. SiP started out as a bridge technology to be used between device generations. However, many companies exist today by making SiP devices or “Modules”.

As packaging sub-contractors geared up for the increase of SiP applications, device designers kept pushing on SOC solutions as well as the SiP. To keep pace with System On Chip package size reductions, SiP implementations went from packaged devices integrated with passives, to chip on board with wirebonds and surface mount device (SMD) passives. Today many radio transceivers have gone to flip chip as wirebonding required up to 0.75mm of clean space on each side of the device to enable wirebonding. However, migration to flip chip has some issues. For most low to moderate (<100 I/O) pin count devices, a metal leadframe substrate is used. This results in a low cost per pin package. The metal lead frame is the package of choice for radio chips. Conversely, flip chip devices are packaged on a laminate board. The laminate could be FR4, polyimide, bismaleimide triazine (BT), Duroid, or Liquid Crystal Polymers (LCP). These materials all have mechanical and electrical properties that make them suitable for uses in various market segments.



Figure 2-1: Typical LGA package with the central pads shown

Photo courtesy of Stats ChipPAC Inc.

In a standard leadframe package, a large metal pad is used as the attachment point for the device. In the past, devices were

grounded through the backside of the silicon, but patent protection, latch-up issues, and the desire to have separate grounding schemes on one piece of silicon, led most companies to ground devices off pads on the top surface of the device.

Leadframe packages with short wires to ground have about 0.1nH of inductance to ground. A laminate package with one via to ground and a routed line in the laminate may have 0.5-0.8nH of inductance or more. This difference in inductance to ground is not trivial. The performance of a radio transceiver at moderate to high frequencies can be negatively affected by this difference. To mitigate this, the use of a land grid array (LGA) package is an excellent choice. Figure 2-1 shows a typical LGA package, the larger central pads, and I/O pads.

When a device is flipped onto this style of package, one of the central four pads can be taken advantage of as a ground pad. By patterning vias to one of the quad pads that lie under the flip chip ground pad connections, the inductance to ground can be lowered to match the inductance of the metal leadframe. If Electro Magnetic Interference (EMI) is an issue, a drop-in EMI Shield can be added, before injection molding, to provide shielding.

When RF devices go flip chip, a change in the values for components that comprise the radio device are necessary. Typical components for a front-end module are, but not limited to: band pass filters, low pass filters, and baluns. Combinations of capacitors and inductors create these circuits. The filters are designed using the packaged radio devices' characteristic impedances, and capacitances. An electromagnetic (EM) simulation tool is used to determine the values of inductors and capacitors required to create the passive networks. Trade off studies are made by making slight changes to inductance and capacitance values until the simulation reaches an optimum performance level. Passive surface mount components are provided with tolerance ranges of one to five percent or more. Using components with a wide tolerance such as 10% or 20% will lower the component cost. However, the resultant values for capacitance and inductance will vary and combinations of wide tolerance components may produce a filter that does not perform adequately in real world applications. An additional simulation that examines the variability and relates that to performance over multiple components with varying values is known as a Monte Carlo simulation. This simulation, made at the conclusion of the EM simulations, determines the effects of component variation. This ensures the selected component tolerance will create performance that is suitable for the applications of the product.

continued on page 7

Ask the EMPF Helpline!

A customer called into the EMPF Helpline after experiencing intermittent electrical performance in their circuit cards and were interested in design for manufacturing assistance.

The EMPF Helpline received a call from a control and telemetry electronics integrator involving PC board assembly (PCBA) failures in a radio transceiver. This PCBA module is used to control unmanned ground and air vehicles and other robotic systems. The customer had been experiencing intermittent electrical performance in their circuit cards and were interested in design-for-manufacturing assistance. The customer also requested that the EMPF review their PCB layout documentation, in order to resolve any fundamental design issues. The customer was able to obtain assistance with electronics manufacturing issues, RF design, layout, and packaging.

Some of the customer's RF design issues and questions included the following:

- Frequency drift in a crystal oscillator
- Via placement and connection to ground layers
- Trace (width and spacing) issues
- Antenna connector footprint
- Additional mounting holes for an EMI shield
- Determine necessity for impedance matching networks
- Interference between the customer's device and an adjacent wireless transmitter

The customer's circuitry was experiencing drifts in the fundamental frequency of an on-board crystal oscillator (which was a 4 pad surface mount package). The cause of the drift was traced to excessive heat being applied to the component during the assembly process. As it turned out, excessive heat relieved

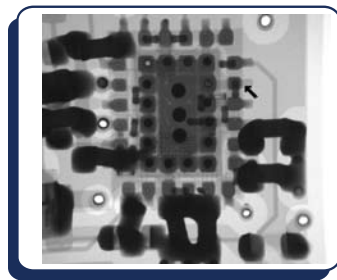


Figure 3-1, X-Ray Image of PCB Assembly showing insufficient solder between device and land

stress within the crystal, causing it to "speed" up. Excessive heat also caused unwanted material internal to the package to adhere to the crystal, thereby "slowing" it down. Ultimately, it was determined that there was no adequate way to solder this part by hand with a soldering iron. (Figure 3-1) To improve solder attachment, thermal relief connections were added to the component lands on all layers between ground pins and the surrounding ground plane. This improved some of the overheating issues that the customer was experiencing. The EMPF determined that the only acceptable method of crystal attachment was using solder paste and hot air reflow or a hot air pencil used for repair of SMT boards.

When designing RF PCBs there are many important factors to consider such as: minimization of signal loss, impedance matching, maintaining low layer counts, and dielectric control. Engineers at the EMPF performed RF simulation to verify the appropriate PCB dielectric thickness between signal layer and ground layer and to determine if the trace widths and spacings were optimized for this high frequency application. This was done to ensure that all of the connections between RF components were true 50 ohm transmission lines. If the traces are 50 ohm lines, it ensures optimal transfer of RF power between components on the circuit card. Overall, RF traces were shortened to minimize signal loss. It was also found that RF signals were being routed through a via hole. Since this would cause the RF signals to couple onto other layers, the EMPF recommended placing the antenna connector on the same side of the PCB as the RF components to eliminate the unwanted via hole connection.

To guarantee protection of the circuitry from moisture and corrosion, the EMPF assisted the customer with selection of conformal coating products. There are two types of conformal coating: translucent and opaque. Since certain conformal coatings containing urethane resin will interfere with RF signals, they were ruled out as a possible selection for this application. Encapsulating ("potting") the boards was also ruled out as an option since the customer would have to incur expensive tooling charges to fabricate a mold.

The EMPF's final recommendation to the customer was the use of an opaque conformal coating which also happened to be Mil-Spec approved. Based on testing and analysis of the radio module, which was performed at the EMPF, it was determined that manufacturing issues were the root cause of the customer's problems.

Also, due to the customer following key design guidelines (listed above) and manufacturing recommendations of the EMPF, the performance of their radio transceiver module was greatly enhanced. If you have any questions regarding the diagnosis of assembly related manufacturing problems or require design assistance and verification for RF circuit assemblies, please contact the EMPF Helpline at (610) 362-1320.



John Finn - *John* is an Engineer at ACI. Comments or questions pertaining to this article can be sent to jfinn@aciusa.org

RF Modules Technology Roadmap

The EMPF is actively engaged in the Joint Defense Manufacturers Technology Panel (JDMPT), through the RF Module Technical Working Group (TWG), to improve on RF Module technologies. This will include generation of a roadmap by the TWG to help guide selection of RF Module technologies gaps in need of development. As part of this support, EMPF representatives participated along with key government and industry contributors in a week-long RF Module Manufacturing symposium in the summer of 2005 at Redstone Arsenal and a RF Module roadmapping effort in Knoxville TN in spring of 2006.

Planning for both of these events was undertaken with the help of much government and industry support. The TWG was instrumental in both of these activities.

RF Modules are multiple component electronic assemblies that perform Radio Frequency (RF) functions. Examples include the cellular telephone, TV tuner, electronic automobile keyless entry device, as well as critical military RF Modules such as the Transmit/Receive module of a Phased Array radar (Figure 4-1) or the electronic fuze of a munition. Although many of these modules are the familiar “solid state” devices, vacuum devices in the form of high RF power Travelling Wave Tubes (TWTs) are also addressed by the TWG and various Mantech projects.

The RF Module TWG is chartered by the JDMTP to “identify

and integrate requirements, conduct joint program planning, and develop a joint strategy for Manufacturing Technology (Man-Tech) efforts conducted by the Army, Navy, Air Force, Missile Defense Agency (MDA) and Defense Logistics Agency” and to “facilitate knowledge sharing, coordination, and formulation of solutions to ManTech issues related to RF Modules at the engineer working level.”

The scope of the RF Module TWG includes RF Module applications in systems such as radar, electronic warfare, and communications. Platforms within the scope of the TWG range from airborne, space based, surface radar, ground based, under sea, and weapon systems.

EMPF contributed in the Electronic Packaging/Materials and Manufacturing sessions at both the 2005 and 2006 conferences. Areas of development that were suggested by EMPF include:

1. Near Hermetic Packaging

This is a topic of great interest that will undoubtedly occupy a prominent place in RF Module development efforts, and was the subject of a recently completed EMPF/Raytheon ManTech project that evaluated near hermetic hydrophobic coatings applied in wafer form to the chip components of the RF Module. Such coatings can render the individual chips making up the RF assembly inherently “near hermetic” and thus eliminate the need for costly, heavy, glass-to-metal sealed traditional hermetic enclosure used today. (Figure 4-2)

2. Wide Band Gap Components

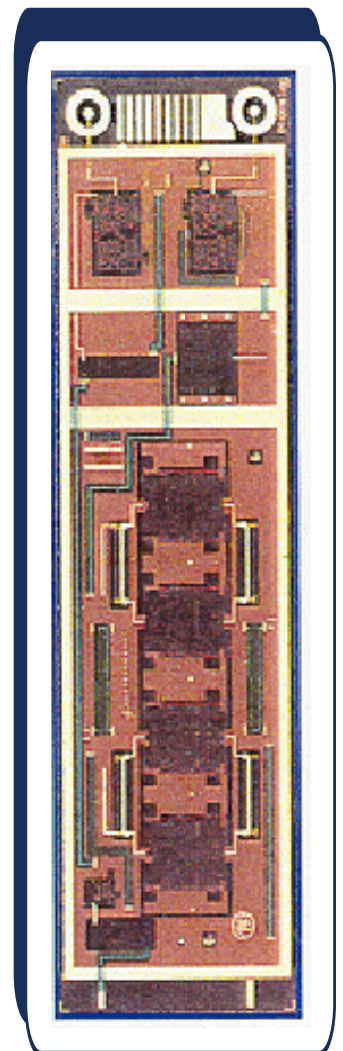


Figure 4-2 Affordable T/R Module based on Polyimide film. Module would be near-hermetic with suitable chip coating not yet available.



Figure 4-1 Transmit/Receive Module of a Phased Array Radar

continued on page 8

IPC 610 Electronic Assembly Acceptability

Specifications have been used in the manufacturing process since the introduction of the idea of “part interchangeability” and the demise of the practice of having the master craftsman complete the entire manufacturing process by himself. This was the “real beginning” of the Industrial Revolution as we know it today. During the period of the 1990’s and the growth of the “Communications and Information Age”, commercial specifications came into common use in electronics manufacturing for both civilian and military products, thus the publication of IPC-A-610, “Acceptability of Electronic Assemblies”.

The IPC-A-610D Revision was published in February 2005 and reflects changes primarily in the form of newly introduced components and processes. It was also re-organized to more readily reflect both the importance of the section and the flow of the process.

Section One: contains information specific to the document’s make-up: scope, purpose, design references, terms & definitions and general applications.

Section Two: contains a listing of applicable IPC documents.

Section Three: contains references and recommendations to manufacturing practices such the application of ESD control and handling practices in order to prevent contamination and physical damage during the manufacturing process.

Section Four: contains information for the proper application of hardware, torque and wiring stress.

Section Five: addresses soldering and the application of solder and is specific about anomalies or defects within the soldered connections, including the introduction of those particular to the use of lead free solder alloys and the acceptance of some types of abnormal conditions.

Section Six: illustrates terminal connections addressing the installation of various terminals, the attachment of wiring, the application of solder and the mechanics of dress and physical protection.

Section Seven: presents the requirements for through-hole technology and addresses component mounting, the use of heatsinks and the securing of components. The section also details the assembly and application of solder to both supported and unsupported holes.

Section Eight: details the requirements for placement and soldered connections of fifteen component

configurations including leadless components, (those having metallized contacts), and various styles of leaded components. There are two new component types and additional criteria for BGA attachment and acceptance guidelines for chip component “billboarding”.

Section Nine: addresses component damage as well as assembly processing damage to connectors, printed circuit boards and assemblies.

Section Ten: lists the requirements and describes the defect condition for gold plated edge contacts, laminate defects, marking, cleanliness and coatings.

Section Eleven: details the requirements for “discrete wiring” including those particular to “solderless wire wrap” and “jumper wires”, (additive wiring).

Section Twelve: addresses the requirements for wiring and the application of solder to “high voltage” terminations. (Certain high frequency applications might demand similar configurations).

Certification to one or more of the IPC specifications has filled the training/certification gap within the industry since the cancellation of the MIL-STD-2000 in 1995. The EMPF IPC-A-610D Revision Training/Certification program, released in late summer of 2005, contained a different approach as compared to the previous program: (1) the programs for certification and re-certification are now the same (2) the program for the Certified IPC Specialist (CIS) is now presented in modular form with modules 1 & 2 being prerequisite for all optional modules as well as modules 4 & 8 being a requirement for certification to either module 5, 6 or 7.

On-site classes for CIS can be scheduled in Philadelphia or custom classes, for both Certified IPC Trainers (CIT) and Certified IPC Specialists (CIS), can be scheduled for presentation at customer facilities. For additional information on registration and scheduling for IPC-A-610D Training/Certification, please contact the Training Center Registrar. Email: registrar@aciusa.org, phone: 610-362-1320 or sign up on the web site at www.aciusa.org.



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Migration of Wirebond to Flip Chip RF (continued from page 3)

When a leadframe and wirebonds are replaced by flip chip and laminate, the device characteristics change enough to require alterations to the filters and passive networks. Acquiring the flip chip device characteristics requires the use of a flip chip test bed and a network analyzer to measure the device impedance during operation.

One of the main advantages of migrating to flip chip from a wire bonded SiP is the reduced number of processing steps. If we use traditional wirebonding and combine surface mount passives, a product flow depicted in figure 2-2a emerges. In figure 2-2b, the process for SiP with flipchip is shown. A clear reduction in the number of process steps required to create the final product occurs when all attachments are made by soldering

With SiP modules, the most difficult part of the RF integration happens inside the package. A company wishing to use the module need only develop a 50-ohm (or other depending on the device) impedance transmission line to the antenna input. Conversely, the same company selling a single chip, may spend many days helping prospective customers debug their product boards to get optimum performance. From a time to market perspective, modules ease integration headaches, reduce board problems, and lower cost at market entry.

RF modules have made significant gains in the marketplace due to reduced development cost, shorter production cycles, im-

proved technical support, and broader application. There are challenges when evaluating the flip chip device characteristics. Moving a radio frequency device to flip chip must be carefully evaluated based on product application, competition, and market conditions. From a military perspective, standardization at the module level will reduce sustainment expense, improve performance, and lower overall cost.

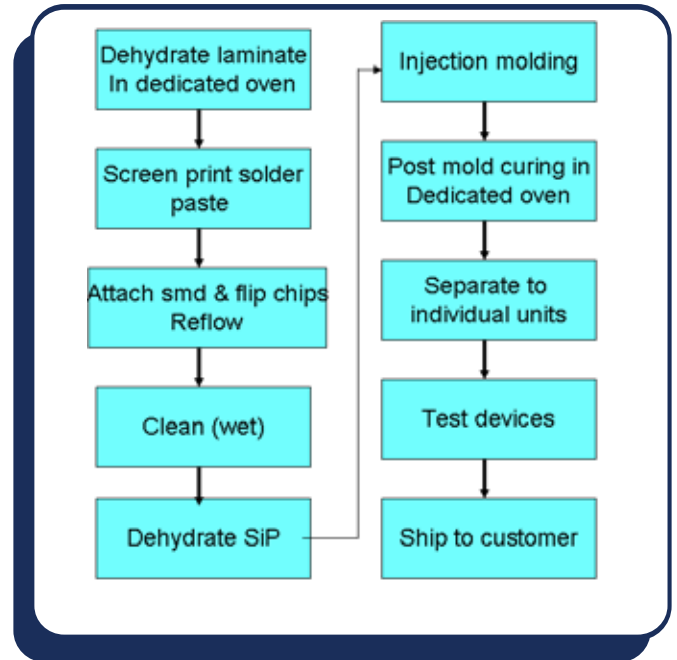


Figure 2-2b - Process flow for SiP with flip chip devices

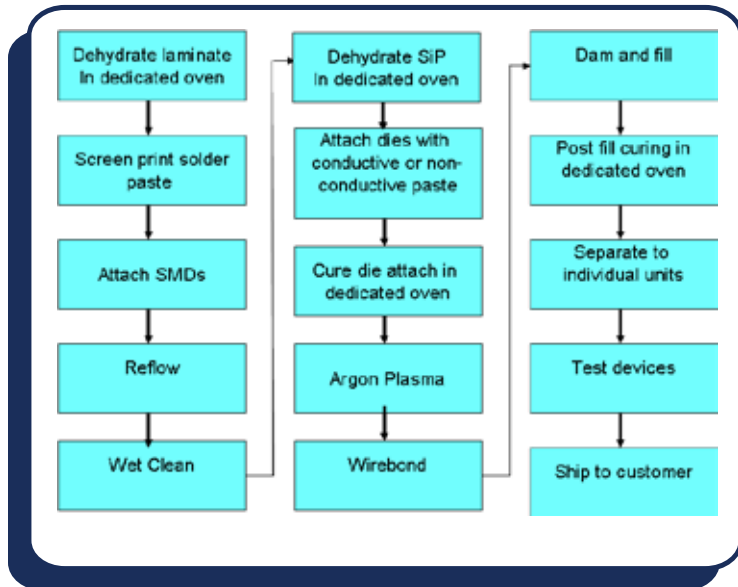


Figure 2-2a - Process flow for SiP with wire bond devices



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RF Modules Technology Roadmap (continued from page 5)

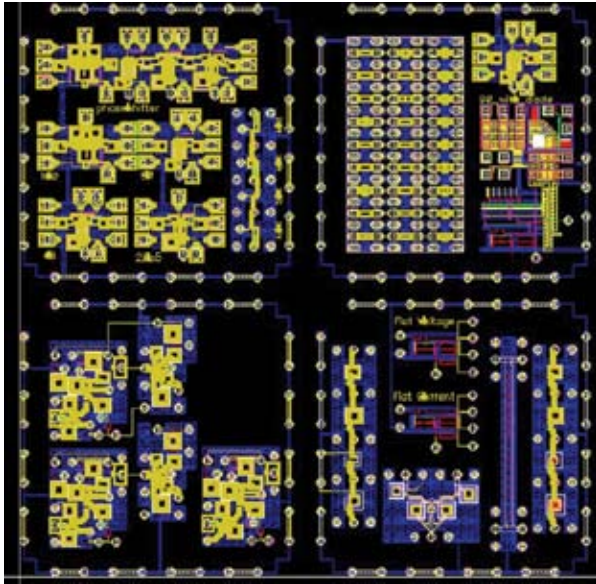


Figure 4-3 Ultimate RF Module integration (Affordability) represented by Silicon-Germanium RF System on a Chip (SOC)

These integrated circuit materials, including Silicon Carbide (SiC) and Gallium Nitride (GaN), will allow higher RF power devices to be made. However, the packaging materials that will withstand the higher operating temperatures for these devices do not yet exist. The EMPF is already engaged in assessment of new packaging technologies for high temperature electronic assemblies, both in the RF and the high power electronic technologies needed for DDG-1000 applications.

3. Liquid Crystal Polymer Materials

This is a class of polymer materials that are becoming available as conventional laminates from the existing printed circuit laminate suppliers. They have a wide range of attractive RF properties, such as low RF loss and low water absorption. They are potentially useful in the near-hermetic applications and could, combined with the near-hermetic coated chip, constitute an important part of the future affordable, lightweight, reliable RF Module. The EMPF is not currently engaged in the Liquid Crystal material validation.

continued on page 11

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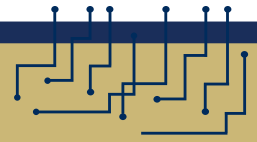
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The EMPF Monolithic Microwave Integrated Circuit (MMIC) environmental coatings project included testing the performance of wafer-level near-hermetic coatings used on several RF devices. RF testing was performed on gallium arsenide RF amplifier test die at regular intervals after temperature humidity biased (THB) exposure. These die were packaged in pin grid arrays (PGAs) and this testing was performed using a manual probe testing set-up. It was performed in an efficient and accurate manner to prevent scheduling delays with the environmental equipment. Below are some tech tips that may be useful for developing an RF test for similar wafer open lid devices.

Design for Test

- Device testability should be designed into the test samples whenever possible. In the case of the MMIC Environmental Seal Project, a matrix of various coating options tested included uncoated, organic, silicon carbide and organic/silicon carbide coated devices. In order to test these devices the chip surface was exposed to the RF probes. A separate test pad chip area was implemented into the design to provide a stable platform for manual RF probing. Traditionally, hermetically sealed devices could not be included in this test group because the test pads for the devices were sealed under the lid.
- The devices were designed into a PGA package so that a pin and socket could be used during testing. The pin and socket set-up creates a solid platform for securing the devices during testing. At the same time, the sockets allow the devices to be easily removed after probe testing. Similar sockets were used for environmental testing to help facilitate quick and safe transfer of the devices from the test chambers to the storage boxes.
- Adequate spacing between devices is also a requirement for efficient testing. There should be no overlap between adjacent test pads and no hindrance between devices. In our case, a small chip resistor between FET test pads required lowering of the entire sample stage to prevent crashing the delicate RF probes during testing site changes.

Select Robust RF Test Equipment

- Having the proper test equipment is also an important part of efficient RF testing. This allowed fast transitions between samples, reproducibility, and excellent reliability. Equipment used for RF testing of FETs evaluated in the environmental coating project included a SUSS Microtec PM5 probe station fitted with RF probes. The probes were constructed using a MEMS process that makes them more robust than other types of probes. The test device was powered by a HP model 3610A power supply (VS1) and a Keithly model 2420 (VS2) source meter. Gain measurements were recorded by an Anritsu 37347D network analyzer which allowed measurements at specific frequencies. This set-up proved to be extremely consistent.
- A main concern when performing manual RF probing is maintaining the planarity of the probes during testing. It is extremely easy to apply excessive pressure on the pad surface and knock one of the signal-ground-signal probes out of alignment. Also, if the height of the test pad is inconsistent, partial contact may result. It is suggested that robust RF probes be utilized to prevent planarity problems. Each probe tip acted as a contact spring providing solid contact with pads of different heights.

Use the Correct Testing Parameters

- Some common RF testing parameters include S-Parameters, Voltage Standing Wave Ratio (VSWR), RF-intermediate frequency (IF) - local oscillator (LO) isolation, phase noise, carrier suppression, gain compression, I/O balance, conversion gain, IP3 (TOI), noise figure, and RF power. It is important to match the correct testing parameter with the proper device function. The S-parameters (scattering parameters) were used to measure device performance for the FETs tested in the environmental coatings project. These parameters are important for verifying proper signal transfer.



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Manufacturer's Corner

Seica Functional Test Equipment

Within the defense/aerospace sector, the re-hosting of legacy test programs from obsolete test equipment is critical to meet product sustainment requirements. As the life of Automatic Test Equipment (ATE) is often shorter than the life of the product or program, this condition may jeopardize usage of existing test environments and diminish through-life-support (TLS). In addition, the costs and time delays to migrate test program sets (TPS) to new ATE environments every few years, is not a cost-effective option.

Recently, a challenge was presented by a customer to migrate TPS from an obsolete test environment to the Seica Valid VIP Test System. The requirements posed by the end user were ambitious and demanded a comprehensive approach to the migration solution. The original ATE was equipped with 4 D2 (32 channels) and 10 D3 (240 channels) cards for digital test. The D3 channel cards were connected to corresponding A3 cards to become fully hybrid and assure analog test capabilities. The program did not take advantage of the multiplex capability of the ATE channel cards, so the effective requirement was limited to 272 hybrid pins/channels. The technology of the boards tested requires TTL levels; however, for some boards, digital, low speed signals between $\pm 15V$ or $0/24V$ are required. All digital test programs were generated via LASAR simulation, but some local modification (or extensions, like memory tests) were apparent. Test programs were executed at moderate speed, usually around 2-3MHz, rarely reaching the 5MHz limit of the D3 channel cards. All digital test programs included go/no-go and guided probe diagnostics; the fault dictionary was not utilized.

Analog, parametric tests include DC force, and measure through I/O pins of the board, performed by internal ATE instrumentation routed via the A3 cards. Specific time/frequency tests were added using the internal time measurement system (TMS) and routing it through the digital 2-lines switching inherent with the structure of the digital channel cards.

For each TPS, validation of the migration process included, loop-testing against three boards and verification of the good-diagnostic results via insertion of five physical faults.

The end user expressed the need to maintain the LASAR simulation environment to assure a comprehensive process of generation, validation, coverage assessment and easy modification for the digital part of the test programs. The Target Test System was an excellent match and in some areas outperformed the obsolete system. Identified differences were efficiently addressed and met the client's requirements.

To prevent the need of manual intervention, within the program translation software, Seica implemented automatic adjustment of the edge positioning where required, with monitoring of such modifications.

Both the legacy ATE and Valid System have test oriented languages with very similar structures. Digital test patterns, including logic states and timing information, are dealt with in the same manner and maintain a one-to-one correspondence. Valid System provides a friendly, user-oriented debug environment to ease validation of digital and analog test programs. The translation process, encompasses the obsolete test programs, and re-builds the Multi-Main structure to maintain operation on separate test modules.

Digital test debug takes advantage of the data acquisition memory of the channel cards and offers a very flexible logic analyzer capability across all I/O of the board under test. Modifications were promptly implemented and quickly back-annotated through incremental compilation. Diagnostic guided probe data can be verified, edited or learned from a reference node.

The process was extensively bench-marked for comprehensiveness, quality and overall advantages against alternative solutions. The verification was done against a complex digital board, migrating go no/go and guided probe diagnostics both via the LASAR/L2POST and the L2/XEC source paths. The full solution included a fixture adaptor to host the old fixtures and a conditioning harness to allow test and diagnostics at different temperatures.

For additional information on Seica Test equipment or to schedule a demonstration of the Seica Test equipment located at the American Competitiveness Institute, please contact Robert N. Berta; telephone at 610-362-1200 ext 253 or via e-mail at rberta@aciusa.org.



Robert Berta - *Robert* is the Business Development Representative at ACI. Comments or questions pertaining to this article can be sent to rberta@aciusa.org

RF Modules Technology Roadmap (continued from page 8)

4. Silicon Germanium System-On-A-Chip (SiGe SOC)

This is the next step in RF Module integration presently being pursued on a ManTech program by the EMPF and one of its Industrial Advisory Board (IAB) members. Novel new interconnection of these new unique integrated SiGe SOC RF components will be incorporated, with the first application scheduled for DDG-1000. This is a potential gap-filler, as it represents a level of electronic integration in RF Modules that could lower the parts count for a given assembly thus lowering cost and increasing reliability. (Figure 4-3)

5. Thermal Management

This is another roadmap area that arises in any discussion of RF Modules. There are several ongoing EMPF/ManTech programs on thermal management, any of which can be applied to RF modules. These include the EMPF thrusts on Integrated Power Systems for Integrated Fight Through Power. The EMPF has been specifically involved in RF Packaging thermal management comparisons from RF Packaging programs conducted in recent years.

The EMPF continues to support the RF Module TWG of the JDMTP in their efforts in RF Roadmapping. Current and proposed Navy ManTech projects will continue to help identify potential critical issues in RF Module packaging and manufacturing issues.



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Free Electronics Manufacturing Assistance
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The analytical services laboratory at the EMPF provides a full range of solutions tailored for the electronics manufacturing industry. All testing is conducted in accordance with IPC, JEDEC, ASTM, Belcore, and MIL-STD specifications.

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- Vibration Testing
- Thermal Shock Testing
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- Level 1 component failure analysis

Contact the EMPF helpline for any of the above laboratory services at:

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Skills

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April 3-4

Chip Scale Manufacturing

February 20-22

Electronics Manufacturing

Boot Camp A

January 29 - February 2
April 16-20

Boot Camp B

February 5-9
April 23-27



Certifications

IPC J-STD-001 Instructor Certification

January 8-12
February 12-16
March 12-16

J-STD-001 Instructor Recertification

January 17-18
February 21-22
March 21-22

IPC-A-610 Instructor Certification

January 22-26
February 26 - March 2

IPC-A-610 Instructor Recertification

January 16-17
February 20-21

WHMA-A-620 Wire Harness Manufacturing (Operator)

March 13-15

IPC-7711 Certified IPC Specialist (CIS) SMT Rework

February 12-14

IPC-A-600 PWB Acceptability

January 3-5
February 27 - March 1

IPC Challenge

January 17
February 23
March 23

IPC-7711/7721 Certified IPC Specialist (CIS) SMT Rework and Circuit Repair

February 12-15

IPC-7711/7721 CIT Recertification

February 20-21

IPC-7721 Certified IPC Specialist (CIS) Circuit Repair

February 5-6

IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCB's

February 5-8

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March 26-27

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April 11-12

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March 6-8

For more information, please call (610) 362-1320 or email: registrar@empf.org

For a complete course schedule, visit:

www.empf.org/html/empfasis/emlc/upcoming.pdf

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