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*The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government centers and laboratories in the U.S.*

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## Power Electronics and Packaging Facility

As a part of meeting the U.S. Navy's goals for integrated power and propulsion, Navy ManTech, through the National Electronics Center of Excellence, will establish a power electronics assembly and packaging capability. This will entail analytical and electronic packaging equipment that will be used to support current and future U.S. Navy surface ship platforms that require advanced power electronics. It will also provide power electronics device prototyping capabilities for the U.S. Navy and will enable device level failure analysis and reliability testing on power electronics and high power RF components.

The use of reliable power electronics is critical to the DDG-1000 multi-mission destroyer (Figure 1-1) and other future surface ship platforms. Several demands will be placed on future power systems used in U.S. Navy ship programs. Specifically, the following challenges must be addressed when considering insertion of new technologies into advanced all-electric ship platforms:

- ◆ Power electronics used in advanced ship platforms must provide higher current density, switch at higher frequencies, and operate at higher temperatures.
- ◆ Power electronics packages available today are not designed or built to meet environmental and operational demands.
- ◆ The risks associated with inserting advanced devices on board future DDG-1000 and other future surface ships must be mitigated.
- ◆ Power electronic systems must be reliable, maintainable, and supportable.
- ◆ New technologies must be thoroughly tested and failures anticipated prior to implementation.
- ◆ Commercial materials suppliers and component vendors are risk averse.
- ◆ Advanced power devices must be applied to power systems used in future surface ship platforms.



Figure 1-1 – DDG-1000 multi-mission destroyer

(image courtesy of Northrop Grumman Corporation)

Utilizing the Electronics Manufacturing Productivity Facility (EMPF) in Philadelphia, a U.S. Navy Center of Excellence (COE), the power electronics assembly and packaging laboratory will analyze, repackage, and test advanced semiconductor electronics. The COE also will provide a source for the development of packaging materials for technologies such as wide band gap and advanced semiconductor devices. This development and testing will be essential to aid and shorten the development cycle for the DDG-1000 and other advanced surface ships.

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## Power Electronics and Packaging Facility (continued from page 1)

The facility will benefit future U.S. Navy surface ship platforms by developing capabilities and solutions for the following:

- ◆ Electronic packaging for high power semiconductors
- ◆ High temperature wire bonding materials and techniques
- ◆ High temperature die attach materials and techniques
- ◆ Near-hermetic high temperature housing materials, die coatings, and encapsulates
- ◆ Simulations and models for mechanical, electrical, RF, thermal, and thermo-fluid designs
- ◆ Shorter R&D cycles for RF devices, systems in a package (SiP), and power semiconductor packages and materials
- ◆ Packaging for high thermal conductivity materials, such as adhesives, thermal pastes, thermal heat spreaders, heat sinks, and die attach solders for junction temperatures greater than 200°C
- ◆ More affordable commercial packaging solutions for up to 200°C operation, high current density packages and modules, high frequency packages and modules, and high voltage packages and modules

The development of an advanced power electronics assembly and packaging process capability will require modern equipment to build advanced prototype module packages. The COE will utilize flexible precision  $\mu\text{m}$  accuracy placement equipment for placing flip chip die, optical components, and face-up die using adhesive, eutectic, or solder

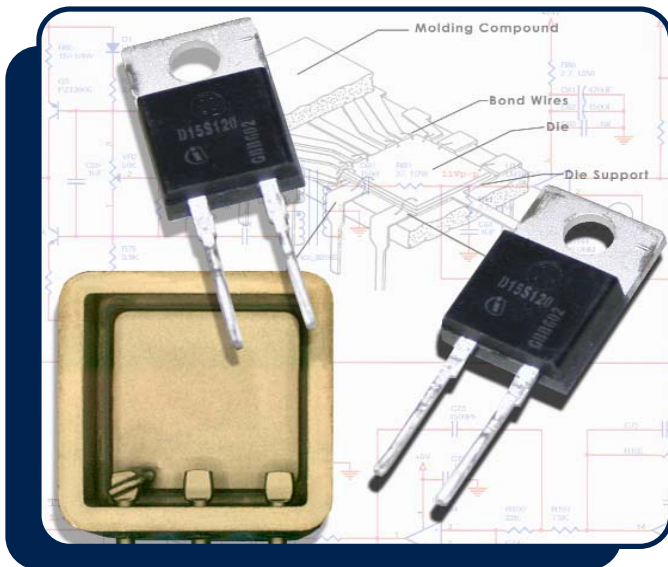


Figure 1-2 – The EMPF will provide packaging solutions for power applications for the U.S. Navy through design, testing, and manufacturing with new materials and methods.

technologies to bond the semiconductor die; a high-speed thermosonic ball-and-stitch wire bonder; a class 10,000 clean area that provides HEPA filtering of the existing room air to remove contaminating particulates; and dedicated ovens for epoxy curing, package bake-out, and after plasma cleaning to assist with repair of defects. The manufacturing equipment to be used will enable the COE to process emerging power technologies and to experiment with new materials and advanced techniques. This equipment will be coupled with existing EMPF manufacturing and process capabilities to provide a full-service power device packaging facility.

In addition to its production capabilities, the assembly and packaging laboratory will be a proof-of-concept facility that will employ analytical techniques such as acoustic microscopy and field emission scanning electron microscopy. This will compliment the manufacturing capability of the packaging lab through the ability to evaluate new technologies such as advanced substrates, die attach materials, and wire bond materials. This added failure analysis capability will be tailored specifically to high power devices to uncover limitations in materials and manufacturing processes. The diagnostic equipment also will be used for manufacturing process control.

The power electronics assembly and packaging facility will address the packaging requirements for high-reliability systems that have a significant need for higher power density, higher operating frequencies, and improved thermal management. The technologies developed at the EMPF packaging facility will have potentially wide applicability to Navy programs, and will be immediately utilized to support current and future Navy manufacturing technologies for DDG-1000. The laboratory can be used to determine package requirements, build reliable packages, and qualify the packaging for use in high-reliability applications. In these applications, outlining power, performance, and packaging details in terms of form/fit/function will be paramount. The laboratory also will aid in designing and/or improving device package layout, including device orientation, wiring configurations, and schematics. This will allow for the best electrical and thermal performance for the device. The laboratory will enable new packages to be built using new die, substrates, and attach materials. Finally, improved wire bonding materials and techniques, including enhanced materials and processes for high temperature operation, will be an additional benefit of the packaging facility.

The ability to test and analyze prototypes is integral to the ability to assemble improved power electronics packages. This reason-enhanced testing and analytical capability will be built into the facility, complimenting the packaging capability and qualifying materials and processes.



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# Lead-Free Training

The term lead-free has caused a certain degree of trepidation among board shops and assembly houses across the entire spectrum of electronic packaging. RoHS legislation has reached its full realization date as of July 1st, 2006, requiring engineers and manufacturers to provide quick solutions for both the manufacturing and reliability of lead-free assemblies. Despite all of the misgivings about the transitory period between the initial stages of lead-free implementation and the eventual maturation point, there are some steps from a technical and manufacturing perspective that can be taken to mitigate lead-free conversion. By now, any remotely interested party to the lead-free transition has heard the catch phrase "lead-free is not a drop in process." This is an established truism intrinsic to most manufacturing processes, and is perhaps more relevant in the case of lead-free due to the number of manufacturing sectors that are involved.

For instance, the selection of a lead-free solder can be daunting, as illustrated by the choice of solder alloys displayed in Table 2-1. These candidates were the result of a study cited by NCMS<sup>1</sup> in an attempt to narrow down the selection process to 8 alloys from a larger pool of 79. Even so, this is not an exclusionary or comprehensive list by any means, with other alloys having been introduced by other consortiums and organizations. The alloys are further classified

Alloy	Melting Temperature
SnPb	183° C
SnBi	138° C
SnAgCuBi	215° C
SnAgCu	218° C
SnAg	221° C
SnAgCuSb	222° C
SnCu	227° C
SnSb	240° C
AuSn	280° C

Table 2-1 – Lead-free alloys and their melting temperatures

<sup>1</sup>NCMS Lead-Free Alloy study 1993-1998

into three general application categories: Reflow Solder, Wave Solder, and Rework Solder.

Each of these solders has unique physical attributes, beyond their inherent melting points, that would be of interest to the manufacturing sector while converting to a lead-free process. Inadequate wetting ability can affect the performance specifications of a PCB assembly if it does not meet the criteria for solder joint coverage. Wetting and issues relating to higher temperature application of the lead-free solders can be controlled, and their effects mitigated, by adjusting reflow profiles, wave profiles, conveyor speeds, flux selections, and other parameters that are within the scope of the specific manufacturing process.

PC board finishes contribute to lead-free uncertainty as well, and add a second-level factor to the interaction with the solder. Some of the more popular board finishes include:

- ◆ Immersion Tin
- ◆ Immersion Ag
- ◆ ENIG
- ◆ OSP
- ◆ HASL
- ◆ Palladium/Nickel

Component leads are also available in a variety of plated metals, from pure tin to the more expensive Nickel-Palladium finishes. SAC (Tin-Silver-Copper), SnAg, Ni, and Pd round out a list of the more popular component finishes currently available.

There are numerous lead-free choices available for manufacturers. Yet despite the massive number of possibilities, the manufacturing sector has been able to adapt lead-free processes while its supporting infrastructure is being built and its material selections are narrowing. Process incompatibilities can often be slow, costly, and painful to resolve, but there is no lack of effort in the industry to do so, with many studies showing improved results in making the lead-free transition.

With such a broad range of metallurgical selections for solder, PCB finishes, substrates, component types, and component finishes, there is a need to extract reliable information to pose as a guideline for lead-free packaging at various levels. At the EMPF training center, we offer a comprehensive approach to lead-free training that will allow participants to gain an understanding of the technical issues surrounding the implementation of lead-free solders in an electronics manufacturing environment. Students will acquire the tech-

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## Die Attachment Technology

An integrated circuit chip is also called a die. This is because the chips are imaged, metallized, and processed in the form of a wafer of semiconductor material (usually single crystal silicon) that is later "diced" with a saw into a large number of individual chips, each one called a "die."

In most cases, each individual die is packaged into a plastic or ceramic package, such as a QFP (Quad Flat Pack), SOP (Small Outline Package), or one of the newer BGA (Ball Grid Array) or QFN (Quad Flatpack No-lead) packages. These packages are then soldered onto a PWB (Printed Wiring Board), usually along with other components, to make a PWA (Printed Wiring Assembly).

In addition to this normal type of assembly, there are two other ways of attaching a die to a PWA: Chip-on-Board (COB) and Flip-Chip-on-Board (FCOB). Figures 3-1, 3-2, and 3-3 (shown on page 8) show the three ways in which a die can be interconnected and attached to a PWB.

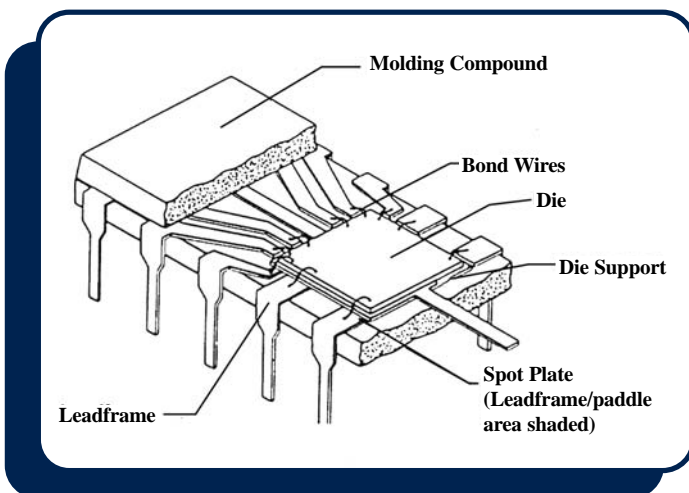


Figure 3-1 – Standard Dual Inline Package (DIP) Cutaway view showing die and bond wires.

There are basic similarities in the manufacturing operations for the die attach step in Figure 3-1, Standard Package Assembly and Figure 3-2, COB. The die is face-up in both the standard package and the COB direct attachment to the Printed Wiring Board. In contrast, for the flip chip die attach (as shown in Figure 3-3 on page 8), the die must be flipped so that the face of the die, with its I/O connections, is turned toward the board.

The equipment for the standard package and COB methods of die attach are quite similar, having the capability to dispense or print the die attach adhesive and to place the face-up die onto the lead frame or the board. However, the equipment used for the flip chip die attach must also flip the chip over so

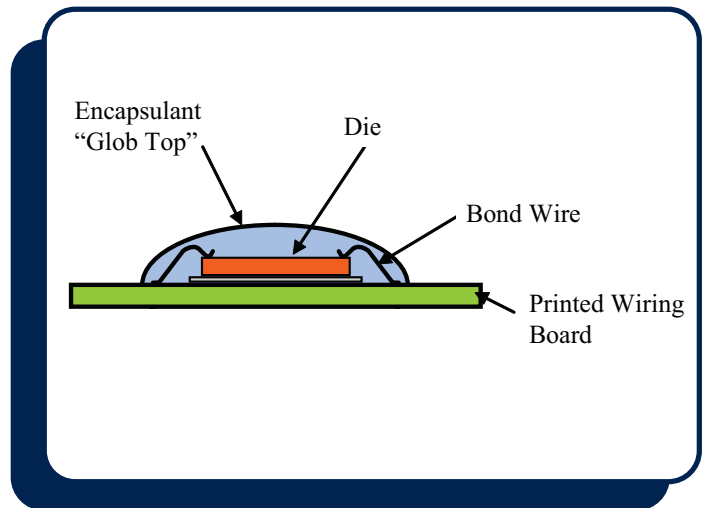


Figure 3-2 – Chip-on-Board (COB)

(Courtesy of Valtronic USA)

that it is face down to present the electrical interconnection pads (bumps) to the substrate, with both an upward-looking camera to align the I/O pads and bumps on the die, and a downward looking camera facing the conductor pads on the board.

Most typical surface mount or die attach machines, however, are equipped only with a downward-looking camera that will align the edges of surface mount components and/or bare integrated circuit die with fiducials or other features of the lead frame or board. For flip chip die placement, this is usually augmented with an upward-looking camera to allow face down alignment of the flip chip pads with pads on the board. It should be noted that packages are sometimes made using flip chip for the interconnection of the die, but those packages are usually Ball Grid Array or Chip Scale packages in which the "lead frame" is actually a PWB. The purpose of this type of package, with flip chip as the die attach method, is to minimize the electrical capacitance and inductance (parasitics) associated with wire bonds. This method of die attachment is often used for microprocessors or ASICs (Application Specific Integrated Circuits) with very high I/O counts that have the need for very good signal integrity at very high signal speeds.

Equipment that uses either solder or adhesive die attachment materials, and methods for executing die attachment for standard lead frame-based packages, or for COB face-up applications, is available with various degrees of placement accuracy.

In fact, placement accuracy has improved within the last five years to +/- a few microns. For instance, many manufactur-

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## Ask the EMPF Helpline!

*A customer recently called the EMPF Helpline with a question involving a piece of electronic hardware that they had built for qualification against Electromagnetic Interference (EMI). During radiated emissions and susceptibility tests, emissions were higher than limits allow, susceptibility affected the operation of the equipment under test, and the customer needed to know how to resolve this issue.*

These tests were conducted in accordance to the military standards for equipment qualification for EMI, known as MIL-STD-461E.

The EMPF suspected a shielding issue in the equipment. The unit being tested was contained in a metal structure, with only aircraft cable connections to interface outside the case. Self testing was unable to determine which piece of equipment in the test set up was affected. The initial arrangement of test cables routed through the wall of the shielded room (access panel) was as follows:

- ◆ Interconnecting test cables and shields passed through a pipe in an access panel to test equipment on a bench outside the shielded room.
- ◆ The cable shields terminated at a grounded bench top that the test equipment sat on outside the shielded room.
- ◆ Steel wool was stuffed in the access panel pipe around the cables.
- ◆ Aluminum foil was wrapped around each cable at each end of the pipe and taped.

The EMPF's first recommendation was to re-route the interconnecting test cables to comply with military standard test layouts. The next recommendation was to isolate the problem to either the unit under test or the interconnecting test cables. The test cables were covered with shielding material and grounded from the access panel to the unit under test, which caused the radiated emissions test levels to drop, indicating that the emissions radiated from the cables. The extra shielding material was removed.

Next, the interconnecting test cables shields were checked for deformities. Much of the webbing seemed flexed, or open in spots, and inner bundle wires showed through at the bends. Working the webbing (bunching) helped close these gaps. However, there was little change in the test results.

The customer then disassembled the connectors and verified a 360° termination of the shields. The outer shields were terminated in an aviation-type connector with a tapered slip ring tightened by a ring nut. Inner bundle shielded cables were terminated to ground pins. Still, there was no change in the test results.

The interconnecting test cables shields termination at the power cables breakout were checked to ensure a termination close to the line impedance stabilization network (LISN)'s ground. This end had metal tape connected to the ground plane. The tape was replaced with a buss wire soldered to 360° at the shield end and connected to the LISN's ground post, with little change in the test results.

The interconnecting test cables shields termination at the access panel were inspected for low resistance termination. Even though the D.C. resistance measurements indicated an acceptable connection, the RF characteristics of these connections may not have been acceptable. Therefore, the EMPF suspected poor termination at the access panel and recommended properly terminating the interconnecting test cables' outer shields at the access panel. On each shield end, a bus wire was soldered for a 360° termination. Then each shield's termination was connected to the access panel.

Radiated emissions tests levels dropped to within an acceptable range, and radiated susceptibility tests no longer affected the operation of the equipment being tested.

This scenario is an example of inferior interconnecting test cables causing undo concerns about a properly designed product. Conversely, interconnecting test cables that have more shielding than the installed cables can hide potential problems, which may lead to costly liabilities and possibly catastrophic consequences when the device in question is put into service.

Cables that are not representative of the actual installation can generate useless data and false test results. These tests are not intended to exercise and measure the limits of the support equipment outside the room where the device in question is being tested.

Several key points emerged from this troubleshooting exercise.

- ◆ Interconnecting test cables should be built to emulate the installed cables.
- ◆ Interconnecting test cables should terminate both at the equipment under test and the access panel.
- ◆ Interconnecting test cables should be contained in the shielded room and the excess routed on the bench.
- ◆ Test equipment outside the shielded room should be isolated (filtered) from the equipment under test inside the room.

The bottom line here is that it is recommended to terminate the interconnecting test cables and their shields, and all test equipment employed for EMI compliance testing should come as close as possible to the equipment actually being employed in the final installation to ensure the accuracy of the test results.



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## High Temperature Packaging for Power Devices

The U.S. Navy's next generation surface ships will utilize various power systems, such as Integrated Fight Through Power (IFTP), Electric Drive (ED), and Reconfigurable Zonal Systems. The present on-board power stations, however, are not adequate to support electric weapons or high power radar. A fundamental change in how electric power is converted, distributed, and managed will be required in order to fully utilize the electric power available aboard these new platforms. The concept of an "electric warship" will depend on the ability to rapidly shift power to major loads to support tactical needs. To ensure this capability can be met in a timely and affordable manner, there are technology issues that must be addressed at both the material and component levels.

One issue that must be addressed involves weight and size. Weight and center of gravity are critical concerns of the next generation power distribution system. The current methods for generating pulsed power require the use of heavy, bulky systems placed in areas that are not optimal for carrier design. One method to reduce the weight and size of the current iron and copper transformers used in legacy power distribution systems is to increase the switching frequency from 60 Hz to 15 - 20 kHz. The Solid State Power Station (SSPS), for example, uses this design principle. However, silicon exhibits high switching losses at these frequencies, so high power devices (e.g. Insulated Gate Bipolar Transistors - IGBTs) cannot operate at 10 - 20 kHz.

The new Wide Band Gap semiconductor materials, principally Silicon Carbide (SiC), offer superior materials properties to meet the higher power performance challenges. Continuous power switches, power diodes, and pulsed power switches fabricated from SiC offer reductions in on-state resistance and switching loss over conventional silicon power devices planned for future ship construction. For a given power rating, these components can operate at a higher duty cycle, leading to a reduction in the size of inductors and transformers in power circuits. SiC power electronics also extend solid state technology by offering higher break-

down voltage levels than current silicon technology, to address voltage levels presently managed by electro-mechanical switch technology.

Wide Band Gap semiconductors also represent a possible paradigm shift in semiconductor power density. As shown in Table 5-1, SiC devices can operate at higher temperatures and thus require less cooling. The higher blocking voltages, as compared to silicon devices, allow for the design of smaller and simpler high voltage components. Improved thermal management of semiconductors and passive components through upgraded packaging would allow more current to be handled by a given device and lead to improved power density designs.

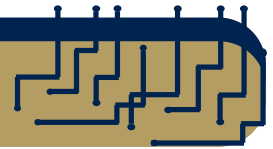
Power conversion equipment developed using SiC technology is projected to significantly reduce the workload and maintenance requirements for current and future carriers and is considered a critical step in achieving CVN 21 compliance with key performance parameters for weight reduction and ship stability. As indicated in Figure 5-1 (shown on page 9), use of SiC power conversion on Navy ships is expected to reduce the current conversion equipment size by approximately 60% and achieve weight savings approaching 2.68 tons for each converter implemented with the new 2.7 MVA transformer technology.

The current packages that are available for SiC severely limit the device applications. To realize the benefits of SiC device technology, designers and engineers need packaged components. However, nearly all component packaging materials are designed for use with silicon devices. Therefore, these packaging solutions were never intended for use above about 150°C. Such packaging would negate a major advantage of SiC devices, namely their high operating temperature capability. Operation of SiC Schottky diodes has been demonstrated above 350°C. High temperature packaging options include both polymer-based and ceramic-based solutions. Currently, the vast majority of high power packages are manufactured using polymers. It is expected that compatible polymer material sets can be found to allow operation in the 200°C - 250°C range. For operation above 300°C, ceramic packages are much more likely candidates. Above 300°C diffusion, oxidation and corrosion are all much more active processes than at 150°C, so new metallurgical interconnect solutions will be required for long-term reliability.

Property	Si	4H-SiC	Benefits
Energy Band Gap (eV)	1.12	3.26	SiC devices can operate at much higher temperatures
Electric Breakdown Field (kV/cm)	300	2200	SiC can withstand much larger voltage gradients
Thermal Conductivity (W/cm-°C)	1.5	3.0 - 3.8	SiC can efficiently conduct heat away from high power junctions

Table 5-1 Comparison of the Material Properties of Si and SiC

*continued on page 9*



With so many variables, troubleshooting wire bond programs can be tricky. The tips that follow will make the process a bit easier.

**Tip 1:** Confirm that the wire bonder's setup is correct.

- a) Install a new wire bonding tool and set screw. If not available, make sure the old bonding tool is the correct part number for the wire size being bonded. Under a microscope, at 10X minimum, inspect the tool and set screw to see if it is worn out or dirty. Reinstall the tool and seat the set screw to the manufacturer recommended setting with a torque wrench. Test the ultrasonics; if the ultrasonics are tuned and working properly, proceed with the setup.
- b) Install a new spool of wire. If new wire is not available, confirm the wire in the old spool is the correct size and alloy composition. Make sure the wire is not dirty, damaged, or spooled incorrectly. Verify the wire feeds smoothly through to the bond tool.
- c) Load the secured copy of the wire bond program into the wire bonder. Always keep a copy of the wire bond program in a secured area away from the production floor. You can easily reinstall the program if the production copy becomes corrupt.
- d) Using a calibrated thermometer, verify the heated stage is the correct temperature. A thermosonic process, gold wire bonding typically requires the product be heated to 150 °C.
- e) Using a setup sample, evaluate the program for repeatability and resulting bond strengths.

**Tip 2:** Bond surfaces must be clean, smooth, and free of contaminants. Use cleaning solvents to flush away contaminants from bond surfaces. Plasma cleaning will remove micro contaminants but in most cases will not remove debris or other macro contaminants. Oxygen plasma will remove organic contaminants. However, to remove inorganic oxides, you will have to use argon gas or a mix of argon and oxygen gas. The plasma from these gases will remove both organic and inorganic contaminants. Measure the effectiveness of plasma cleaning by placing a drop of DI water on the bond surface and visually examining the contact angle of the water drop. A high contact angle indicates surface contamination. A low contact angle, where the water drop spreads over the bond surface, indicates a clean surface.

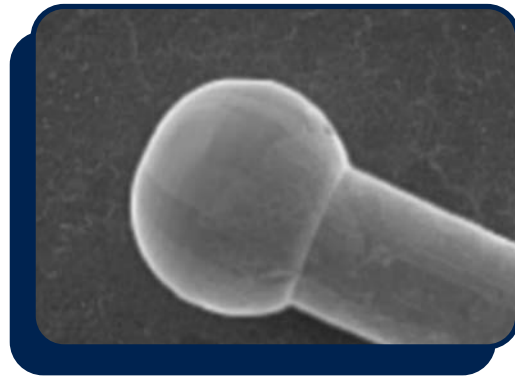


Figure 6-1 – Free-air-ball

(courtesy of Small Precision Tools, Inc.)

**Tip 3:** The product must be rigidly held. If the product moves during wire bonding, ultrasonic energy is lost and the bond will not form completely. Check your work holder, or make sure the tool is clamping the part rigidly before the wire bonding operation starts. The clamping should be repeatable. You may have to put a time delay in your program to allow the clamped part to settle before starting the wire bonding process.

**Tip 4:** Check for consistent and symmetrical free-air-balls. The diameter should be approximately 1.5 times the wire diameter (See figure 6-1).

**Tip 5:** Adjust the ultrasonics, force, and time. Change one parameter at a time, as changing all the parameters at once will make it impossible to determine which change has the most impact on improving the wire bond.

**Tip 6:** Replace the wire bond tool with a different lot number of the same tool, or use an equivalent tool from a different supplier.

**Tip 7:** Replace the wire with a different lot number from the same supplier, or use an equivalent wire from a different supplier.

**Tip 8:** Finally, check the equipment calibration, the bond head mechanisms, and the operation of the machine.

With good controls on incoming materials, dependable wire bond process control checks, and regular equipment maintenance and calibration, the wire bonding operation will run defects of less than 100 ppm.



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# Die Attachment Technology

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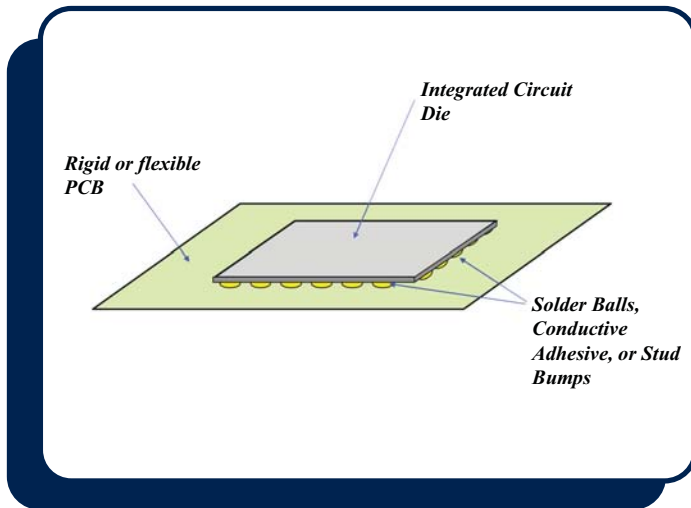


Figure 3-3 – Flip Chip (FC) or Flip-Chip-on-Board (FCOB)  
(Courtesy of Valtronic USA)

ers are claiming 5 - 10 micron placement accuracy. For a premium price, accuracies down to +/- 1 micron are now available. These accurate die placement machines, combined with the most recent advances in wire bonding equipment allowing extremely accurate wire length, loop height, and loop shape control, allow COB with wire bonding to compete with flip chip in RF (Radio Frequency) applications where the accuracy of the parasitic reactances at each I/O pad of the die is a factor in the overall design. In applications such as this, the extremely precise die position, relative to other die in the assembly, defines an accurate bond wire length (and therefore resistance) and capacitance and inductance (wire loop control) that can become a predictable and reliable part of an RF design. Die attachment accuracy is now a formidable tool in such applications.

Some flip chip systems do not enable "self alignment" by utilizing the surface tension of liquid solder (molten solder bumps) to pull the die into alignment with the substrate pads. Those applications (using non-melting metal bumps) benefit because the original placement of the flip chip die can now be sufficiently precise so that no such "self-alignment" is required. Such a machine is shown in Figure 3-4. This machine is being used to flip chip die attach thousands of die per hour for an RFID (Radio Frequency Identification) Tag application. It has been shown to be suitable for silver bumped flip chip attachment in the EMPF Bumped RF Devices project.

As with die attach equipment, adhesive die attach materials (applied to adhere the die to the PWB or lead frame) are also undergoing a revolution. The EMPF is currently evaluating an academically developed nanoparticle silver-based die

attach material for its potential uses in high power electronics, like those planned for the future DDG-1000 multi-mission destroyer. Because of its nanoparticle precursor, this silver paste becomes many times more thermally and electrically conductive than the solder materials usually used for this application. Upon sintering of the nanoparticles, thermal and electrical conductivities, many times higher than the solders or conductive epoxies that are traditionally used for this purpose, develop which approach those of metallic copper.

The benefit of the nanoparticle conductive silver paste is another area where flip chip improvements might be possible. This is particularly true in the area of thermal management for flip chip devices using solid metal bumps, where any type of solder attachment of the metal bumps forms a high thermal resistance solder layer at each I/O site. Attaching the flip chip using silver nanoparticle paste could potentially alleviate these thermal bottlenecks.



Figure 3-4 – Die Attachment Machine capable of any of the three attachment schemes discussed.  
(Photo Courtesy of Tyco Electronics)

Die attachment, both in terms of equipment and materials, is only one of the many electronic packaging technology areas that hold opportunity for the constant improvement being pursued at the EMPF. Both the high power electronics being planned for DDG-1000, and the control electronics for GPS and IMU applications, will benefit from continued development of this technology.



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# High Temperature Packaging for Power Devices

(continued from page 6)

ACI is starting a ManTech project aimed at developing high power packages for use in the SSPS and other DoD applications. To be compatible with the commercial packaging infrastructure, these packages will be based on high temperature polymers. Operating temperatures are planned to be above 200°C. Besides providing the I/Os between the system and the microelectronic devices, the device packaging will provide:

- ◆ High voltage insulation
- ◆ Surface leakage passivation
- ◆ Moisture resistance
- ◆ Corrosion protection
- ◆ Mechanical protection
- ◆ Thermal management

A high power component can consist of one or more die that are mounted on a substrate. High power components often use high thermal conductivity die attach materials to mount the die on the substrates. High temperature solders such as gold-tin or gold-germanium can be used. Table 5-2 shows the metrics that will be used to evaluate technology developed to support Solid State Power Substation for the "all-electric" warship. For best reliability, the die are attached to high thermal conductivity substrates that have a low Coefficient of Thermal Expansion (CTE). Potential substrate materials include: aluminum nitride, beryllia, alumina, copper-tungsten alloys, and aluminum silicon carbide metal matrix composites. The bottom-side of the substrate will later be attached to a high capacity heatsink or thermal management system to extract the heat generated by the high power component.

Property	Baseline	Metric
<b>Operation Temperature</b>	~ 150°C (Si in plastic package)	≥ 200°C
<b>High Voltage Isolation</b>	6.5 kV (typical for Si PIN diode)	≥ 20 kV
<b>Current Handling Capability</b>	45 A (individual SiC PIN Diode)	110A
<b>Die Attach</b>	0.6 w/cm-°C (Au/Sn, 80/20 solder)	2.5 w/cm

Table 5-2 – Program metrics for polymer-based high power SiC device packaging

## SSPS

Solid State Power Substation

Reduction in Weight and Size Through SiC Based Technology

**Current Transformer**      **New Requirements:**

6 Tons

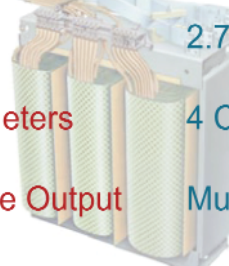
2.7 Tons

10 Cubic Meters

4 Cubic Meters

Fixed Single Output

Multiple Taps/Outputs



By beginning implementation of SiC based technology, increased functionality and power management can be achieved with significant reductions in weight and size. This will not only benefit the CVN 21 carrier platform, but will also be applied to the DDG-1000 ship program.

Project Test Date: 2010

Figure 5-1 – Projected benefits of SiC technology for the SSPS

All die intended for high voltage components must have all sharp corners and edges rounded to eliminate electric field concentration effects. This is often performed using automated grinding equipment. High voltage die also require surface passivation to eliminate surface leakage currents that often result from surface damage caused by wafer cutting and polishing operations. Surface passivation is often accomplished by the application of a very uniform coating of polyimide directly on the bare device. Moisture resistance can also be achieved with a uniform, pinhole-free coating deposited on the device. Mechanical and corrosion protection are achieved through encapsulation with thicker layers of polymers. For corrosion protection, it is important that the encapsulation does not have any cracks or interconnected porosity that will allow ions to be transported to the device. Besides these layers, a packaged device might have other polymer structures that become part of the package. A power device package may be composed of a substrate, one or more die attached to a substrate with a die attach material, wirebonds, I/O leads or screws, and three or more different polymers. These different materials encompass a broad spectrum of properties. Component reliability is critically dependent on the compatibility of all materials that comprise the package.

When designing a high power package that will have large area die, a trade-off is always necessary to balance the CTE

*continued on page 11*

## Manufacturer's Corner

### Orthodyne PowerRibbon™ Wire Ribbon Bonder

Energy saving power management of high-current electric motors and battery-operated portable devices has led to more efficient power semiconductor silicon designs, primarily to accommodate higher currents coupled with lower resistance. To meet these stringent requirements, semiconductor manufacturers have utilized wire bonding processes that have increased the number of large aluminum wires per device to support higher current demands. This exacting process combines vibration and force to increase the surface temperatures of each component, resulting in enhanced molecular cohesion through the formation of intermetallic compounds between the wire and chip pad metals.

Wirebonding interconnects (via wire or wire ribbon) components and conducting paths. The most frequently used method of joining wires is ultrasonic welding, either with (thermosonic) or without (ultrasonic) heating of the bonding system. Wirebonds are found in a multitude of components, including automotive systems, computers, guidance systems, and medical instruments. The wire bond connections are inspected optically, using either a wire bond pull tester or micro-sectioning.

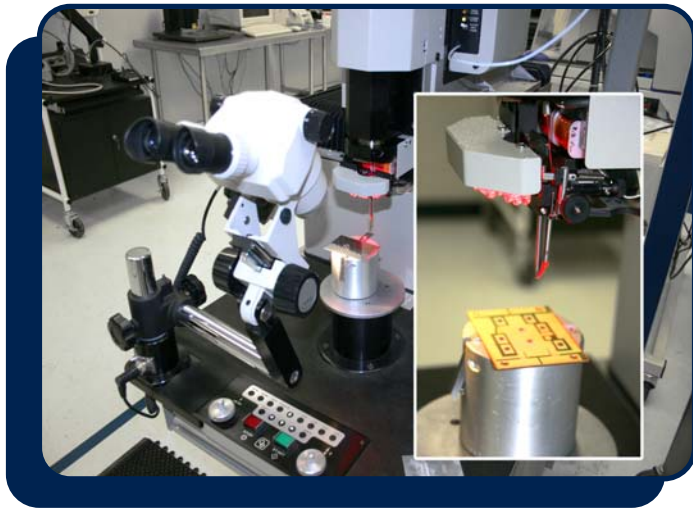


Figure 7-1 Orthodyne PowerRibbon™ Wire Ribbon Bonder

Two terms commonly associated with the process of wire bonding are wedge and ball, each of which defines the subsequent profile of the wire being welded to the device surface. In each case, the selection and condition of materials is vital to the success of the wire bonding process. Aluminum wire, for example, is always wedge bonded, as the aluminum is not conducive to forming the "ball" used in ball bonding. Gold wire, on the other hand, is commonly ball bonded, and the ball can be formed by melting the end

of the gold wire in air, since gold will not oxidize and forms a molten ball easily on flame-off. In special cases, copper wire is used in ball bonding, but it requires a reducing atmosphere to form a ball without oxidizing significantly. In addition, gold ribbon is an excellent substitute for gold wire, due to its compatibility with high frequencies, which makes it an ideal choice for fine pitch applications in the manufacturing of telecommunication systems and peripheral equipment.

Equipment selection for wire bonding should be based on the requirements of the component, such as current, voltage, and environmental stress; the selection of wire bond materials (usually aluminum or gold); and, most importantly, the vendors' technological capacity. For example, bonding equipment for heavy aluminum wire wedge bonding is configured to apply higher bonding loads to meet the requirements of high current levels. Furthermore, procedures that eliminate stress during handling, fabrication, and assembly are critical to achieving success in the manufacturing process. This requires developing, implementing, and constantly monitoring vendors, in-coming inspection, in-house storage, and handling procedures to achieve successful, repeatable manufacturing results.

Orthodyne's PowerRibbon™ is industry recognized as a leading technology designed to work with current package design standards for heavy aluminum wire. An environmentally friendly ultrasonic interconnect process similar to aluminum wedge fine wire bonding, PowerRibbon™ Technology combines the flexibility and ruggedness of the large aluminum wire bonding process with the higher productivity and product performance of copper clip bonding. PowerRibbon™ can be retrofitted to the Orthodyne M360C wire bonder and supports ribbon sizes ranging from 30 mil x 3 mil to 80 mil x 8 mil. Additional ribbon sizes, predicated on requirements, are available.

For additional information, or to arrange for a demonstration of the Orthodyne PowerRibbon™ wire bonder located within the factory of the EMPF, please contact Bob Berta at 610-362-1200 ext 253 or via e-mail at [rberta@aciusa.org](mailto:rberta@aciusa.org).



Author of article: *Bob Berta* – Bob is the Business Development Representative at ACI. Comments or questions pertaining to this article can be sent to [rberta@aciusa.org](mailto:rberta@aciusa.org).

# High Temperature Packaging for Power Devices

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mismatch between the various materials that comprise the package. High power packages are designed to carry current pulses in the range of 100A - 100,000 A. This forces the package to have relatively large conductors made from high conductivity metals such as copper. All high conductivity metals have high CTEs (e.g., the CTE of copper is 16 ppm/°C). However, microelectronic devices have a low CTE (e.g., the CTE of SiC is 4 ppm/°C), which creates significant packaging issues for devices expected to be routinely cycled between room temperature and operating temperatures exceeding 200°C. For packages to be reliable, they must remain crack-free after undergoing many thermal cycles. As devices are designed for higher and higher operating temperatures, the thermal cycling stresses become larger and larger. Compatibility must be ensured by testing high power components to failure and understanding the failure modes. Since the CTE mismatches in a package are quite substantial, the materials must be compliant. In addition, all interfaces within the structure must exhibit excel-

lent wetting properties so high adhesion strength is developed. In high voltage components, small cracks (especially near metallic conductors) are a source of partial discharge events, which will eventually lead to dielectric breakdown failure.

In conjunction with a commercial supplier of packages, ACI expects to begin a Navy ManTech project to develop high temperature packaging for high power SiC devices. The program will ascertain a compatible materials set and will develop a reliability model for the package.



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# Lead-Free Training

(continued from page 3)

nical insight necessary to select the proper choices of components, alloys, substrates, finishes, designs, and environmental tests to achieve a level of reliability needed for various applications.

Most importantly, the EMPF offers hands-on training that gives students first-hand experience with the manufacturing issues surrounding the implementation of lead-free processes. Students will learn:

### State of the Market Concerns

- ◆ Market drivers and pressures for lead-free implementation
- ◆ Legislative initiatives, including RoHS and WEEE

### Material

- ◆ Lead-free solder alloys
- ◆ Board Finishes
- ◆ Substrate impact
- ◆ How lead-free alloys affect components
- ◆ How to select the appropriate lead-free materials

### Manufacturing

- ◆ Understanding the process variables required for lead-free manufacturing
- ◆ Designing experiments for the introduction of lead-free processes in a manufacturing facility
- ◆ SMT reflow
- ◆ Wave soldering
- ◆ Hand soldering for rework and repair

### Reliability

- ◆ Designing for harsh environments
- ◆ Thermal cycling behavior of lead-free solder joints
- ◆ Shock and combined environment behavior of lead-free
- ◆ Modeling for reliability
- ◆ Mitigating the effects of tin whiskers

### Case Studies

- ◆ Critical findings from ACI experience
- ◆ Failure modes
- ◆ Largest causes of variability

Remember, adequate preparation in lead-free processes will allow potential problems that may arise in future designs.

For more information on lead-free training, or other classes available from the EMPF, including IPC certifications, please contact the registrar at (610) 362-1295, via email at [registrar@empf.org](mailto:registrar@empf.org), or find course descriptions on the web at <http://www.aciusa.org/courses>.



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# EMLC Upcoming Course Schedule 2006

## Skills

**BGA Manufacturing, Inspection & Rework**  
September 21-22  
October 12-13  
November 28-29

**Chip Scale Manufacturing**  
October 24-26

## Electronics Manufacturing

**Boot Camp A**  
September 11-15  
November 6-10

**Boot Camp B**  
September 18-22  
November 13-17

## Certifications

**IPC J-STD-001 Instructor Certification**  
September 25-29

**IPC-A-610 Instructor Certification**  
September 18-22

**IPC Challenge**  
September 27  
November 1  
December 13

**WHMA-A-620 Wire Harness Manufacturing (Operator)**  
October 3-5  
November 29 - December 1

**IPC-7711 Certified IPC Specialist (CIS) SMT Rework**  
November 28 - December 2

**J-STD-001 Instructor Recertification**  
September 18-22  
October 16-20  
November 6-10

**IPC-A-610 Instructor Recertification**  
September 25-26  
October 30-31

**IPC-7711/7721 Certified IPC Specialist (CIS) SMT Rework and Circuit Repair**  
September 11-15

**IPC-7721 Certified IPC Specialist (CIS) Circuit Repair**  
November 2-3

**IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCBs**  
September 5-8

## Continuing Professional Advancement in Electronics Manufacturing

**Lead-Free Manufacturing**  
September 7-8  
October 17-18

**Design for Manufacturability**  
October 9-10

**Failure Analysis and Reliability Testing**  
October 3-5  
November 27-29

**For more information, please call (610) 362-1320 or e-mail: registrar@empf.org**

For a complete course schedule, visit:  
<http://www.empf.org/html/empfasis/emlcupcoming.pdf>



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