empfasis

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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government centers and laboratories in the U.S.

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In This Issue

DDG-1000/LCS/CVN-21/ Virginia Class Affordability

To increase its current fleet from 281 ships to 313 ships, the Navy plans to build between seven and fourteen ships a year for the next 5 years. These include one CVN-21 aircraft carrier, 23 Littoral Combat Ships (LCS), eight DD(X) destroyers and five Virginia class attack submarines. This number will makeup the current 32 ship shortfall and will include replacements for ships scheduled to be retired. Adm. Michael Mullen, the Chief of Naval Operations, estimates it will take an average of $13.5 billion a year in 2006 dollars to support this effort. With a requested $10.57 billion 2007 budget there is a $2.93 billion shortfall starting next year which has initiated a ship building affordability initiative in the Navy. The EMPF, thru the Office of Naval Research (ONR), has been actively addressing this initiative through innovative investment recommendations in electronic manufacturing technology.

Integrated electronics, propulsion & weapons systems are key high-cost contributors to ship acquisition. These costs are realized due to custom requirements and correlating custom electronic designs. Risks associated with the integration of advanced electronic device and material technologies are inhibiting the adoption of state of the art systems and subsystems that will create transformational cost reductions to current naval ships. The EMPF has been involved in reducing the acquisition cost of Electronics technologies for specific systems/subsystems on target platforms through the introduction of less expensive, smaller, lighter and better performance electronic technologies. Cost savings can also be realized through the insertion of COTS, open systems, and an increased amount of electronic functional integration. Potential systems of interest are:

Figure 1-1 CVN-21

- **Radar**
  - Affordable T/R Modules for Phased Array Antennas
  - Affordable Power Amplifiers for Phased Array Antennas
  - Affordable Backplane and Support Electronics
- **Communications Systems**
  - Combined Antenna Functions to Drive Down the Acquisition Cost of Antennas
  - Improved Affordability through High Power Integrated Power Amplifiers
- **Sonar**
  - Affordable Transducers and Transducer E-O Networks through Chip Scale Integration and Manufacturing Process Improvements

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DDG-1000/LCS/CVN-21 Affordability
(Continued from page 1)

– Affordable High Energy Acoustic Power Amplifiers and their Networks through Chip Scale Manufacturing Process Improvements.

- **Navigation**
  - New sensor technologies such as fiberoptic gyros
  - integrate manufacturing technologies into the SSBN
  - Integration of “stovepipe” navigation technologies (Doppler Velocity Log and Fathometer) into one FOG based system

- **Power Electronics**
  - PCM Affordability through Improved Power Electronics Module (PEM) Manufacturing
  - Motor Controller Affordability through Improved Enclosure Communications Module Design and Manufacturing
  - Permanent Magnet Motor Monolithic Stator (PMMS) Affordability through Improved Segmented Stator Manufacturing

- **Propulsion**
  - Affordability through Maximized Efficiency in Manufacturing of propulsion electronic converters
  - Line Replaceable Unit (LRU) affordability through improved heat sink design and power conversion module electronics manufacturability

The EMPF has several projects underway aimed at reducing the costs of shipboard electronics. Hermetic sealing of T/R modules for phased arrays project is investigating the cost reductions for radar t/r modules by eliminating the expensive hermetic enclosure and replacing it with a MMIC wafer level coating that provides the needed environmental protection.

Manufacturing of Light Activated Semiconductor Switches (LASS) will develop automated manufacturing processing for the production of reduced cost Light Activated Semiconductor Switches. Manufacturing and packaging of power systems for DD(X) and Carriers (Solid state transformer). SiGe SoC initially for conformal mounting on aircraft this technology is directly applicable to ship radars. LCS Phase 2 planned to start in FY 2007 will leverage the phase one effort investigation by building a prototype multifunction antenna for the LCS ship.

Figure 1-2 LCS

Enhanced 3D design and Production Process Methodology planned to start in FY 2007 will utilize statistical methods, production tolerance analysis and 3D RF analysis to improve first time yield and producibility of complex designs resulting in substantial cost savings for RF products. In addition the EMPF is investigating the affordability impact of the following:

Figure 1-3 DDG-1000

- Multi-function radar affordability through highly integrated Systems on a chip technology

- Reduced power conversion requirements through smart integration of stored energy

- Integrated submarine/shipboard navigation system

- Power conversion components and systems affordability through improved thermal management and manufacturing processes

- Manufacturability of low cost hi power SiC limiters/ switches for naval EW and radar systems

The EMPF will continue to be an active partner in the Navy’s ship building affordability initiative by developing projects that reduce the acquisition costs of ship board electronics through the introduction of advanced manufacturing processes, improved electronic devices, materials and system technologies. Expanded use of COTS, open systems and an increased use of electronic functional integration will be applied to ship board systems resulting in substantial savings to the Navy.

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IJP-J-STD-001D
Operator Proficiency Training

Operator proficiency trainingis being offered for IPC-J-STD-001D. This standard describes materials, methods and acceptance criteria for producing soldered electrical and electronic assemblies. This training is applicable for anyone who is responsible for the assembly of equipment built to the requirements of IPC/EIA J-STD-001.

The J-STD 001 Application Specialist course consists of five modules in which the duration can range from one to five days depending which modules are chosen to be taught. This modular design allows employers to select the appropriate amount of training to meet each individuals needs.

• **Module One:** which is the pre-requisite for modules 2 - 5, covers General requirements, materials, components, cleanliness, assembly and soldering processes. The remainder of the program is as follows:

• **Module two:** Wrapping, soldering, and inspection of stranded wire connections to various terminals.

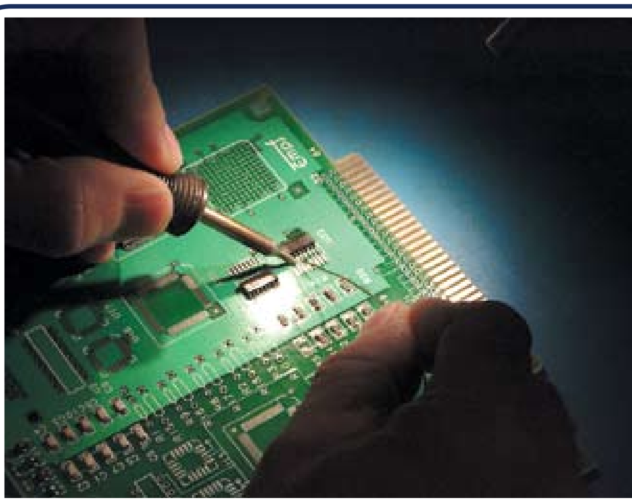
• **Module three:** Installation, soldering, and inspection of components in plated- through-holes.

• **Module four:** Mounting, soldering and inspection requirements for surface mount components.

• **Module five:** Inspection criteria of the ANSI/J-STD-001.

Students will learn the differences between the three product classes, how to interpret the requirements of the standard and become familiar with the terminology used.

Workmanship skills assessment is used with modules 2-4. The student must perform wire and component preparation and hand solder the terminations. The soldered connections have to meet class 3 requirements of the J-Std. It is also required that ½ of the soldered connections be done utilizing lead-free solder.



There is also written tests associated with each module. Module one has a open and closed book multiple choice test. The average between the two tests must be 70% or greater. The remainders of the modules each have an open book test in which the student must score greater than 70% on each.

Upon successful completion the student will receive a certificate valid for two years from the date of issue in the areas where proficiency is demonstrated. The certification is a portable credential which is issued to the individual.

If the student was previously certified to the J-STD, they have the option of either taking the recertification class or they may go thru the challenge process. The recertification class runs for 2 days. The first day is a general review of the standard highlighting the differences in the D revision. On the second day the student will perform the workmanship samples and take the written tests. The challenge process is a one day class where the student comes in and takes all the tests and then completes the workmanship samples without any technical instruction or review.

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Ask the EMPF Helpline!

A customer conducted accelerated fatigue tests of a circuit board assemble and wanted to analyze the failed components and decide whether the damage created was of the same mode (cyclic thermal fatigue) as field failures that they had already seen.

The EMPF noted some difference between the lead geometry and bend radius of the field components was apparent (Figure 1). An appreciable amount of conformal coating, however, was noted fewer than one of the components in Group "T".

Figure 1. Open and filled lead frames of components from group "J" and "T" (left and right).

Wetting of the solder up the leads was present for components from Group "T" and indicated solder profile issues. A majority of the solder had been pulled up the lead from the base of the solder joint. The lack of solder under the foot has contributed to the lack of solder joint strength and hence the failure mechanism. IPC-A-610D 8.2.5.5 only states that the target condition for maximum heel fillet height is that solder extends above the lead thickness but does not fill the upper lead bend, and also that the solder does not contact the component body. In this case, solder was present beyond the upper lead bend and had also contacted the component. This condition is not an IPC defect by definition, but can reduce reliability.

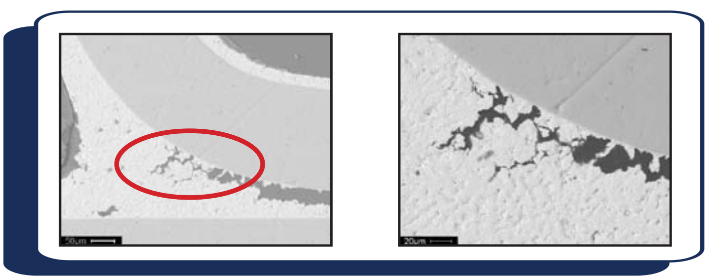

Figure 2 these are characteristics of a cyclic fracture.

Cross sections of the Group "T" solder joint showed that a solder fracture was present. It was deformed and ran through the Pb-rich matrix Figure 2. These are characteristics of a cyclic fracture. Figure 3 shows backscatter (left) and secondary electron (right) image show that the fracture was through the bulk solder and near the intermetallic of the component. The fracture appeared to have initiated at the toe of the solder joint and propagated under the lead to the heel of the solder joint. At the component interface, intermetallic measurements indicated some growth (from typical initial solder thickness of 1-1.2um) to 3.5 um. This indicated a high temperature application.

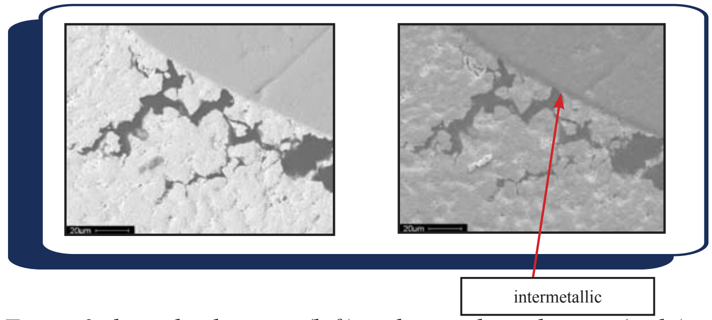

Figure 3 shows backscatter (left) and secondary electron (right)

Observations of the microstructure show that there was severe micro-voiding present in the Pb-rich regions of the solder. There was little, if any grain growth and no grain elongation. The severe micro voiding had enabled fracture initiation locations. The response of solder to cyclic loading under thermo mechanically driven environments is complex. However, above 100°C, solder decreases in strength rapidly. The combination of application temperature of 130°C and the inherent low tensile strengths has had a severe influence on the solder microstructure and joint reliability. ACI offered the following materials engineering improvements ranking in order of ease and importance.

Modification of PCB board material to higher Tg. Thermount, because of its low CTE, is expected to minimize the effects of CTE mismatch for components that are silicon (bare die) or have a large fraction of their volume (die/packaging volume ratio) as silicon. Polyimide is expected to minimize temperature effects in general because of its high T_g (glass transition temperature). Also below are relative cost increases from a standard grade FR-4.

Tetra functional FR-4	*1.0x*	*GF T_g 170°C*
Multifunctional FR-4	*1.2x*	
Thermount 85NT	*2.0x – 2.5x*	*T_g 240°C min*
Polyimide	*2.5x-3.5x*	*T_g 250°C min*

Substitution of PbSn eutectic. Replacement of solder that considers the application high temperature environment such as 95Sn 5Pb. *Board components will need to be examined to determine if they can withstand the higher soldering temperatures.*

Alloy Composition	**Melting Point**
62-Sn/36-Pb/2-Ag	*179C (355F)*
63-Sn/37-Pb	*183C (361F)*
60-Sn/40-Pb	*190C (375F)*
96.5-Sn/3.5-Ag	*221C (430F)*
95Sn/5Pb	*~240C*
10-Sn/90-Pb	*302C (575F)*

From the Help Line customers fatigue testing, Figure 2 is an SEM

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Ask the EMPF Helpline!
(contingued from page 4)

image that is an overview of solder joint showing that one of them is cracked throughout the entire lead. The fatigue test is proceeded rapidly, and at 1.5 mil peak-to-peak displacements, a sample failed at 680 cycles. The crack appears to have initiated at the toe and shows some distortion, Figure 3. There is also some compression action within the crack along the intermetallic. The compression action and distortion of the crack appear that it is beginning to conform and model the expected behavior. The bulk solder of the broken (left) and opposite (right) joint at high magnification, Figure 4., show micro porosity and a soft distorted solder. Even though there has been stress on the solder joint, there is no alignment of the grain structure. Even though there has been temperature exposure, there is no grain enlargement.

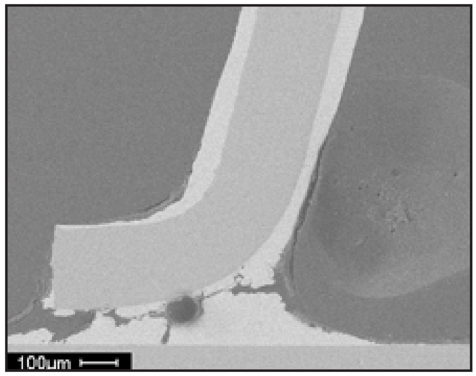

Figure 4 shows micro porosity and a distorted solder.

Comparing the microstructures of the original failed samples of Group "T" with the fatigue samples, it was observed that the latter was beginning to approximate the damage that had occurred with the failed samples. In this way, test fixture setup and displacement profiles will be determined that allow the customer to test assembly designs and increase lifetime and reliability.

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Corrosion in Electronic Hardware

Corrosion of 100k ohm resistor and ajacent wire.

Figure 1. Close up photo of arc suppressor housing and corroded resistor from field failure

An EMPF customer was experiencing corrosion of a 100k ohm resistor on a CRT socket. The initial resolution by the customer was to go with a no-clean process for attachment of the arc suppressor housing. The problem persisted, however. As a result, the EMPF proposed elemental analysis of the corrosion through Scanning Electron Microscopy with Energy Dispersive Spectroscopy (SEM/EDS). The results of the SEM/EDS analysis of a stock resistor and a corroded resistor indicated:

- The ends of the resistor were composed of tin (Sn) over copper (Cu) over iron (Fe).
- The wire leads coming out of the resistor were tin (Sn) over copper (Cu).
- The internal body of the resistor was composed of silicon (Si) and aluminum (Al).
- The potting compound was silicone based.
- The appearance of the corrosion suggested iron oxide (reddish/brown) and copper oxide or copper hydroxide (green/blue) and was confirmed to be iron (Fe) and copper (Cu) (Figure 2).
- The internal body of the resistor was composed of silicon (Si) and aluminum (Al) and the casing was composed of was silicon (Si).

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Figure 2. Optical Microscope images and SEM/EDS analysis of corrosion points

The corrosion was concluded to be the result of dissimilar metals (iron and copper) in the presence of moisture. The presence of visually detectable flux residue was not necessary to cause this type of corrosion from occurring. The moisture most likely penetrated the resistor's silicone potting compound and the corrosion began at the junction where the wire contacted the end of the resistor. The electrical failures expected from this are loss in impedances at the resistor at best and shorts at the worst. EMPF's recommendations were to take measures to assure the assemblies are kept dry and identify a component of a different composition in order to remove the potential for this failure mechanism if humidity or moisture is present during operation.

An alternate resistor was identified and replaced the steel end-capped resistor. After some period of time with the new resistor in place corrosion, failures developed once again (Figure 3).

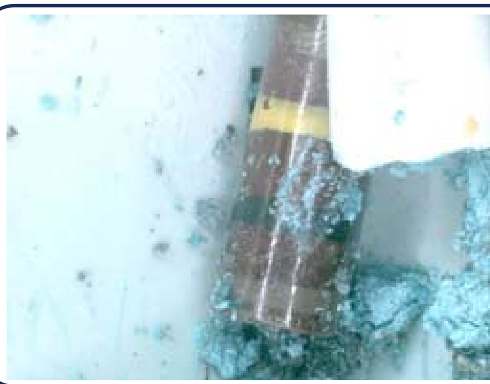

Figure 3. Photo of corroded resistor from a field failure

It was determined that a no-clean hand-soldering process was implemented. The bare board had a HASL finish which was applied with a water soluble flux. The resistor according to the customer was operating at 9.5KV and +/- 15µAmps. In addition, the assembly was not conformally coated.

As in the previous work, the assemblies were visually examined and elemental analysis of the corrosion was performed through SEM/EDS. Along with these steps, the ionic cleanliness of the raw materials, in-process and finished assemblies was determined. The results of these findings were:

- Corrosion was observed on field returns at the resistor and the through-hole leads of the housing.
- Inventories of the video amplifiers displayed white residue at the solder joints on the resistor and at the through-hole connections of the CRT socket.
- The blue-green color of the corrosion indicated it was mostly copper oxidation which was confirmed through SEM/EDS analysis *(Figure 5)*.
- The resistor body was composed of oxygen, silicon and magnesium while the lead was tin (Sn) plated copper (Cu). There was no indication of a mismatch in materials (i.e. galvanic corrosion).
- Ion chromatography (IC) analysis of a full assembly (assembly 1) indicated the presence of chloride, bromide, nitrate, sulfate and an unknown peak at 2.4 minutes and 4.5 minutes with the bromide levels and the peak at 4.5 minutes being significant *(Table 1)*.
- IC testing of a bare board indicated the presence of chloride, bromide, and a peak at 1.1 minutes. Bromide levels were above ACI's recommended limit of 5 µg/inch^2 for bare boards *(Table 1)*.
- IC testing of the resistor and a suppressor housing unit indicated trace amounts of chloride, nitrate and sulfate along with the peak at 1.1 minutes observed on the bare board *(Table 1)*.
- The arc suppressor housing unit was removed from assembly 2 and both parts analyzed separately. Prior to analysis residue was noted on the PCB surface underneath the location of the CRT socket. IC testing indicated the presence of chloride, bromide, nitrate, sulfate and the 1.1 minute peak on both the board and arc suppressor housing. The peak at 4.5 minutes observed earlier was observed only on the arc suppressor housing unit *(Table 1)*. Bromide levels on the board were above ACI's recommended limit of 15 µg/inch^2 for assemblies.

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Corrosion in Electronic Hardware
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Table 1. Ion chromatography results

Comments	Customer code	Amount of each contaminant (ug/in^2) chloride	bromide	nitrate	sulfate
Full PWA from inventory	Assembly 1 from inventory	2.9	10.5	0.6	2.2
PWA from inventory disassembled by ACI	Assembly 2 wo/heat sink & CRT	3.2	16.2	0.4	2.1
	arc suppression housing from S/N 0860	2.3	4.3	0.2	5.2
inventory parts	8 resistors	1.7	N.D.	0.1	0.9
inventory part	bare board	0.5	14.9	N.D.	N.D.
inventory part	unprocessed CRT	0.8	0.0	0.1	1.2
in-process sample	Assembly 3 prior to CRT	1.9	9.8	0.4	0.4
in-process sample	Assembly 4 prior to CRT	5.1	10.7	0.4	0.4
in-process sample	Assembly 5 prior to CRT	3.1	11.4	0.3	0.3
THT WS process done by ACI	Assembly 6 WS process for THT step wo/heat sink	2.8	4.0	0.2	0.3

N.D. refers to none detected

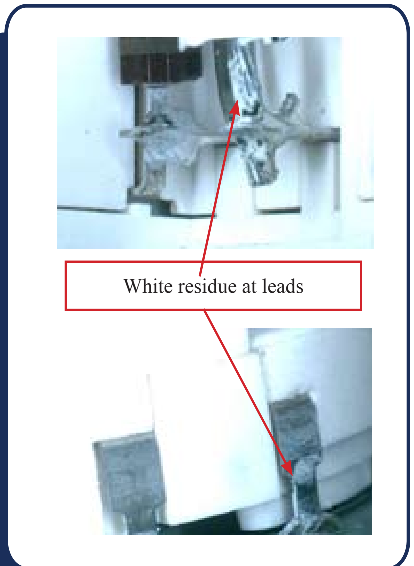

Figure 4. Microscope image of resistor and housing leads.

- Analysis of the no-clean flux used to attach the suppressor and resistor displayed chloride, nitrate and a peak at 6.5 minutes. This peak did not correlate with peaks observed after secondary soldering of the suppressor or resistor.

- Three assemblies prior to attachment of the arc suppressor housing unit and resistor were IC tested. These results indicated the presence of chloride, bromide, nitrate, sulfate and the 1.1 minute peak (Table 1). Bromide levels were excessive however.

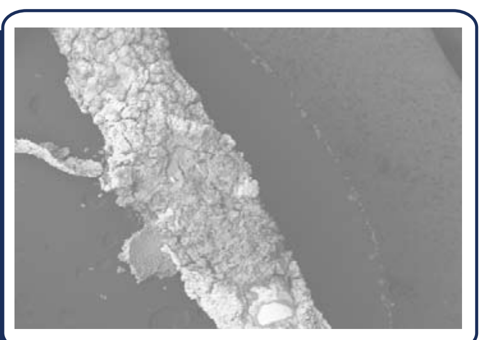

Figure 5. SEM imaging and EDS analysis of the failed resistor leads.

EMPF has generic guidelines for assemblies that are not application specific. The level of ionic residue that is acceptable for this application is unknown. Given the application and end-use environment, it was determined that a removable water soluble flux chemistry was necessary. As a result Highly Accelerated Stress Testing (HAST) was performed to asses the potential for such a process to provide adequate long term reliability. The matrix of samples involved in the HAST exposure were subjected to 168 hours of unbiased HAST at 130°C and 83%RH at 1.27 atms vapor pressure based upon MIL-PRF-38535E and JESD22-A110-B. One test board treated with the water soluble process was analyzed by ion chromatography (Assembly 6) and displayed acceptable levels of chloride, bromide, nitrate

and sulfate. The peak at 4.5 minutes observed earlier was also observed on this board but relative levels of this peak indicate it was not excessive (Table 1).

The HAST exposure did not initiate corrosion on the ACI-recommended water soluble processed assemblies

Conclusions/Recommendations:

Choice of components was initially identified as the cause of the failures. The complexity of problem was not initially clear and subsequent analysis identified ionic residue contamination from the secondary no-clean hand soldering process as a related cause given the application and end-use environment.

Bromide levels were high for the bare board which would be expected for a HASL finish as a highly active flux is utilized during the hot air solder leveling (HASL) process. However, corrosion was only observed at the leads of the CRT and resistor suggesting the bare board residue was not the key factor in these failures.

A number of unknown peaks were observed from analysis of the assemblies. In some instances these peaks were significant relative to the overall level of ionic residue observed. The major unknown peak at 4.5 or 4.8 minutes was not observed on the in-process assemblies prior to attachment of the CRT and resistor. The presence of this peak after secondary hand soldering indicates it was part of this processing step, most likely a weak organic acid from the no-clean flux.

A no-clean flux is designed to burn off during soldering removing

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Corrosion in Electronic Hardware
(continued from page 7)

surface oxides and provide a clean solderable surface with no residue or some benign residue left behind. No-clean flux chemistries historically do not solder as well as activated fluxes. As a result, hand soldering habits are to utilize more flux to get the necessary soldering conditions. This practice and the non-uniform heating of hand soldering generated the residue underneath the CRT. The presence of significant flux residue in a higher voltage application and uncontrolled end-use environment provided a situation for corrosion to occur.

Because of the application and possible end-use environments, ACI recommended utilizing a water soluble flux chemistry that can be cleaned for attachment of the CRT housing and resistor. Limited testing has demonstrated that a water soluble flux if removed properly will not induce corrosion. Application of a conformal coating was also suggested to further extend the usable lifetime of this assembly and would be able to be qualified by ACI if such an additional processing step is a prudent option from a cost/benefit standpoint.

EMPF was further tasked to provide support by doing the CRT attachment through the same water soluble hand soldering step identified during HAST exposure. The cleanliness of the assemblies is currently being determined and to date assemblies have been well below the 10.06 µg NaCl equivalent/inch^2 limit prescribed in J-STD-001. This data will be supplied to the customer and used as a baseline for further technology transfer to allow for on-site processing of assemblies by the customer or contract manufacturer if so identified.

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Manufacturer's Corner
Advanced Stencil Printer Technology

Electronic manufacturing centers face multiple challenges as they implement new processes and procedures to support lead-free manufacturing requirements. Continuous miniaturization of components coupled with inconsistent wetting behavior of lead-free solder paste has created increased concerns for stencil fabricators and manufacturers of stencil printers. Today, more than ever, stencil printers must provide accurate, repeatable deposition of solder paste, meet production thru-put requirements, and provide real-time printing and inspection solutions. Recent stencil printer technology advancements have achieved a reliable, automatic inspection process of the substrate, with the capability to auto-correct substrate mis-alignment, prior to printing. By coupling high-resolution optics to precision motors utilizing digital servo controllers with optical feedback, fiducial recognition and real-time correction to mis-aligned substrates is achieved. The high resolution optic recorder is mounted to a servo-controlled, XY gantry located above the stencil. Levels of direct and diffused intensity-controlled illumination are obtained for evaluation. This unique process acquires any shape on the substrate or stencil which can be used as a fiducial; multiple fiducial locations can be selected to further increase alignment accuracy.

Additional parameters must be recognized to achieve proper PCB solder paste printing. Excessive squeegee pressure is a known contributor to numerous print errors including solder bridges. To address this concern, some stencil printer manufacturers integrate two independent servo-controlled motor-driven print heads to provide real-time pressure measurement. Based on product process requirements, the squeegee pressure is pre-programmed via a user interface. Squeegee pressure is then monitored up to 2000 times per second and when deviations are identified, corrections to pressure are automatic thus ensuring optimal squeegee pressure. In addition to monitoring and managing squeegee pressure, each print head is equipped with an optical encoder that constantly monitors print head height, automatically implementing adjustments when required. Manufacturers of stencil printers are implementing technology-based process controls to ensure maximum yield and achieve the requirements of quality standards.

Exerra Corporation has recently announced its 2D&D™ print quality inspection system. The 2D&D™ is based on a proprietary image processing generator that enables 100% inspection of 100% of assemblies - without compromising on throughput. During each inspection cycle, the color camera rapidly scans the PCB and acquires a set of color images at a resolution of 8 microns. The images are then compared to reference images and adjusted to meet product acceptability standards. The application of a color camera enables the inspection system to analyze solder color differentiation, which if often not possible with some existing monochrome camera-based processes. The intuitive interface enables the user to define the entire PCB or

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Tech Tips...

BGA ReBalling

It may not be a sound economic decision to reball and reuse a BGA component that has a low initial cost. However, many custom ASIC's and even some "off the shelf" BGA components, because of their complexity, can be very expensive with limited availability and excessive long lead times. For these types of components it can be rather cost effective to have the ability to reuse components that have failed due to soldering defects. In this article we will discuss some considerations that must be addressed in order to successfully perform reballing of BGA components.

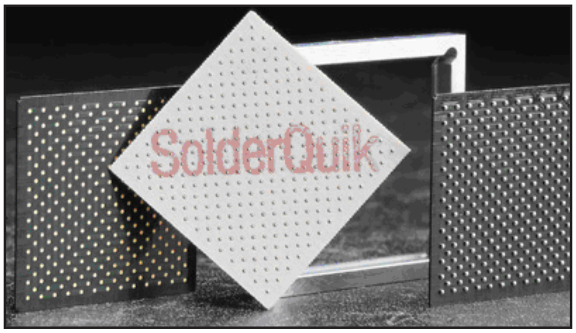

Figure 1. Solder preform material and fixture

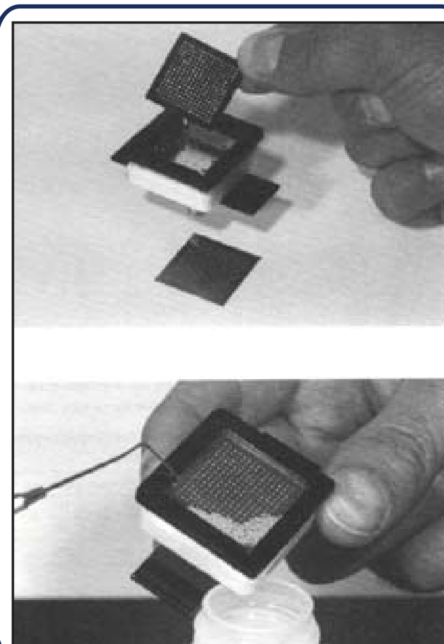

Figure 2. Solder Reballing screen and fixture

Package Specifications:
It is important to know the component package specifications before attempting a reballing process. These specifications include maximum thermal limits for the component materials, alloy type (either eutectic or high temperature), ball size, moisture sensitivity level, and most importantly the manufacturer's recommendations for the maximum number of reflow cycles the component can withstand. This information can be obtained from the component data sheets or directly from the component manufacturer.

Component Substrate Preparation:
Before attaching the new component interconnects the component substrate must be carefully prepped by removing all remaining residual solder. The most efficient method is to use solder braid and a wide blade soldering iron tip. The use of flux during this process will increase the effectiveness of the solder braid in wicking the residual solder from the component substrate. Care must be taken to avoid "scrubbing" the substrate surface with the solder braid and iron tip during this process, which can increase the risk of component substrate damage. Once all of the residual solder has been removed from the component substrate, it should be thoroughly cleaned using isopropanol alcohol (IPA) to remove any remaining flux residues. The component substrate should then be inspected for any evidence of component substrate damage.

Reballing Process Options For Eutectic Interconnects:
Once the component has been properly prepared for attachment of the new interconnects (balls), a process for accomplishing this task must be selected. The three main options available when reballing with eutectic balls are the preform method, the screen method, or a relatively new method based on the screen method which employs a vacuum pick-up for holding the alloy spheres in place. The screen method requires the application of water-soluble tacky flux and a specialized fixture where individual solder balls are placed over the corresponding component substrate land pattern. Once all of the lands have a new ball in place, the entire fixture is sent through the reflow process to melt the solder balls onto the component. An alternate method is to use solder preforms in conjunction with a simple frame sized to match the outside dimensions of the component. This method has proven more efficient and reliable than the screen method. The solder ball preforms are available in literally thousands of package configurations and are very easy to use. The preform consists of precisely spaced balls sandwiched between a lamination of cardboard that has been impregnated with a water-soluble flux. Simply apply a water-soluble tacky flux to the component substrate, place the preform onto the component and then place the component into the frame. Next, reflow the component in the frame to melt the solder balls onto the component substrate. Once the solder preform balls have wetted to the component substrate and resolidified the cardboard can simply be peeled away from the component and cleaned using DI water. This method, although more efficient, does require a bake out cycle of the reballed components for approximately 24 hours prior to placement of the components onto an assembly.

Reballing Options For High Temperature Interconnects:
When attaching high temperature interconnects to a component the only viable option is to first screen solder paste onto the component substrate

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✂ cut here and save!

Manufacturer's Corner

Advanced Stencil Printer Technology (cont. from page 8)

select "areas of interest" as required. Each "area of interest" is presented as an icon on a graphical representation of the PCB, and can be magnified for close-up inspection. Each type of defect is displayed on the screen in a unique color, making it easy to identify various types of problems, when identified. The frequency and level of inspection is user-defined and can be executed after every printing and stencil cleaning cycle. The inspection system generates both statistical and graphical reports, featuring automated alerts when measurements exceed defined tolerances.

Figure 1: Exerra ep-33

The Exerra ep-33 features an automated stencil aperture inspection process to ensure that apertures are free of clogged paste. As in the printing inspection, the user can define whether to inspect the entire stencil or only selected areas of interest (for example, fine-pitch components). The results of the stencil inspection can be set to trigger automatic or manual stencil cleaning. The In Process Stencil Cleaner (IPC™) operates simultaneously as the stencil shuttle retracts, ensuring maximum throughput. The stencil cleaner offers both dry and wet wiping, or can be programmed for a combination of both. For wet cleaning, the solvent is evenly distributed on the surface of the cleaning paper with a unique spraying mechanism. The amount of solvent used and the rolling speed can be pre-programmed by the operator. The paper used in each cleaning cycle is also constantly monitored. The Exerra ep-33 utilizes a flexible and easy to set-up print nest with magnetic support pins and bars for underside support. Boards are held firmly in place during the print cycle by pressure-adjustable side clamps, which guarantee reproducible printing; optional vacuum system and dedicated work-holders are also available. The Exerra ep-33 features a clearly structured and intuitive, mouse-driven user interface that simplifies operation and drastically reduces training times. Utilities and parameters are logically displayed on the screen, enabling quick access and extremely fast programming. Unused functions can be switched off to prevent any unauthorized process changes, and all levels can be locked, ensuring that stable processes cannot be changed.

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Tech Tips... BGA ReBalling

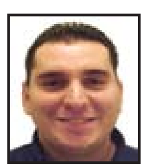
(continued from page 9)

using a solder paste stencil and then placing the high temperature preform into the screened solder paste. The use of a split vision rework station helps in alignment of the preform to the component. The thermal profile requirements for reflow are also more critical when working with high temperature interconnects as opposed to eutectic. It is critical that the thermal profile be of sufficient heat to fully reflow the eutectic solder paste without reflowing the high temperature interconnect and remain within the maximum component temperature rating.

Cleaning per flux chemistry:

The cleaning process of the reballed component will depend upon the type of flux chemistry used during the reballing process. If using a no-clean or rosin based flux chemistry, isopropanol alcohol will do a very good job of removing flux residue. When using the solder preform method, which requires the use of water-soluble flux, cleaning in DI water is necessary. Because of possible water absorption by the component during the DI water cleaning process, it is necessary to preform an additional process step of a bake-out cycle of the component prior to use. The recommended bake-out for standard PBGA packages is 24 hours at 125 degrees Celsius. Other component configurations may have different recommendations, which can be obtained from the component data sheet. When properly performed, the reuse of BGA components is possible and can be very cost effective. Understanding and adherence to the component and process specifications is critical to success of reballing a BGA.

With experience, reballing and reuse of BGA components can be achieved rather easily. The EMPF offers a two-day curriculum on BGA processing and rework which covers all aspects of BGA reballing methods. If you would like additional information please contact the EMPF helpline at 610-362-1320 or log onto the EMPF website at empf.org.



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R&D: Advanced Development using Architecture Standards

Globalization of the electronics manufacturing industry has provided consumers a low cost high volume product pipeline. Open architecture standards for hardware and software have matured along with design and simulation platforms resulting in a toolbox approach for systems development. Almost every major semiconductor corporation offers systems developer's access to pre written software for their open architecture devices. Designers have the luxury of using verified code, which are governed by third party committees or standards organizations. The open standards ensure interoperability between multiple hardware vendors. Consequently, developers go quickly from concept to product with a high probability of success on the first try.

The USB interface standard is a good example of an open standard protocol, which created a plethora of companies who brought products to market in less than 6 months. With the open standard for both hardware and software (plug and play) inserting a USB compliant device into a computer having a USB receptacle guarantees that the computer will be able to interrogate the device and set up a connection enabling other applications and hardware no matter who made the device. Microprocessor device manufacturers, driven by Moore's law to ever-smaller gate sizes have been enabled by the transistor race to offer cost effective integrated families of logic blocks with specific functionality. Today any number of combinations of DSP cores, communications protocol cores, and microprocessor cores are available. The ease of use gained by open standards, coupled with integration at the silicon level, and has spawned fierce competition between semiconductor corporations for board space on consumer products. Each new generation of device will have increased functionality, higher operating speeds; operate at lower voltages, or all three. The open architecture software standards and toolbox approach to hardware development have allowed for tremendous gains in time to market, functionality, and multiple protocol devices. Moore's Law has driven device designers to develop new generations of devices to coincide with each new fabrication process node or face declining market share based on cost or functionality. An unforeseen result of the relentless drive for ever-smaller devices is consumer product life cycles are now 12-18 months. This runs contrary to military systems, where serviceable lifetimes are measured in decades. The good news is that with open standards in place, many legacy systems can be re-engineered to fit in the given space and perform as planned with greater reliability and less weight. Nevertheless, just tossing a board over the fence for re-engineering it to accept a new processor may not be the only aspect to consider. Today, the EMPF and ACI's Center of excellence stand at the ready to engage upstream with designers, and engineers, and downstream with end users to facilitate designs which drive legacy systems to a modular, extendable and field serviceable platform that can deliver performance, new functionality, and ruggedness. The following applications demonstrate the importance of upstream engagement and open system architectures.

Design Scenario One

In a program sustainment, application for the AN/ARS-6(V) personal locator system (PLS) ACI was tasked to upgrade the radio functionality using COTS parts, and open architecture while sustaining the service life of the AN/ASR-6(V) transmitter receiver unit , control display unit, and remote display unit.. The original PLS unit used conduction cooling while many of the replacement sustainment COTS components were designed for forced convection cooing. The system display had to meet an additional requirement of being viewable by persons wearing night vision goggles. The redesigned unit must pass functional testing, accepting data from GPS (global positioning satellites) and SARSAT (Civilian Satellite based search and rescue) waveforms and be compatible with the newer CSEL survival handheld radio, which would be provided by a separate vendor in module form. The original PLS contained two ASICs (Application Specific Integrated Circuits) which provided the basic functionality and used the Distance Measuring Equipment (DME) waveform for location. In this case, the ASIC's we no longer available without re-design and the additional functionality required would need to be incorporated into the operating system. ACI engineers examined the systems and decided that the best way to provide functionality, and be sustainable in the future would be by the incorporation of a Field Programmable Gate Array (FPGA). The FPGA eliminated the original ASIC devices, and need to develop new hardware for the other functions. The FPGA could be set up to run in any of the required modes, and since all of the protocols were open standards, the firmware implementations were straightforward. This made the overall finished product smaller than its predecessor did. The FPGA would be easier to shield and the resulting system is currently undergoing Airworthiness Certification.

Design Scenario Two

A system design engineer is tasked with adding a card interface socket that enables wireless communications. Open architecture is available for many protocols including PCMCIA, PCI, Mini PCI, USB and SDIO. Each of the listed types was created primarily to make a physically smaller card to address the commercial desire for smaller, less expensive devices. Most offer Bluetooth™, 802.11, and Ethernet protocol. The system designer must weigh the pros and cons of his applications expected service life, and how long each of the successively larger open architecture platforms will be serviceable.

Conclusions

In order for military systems designers to exploit the open standards and produce field serviceable, supportable and rugged systems, designers will need to anticipate allowing for more than one interface/communications standard in their boards. New designs should support multiple protocols, and use modular design techniques. By adopting modular designs, many systems will be able to share common module designs. This enables field serviceability, and re-use, driving ownership costs down. Open Architectures allow for rapid design cycles and multiple protocols to exist in a given product. The planners of products and systems, either new or re-engineered must work upstream with engineers, and designers to deliver systems downstream, which the harness and exploit the ability to quickly modify the performance, capability, and specific functionality offered by modular design concepts.

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EMLC Upcoming Course Schedule 2006 & 2007

Skills

BGA Manufacturing, Inspection & Rework
January 29-30
March 28-29
April 3-4

Chip Scale Manufacturing
February 20-22

Electronics Manufacturing

Boot Camp A
January 29 - February 2
April 16-20

Boot Camp B
February 5-9
April 23-27

IPC member

Certifications

IPC J-STD-001 Instructor Certification
January 8-12
February 12-16
March 12-16

J-STD-001 Instructor Recertification
January 10-11
February 21-22
April 26-27

IPC-A-610 Instructor Certification
January 22-26
February 26 - March 2

IPC-A-610 Instructor Recertification
January 17-18
February 19-20

WHMA-A-620 Wire Harness Manufacturing (Operator)
March 13-15

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January 3-5

IPC-A-600 Instructor Recertification
January 31 - February 2
February 28 - March 2

IPC Challenge
January 17
April 25

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February 12-16

IPC-7711/7721 CIT Recertification
April 4-5

IPC-7721 Certified IPC Specialist (CIS) Circuit Repair
January 18-19

IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCB's
May 1-4

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April 2-3

Failure Analysis and Reliability Testing
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March 6-8

For more information, please call (610) 362-1320 or email: registrar@empf.org

For a complete course schedule, visit:
www.empf.org/html/empfasis/emlc upcoming.pdf

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