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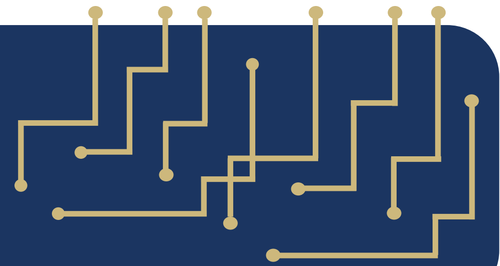

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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government center and laboratories in the U.S.

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Affordable Antenna Technology

TThe U.S. Navy continuously seeks to deploy new technology in order to increase the mission capabilities of surface ships and submarines. Shipboard electronic systems must support multiple mission scenarios. This includes intelligence gathering, reconnaissance, mine hunting, interdiction of enemy ships, as well as the transport of personnel. Integration of emerging wireless technology, such as network-centric warfare and precision weaponry, will enable successful execution of these diverse service requirements.

Modern warships feature multiple communications systems that are tailored for a particular mission. Achieving reliable operation of a wireless system that co-exists with other radio frequency (RF) platforms is a substantial design challenge. Comprehensive planning is required to determine the optimal locations for the multiple antennas mounted on a warship. Deploying the same communications systems across multiple vessels is complicated because the available space for mounting the antennas is not same on each warship. Recognizing the need to address a gap in antenna technology, the U.S. Navy has tasked the EMPF, along with its industry partners, to research new multifunctional capabilities for antennas in small or combined form factors. As a result, a new research program has been created to develop Flexible Antenna System Technology Insertion.

Figure 1-1 Concept Drawing

To establish the research goal, antenna count, placement of the antenna arrays, and the functional capabilities of each communications system utilized on the warships were considered. Requirements of the new system were also determined by this analysis. A flexible, multi-use antenna platform must be reconfigurable, as it will be utilized to counter anti-access threats. With the present technology, multiple antennas are required to implement the complete communications solution. Installation of multiple antennas would clutter the mast of the warship. In addition, co-location of antennas tends to cause interference problems and coupling between the transmitting and/or receiving elements. This can degrade the operation and integrity of the communications/radar/intelligence systems.

The EMPF has established the following goals for the Flexible Antenna System Technology Insertion research project:

- Assessment of operational requirements for the new antenna and capture of systems requirements.

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NAVY MANTECH manufacturing technology program

Affordable Antenna Technology
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- Antenna technology investigation – review commercial off the shelf (COTS) and state-of-the-industry military antennas in addition to contemporary antenna technology research.

- Correlation of technology to the new ship acquisition requirements.

The EMPF strategy includes a partnership with leading technology providers in the defense industry. The EMPF will work with companies that have significant experience in the design of antennas, radio systems and ancillary equipment for maritime, terrestrial, and airborne platforms. The EMPF program will also incorporate the knowledge gained by companies that have contributed to the development of advanced, compact, multiuse antenna farms. As a result of this cooperation, a block diagram of proposed techniques for integration of the requirements and the associated technologies was developed. Co-site issues (potential interference between closely spaced antennas) and a mitigation plan, were also identified. Specific emphasis was placed on exploiting the current state-of-the industry in HF, VHF, and UHF technology. Recent COTS antenna technologies were identified, including ultra wideband (UWB). A correlation of the antenna technology and the new shipboard requirements resulted in multiple recommendations and approaches that were then narrowed down to a final approach, set of construction materials, and superstructure design for optimization.

The Goals for the Flexible and Affordable Antenna System are:

- Leverage the EMPF and industry partner findings to develop prototypes of critical hardware components such as antennas, filters, couplers and active cancellers to reduce the required number of antennas needed to support adaptable mission requirements.
- Define a standard interface for Navy shipboard communications equipment to allow compatibility with the new ship radio suite concept and proposed antenna solution.
- Design a single mast system and ship kit for integration into the ship along with the required documentation.

The findings from initial studies showed that no single specialized antenna met all requirements. For the remainder of this initiative, the technical approach will be to investigate current state of the art antennas and specifications (i.e. return loss, frequency response, bandwidth, gain, radiation pattern, max available power gain, and antenna-to-antenna isolation) that were collected in the initial studies. While the recommendations made in the initial studies were general in applicability due to the proprietary and competition-sensitive status of the new ship designs, the activities in the remainder of the initiative will follow these general recommendations to the specific dimensional and materials details for the selected sea frame concept.

The program will develop methods for reducing the antenna farm's physical outline. A computer model of the baseline antenna system will be constructed and simulations conducted on up to two candidate concepts. By leveraging the EMPF's industry partners capabilities, a prototype package will be developed and designed with a requirement to be survivable in a surface/marine environment. The proof-of concept Antenna System Prototype will then be designed and verified electrically. Functional tests will also be performed on the "electrical" prototype (with a near mechanical form factor) over a section of the 3 MHz – 2 GHz band.

As part of the review and refinement process of the initial study recommendations, requirements analyses (using data from the selected sea frame builder and systems engineering to refine the systems architecture) will be performed. A market survey will be conducted in order to define other Navy qualified antennas as potential candidates for a stacked (extremely affordable, multi-use) architecture. The resulting table of candidates will be

Figure 1-2 Antenna Array Concept

compared to the baseline design and evaluated on whether they meet the minimum RF requirements and maximize cost benefit. This chart of required performance as a function of cost will be invaluable for the required wideband operation from the HF to L-band.

Modeling and system level simulation will play a key role in determining the expected effectiveness of the antenna and digital pre-distortion system. The modeling will include analysis to

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Design for Manufacturability and Assembly

The application of DFMA principles in the manufacturing and assembly of printed wiring boards can manifest in the form of reduced cost and assembly time. It is important to start defining the critical process path during the design stages of the PWB, to avoid potential manufacturing problems encountered during the course of assembly. As an example cited in a previous issue of the Empfasis, the transitions from a Eutectic Tin/Lead to a Lead-Free soldering process is a prime example of the value of a DFMA undertaking.

The list below represents the manufacturing process of a mixed technology PCB with through-hole components on one side, and SMT devices on both sides of the PCB. The insertion of a lead-free paste can change the soldering operations sufficiently to warrant a close examination of the options available in avoiding manufacturing pitfalls. At each interval in the process, there are procedural considerations to be taken into account as part of a DFMA system to define a critical path.

Board prep
- *Substrate cleaning process*
- *Board surface finishes impact wetting of the solder paste onto the pads of the PWB. This is especially true for Lead-Free solders*
- *Board drying for hydroscopic materials. Be aware that the thermal exposure as a result of the solder change will increase vapor pressure*

Stencil print primary side
- *Limitations in pitch*
- *Correct aspect ratio – should be > 1.5 for good paste release*
- *Geometry of stencil apertures*

SMT placement primary side
- *Automated or manual placement*
- *Consider the residence time of the solder paste prior to reflow. It may change versus conventional Sn/Pb paste.*

SMT reflow
- *Reflow ovens. Are they suitable to achieve specified profiles? The risk factor in using a 5 zone oven versus a 10 zone oven for the higher temperature profiles, may warrant the procurement of the higher zone oven.*

Assembly cleaning
- *May be necessary at this stage*
- *Additional drying may be needed for moisture sensitive components*

Dispense adhesive on second side
- *In some cases this may be avoided, depending on the process. If the process used is simply two-sided SMT, smaller devices (< 4 gm/cm^2), allow the surface tension of the solder to hold the component in place.*
- *An alternate PTH solder application may allow the exclusion of the adhesive step*
- *If you use an adhesive, choose one suitable for the higher wave solder temperatures.*

Application of solder paste (alternate to adhesive)
- *Reflow secondary side solder paste or cure adhesive*
- *Be aware of the primary side components. The size of the SMT component will determine the feasibility of secondary reflow process; i.e. adding additional adhesive re-enforcement.*

Secondary assembly cleaning
- *This may be warranted with additional drying to offset entrapped moisture prior to subsequent soldering*

DIPS and axial insertion
- *Consider the lead finish for lead-free soldering application*
- *The MRT rating may have changed due to higher temperature exposure*
- *As always, orientation of the components should be considered*
- *For a limited amount of through hole components, consider truncating the leads to apply an SMT process*

Wave soldering
- *For smaller volumes of PTH, strongly consider a selective soldering approach, which allows more flexibility in design, and localizes the exposure of the board to the through-hole components*
- *Consider the profile changes needed to accommodate the lead-free alloys, including the type and method of fluxing.*

Final assembly cleaning
- *Do not mix no–clean fluxes with other flux types that call for mild cleaning. No-cleans require aggressive cleaning when the application warrants it.*

The range of options and consideration for the mixed technology assembly process will more than likely exceed those that have been listed for this article, and will vary from operation to operation. An extensive examination of each assembly and sub-assembly step will help extract where the cost and time savings can occur. Once the specifics of the assembly process are sorted, it is beneficial to take a broader view of each alternate path.

Table 2-1 shows slight deviations among the three process sequences for the assembly of a mixed technology PWB. The first column indicates a "typical" process flow discussed earlier, as part of the extraction exercise to define options and considerations. The middle column shows a red highlighted cell that substitutes a selective soldering system option for the wave soldering step. This substitution allows SMT reflow for both sides of the assembly in lieu of the adhesive paste on the secondary side. This can occur because the entire assembly is not subjected to the heat of the solder wave, which can potentially cause movement of the SMT devices. Another potential approach, as illustrated in the third column, is to shorten the DIP and axial leads, and incorporate a solder paste in the plated vias where

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Ask the EMPF Helpline!

A customer contacted the EMPF Helpline concerning a solder wetting problem that was observed during a lead-free, SMT wave soldering process with a gold plated PCB.

A customer contacted the EMPF helpline concerning a solder wetting problem that was observed during a lead-free, SMT wave soldering process with a gold plated PCB.

Test Methods:
The EMPF was tasked with assessing the solderability of the board. Samples provided by the customer were stored in a nitrogen box prior to quantitative solderability testing (Wetting Balance testing). This test measures the time to reach the maximum wetting force and is a routine test the EMPF performs.

First, appropriate pads were identified and removed from the board by sectioning. Then, the pads were fluxed and tested in the KWB-1000 Wetting Balance per the parameters listed in table 3-1. Any residue flux was removed with IPA (isopropyl alcohol) before final inspection.

Parameter description	Specific value/type	Parameter description	Specific value/type
Pre-test specimen cleaning	None	Pre-heat, sec	20
Flux type	RMA 185 (ROL1)	Test duration, seconds	5
	Purple flux Organo flux 3355 (ORH1)	Height above solder surface at start of test, mm	10
Flux application, seconds	Dip, 3-5	Immersion angle, degrees	90
Solder	63/37 tin/lead alloy solder	Immersion/Extraction speed, mm/sec	5
Solder test receptacle	Bath	Immersion depth, mm	1
Solder temperature, °C	235		

Table 3-1 Wetting Balance Parameters

The wettable perimeter and cross-sectional area were determined for each sample. This information, along with the immersion distance, was used to calculate the volume and maximum theoretical wetting force based upon the formula shown below. The final units are normalized based upon the wettable perimeter and reported in terms of µN/mm.

F max. theor. = t P cos(α) – (d V g)

Fmax theor = maximum theoretical wetting force, µN/mm
V = volume, mm3
t = surface tension of the solder, (0.4 joules/m2)
g = gravitational constant, (9.81 m/s2)
P = wettable perimeter in mm
α = wetting angle (assumed to be 0
d = density of 63/37 eutectic tin/lead solder at 245ºC, (8110 kg/m3) degrees for perfect wetting)

Acceptable solderability can be established through evaluation of wetting balance curve properties: wetting time, wetting force and general shape of the curve (See Figure 3-1). J-STD-003A provides suggested evaluation criteria based upon these properties. This suggested criteria has been established as a two tier evaluation format with Set A being more stringent. Components meeting Set A suggested criteria are applicable to a larger soldering process window than components meeting Set B suggested criteria.

Results:
The pads tested did not meet Set A, but did meet Set B evaluation criteria. Wetting was slow with significant wetting forces occurring much later in the test with the standard RMA flux and ROL1 flux activity (Trials 1205 and 1206, Table 3-2 and Figure 3-1). Wetting was positive with the wetting forces at five seconds greater than those observed at two seconds. (i.e. F5>F2 as prescribed in Set B evaluation criteria). Visual wetting was acceptable. Analysis of a pad with a highly active water soluble flux (ORH1 flux activity) improved numerical wetting with results meeting both Set A and Set B evaluation criteria (Trial 1207 in Table 3-2 and Figure 3-1).

* F(max at 50%) is 159.6 µN/mm for the PCB pads examined.
F¬2 is wetting force at 2 seconds from start of test.

					Acceptance criteria					
					Set A			Set B		
Sample	Trial#	T_0	F_2	F_5	$T_0 \leq 1sec$	$F_2 >/= F_{(max)}$ µN/mm	$F_5 >/= F_{(max)}$ µN/mm	$T_0 \leq 2sec$	$F_{1<2} > 0$	$F_5 >/= F_2$
pad 1	1205	1.65	58.1	294.19	fail	fail	pass	pass	pass	pass
pad 2	1206	1.63	65.725	290.32	fail	fail	pass	pass	pass	pass
pad 3	1207	0.57	482.41	488.98	pass	pass	pass	pass	pass	pass

Table 3-2 Summary results of wetting balance testing

To is time to buoyancy corrected zero (cross-over time) F5 is wetting force at 5 seconds from start of test.

The PCB samples displayed marginal wetting as established by the evaluation

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Design for Manufacturability and Assembly (continued from page 3)

Process 1	Process 2	Process 3
Board Prep	Board Prep	Board Prep
Stencil Print	Stencil Print	Stencil Print
SMT Placement	Primary SMT Placement	Primary SMT Placement
SMT Reflow	SMT Reflow	SMT Reflow
Assembly Clean	Secondary SMT Placement	Secondary SMT Placement
Adhesive dispense	SMT reflow	DIPS & Axial's Truncated for reflow
Adhesive cure	DIPS & Axial's	SMT reflow
Assembly clean	Selective Soldering	Assembly Clean
DIPS and Axial's	Assembly Clean	
Wave soldering		
Final Assembly Cleaning		

Table 2-1 Mixed Technology Process Paths

the through-hole devices will be mounted. This can be done concurrently when the solder paste is applied on the secondary side for the SMT devices. The through-hole components can be placed manually on SMT assemblies that have a limited number of PTH devices, not necessarily requiring automated insertion equipment. The entire assembly can be reflowed, thus eliminating the need for applying a wave solder to the PTH components.

Regardless of the manufacturing process, there are benefits that can be derived in utilizing the DFMA principles in the area of cost savings, and product delivery. For more information on training courses, please check our website http://www.empf.org and click on training.

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Design For Manufacturability

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High G Packaging

Precision Guided Munitions (PGMs) incorporate an active guidance system within the munition to meet increasingly stringent mission requirements for lethality and collateral damage. This active guidance system relies on highly miniaturized electronics modules. PGMs require the development of packaging techniques that allow electronics modules to withstand the high-g forces encountered during a gun launch. Honeywell's deeply integrated Inertial Navigation System – Global Positioning System with Anti-Jam capability (INS-GPS/AJ) product has been baselined as the primary production of navigation, flight control, and mission computer for a major DoD weapons program. Figure 4-1 shows a typical Inertial Measurement Unit (IMU) that is offered by Honeywell and the basic assembly components and printed wiring boards of an IMU. The newer generation IMUs are more compact, lighter and offer better performance. Currently, a Navy funded program is targeting the packaging aspect of newer generation IMUs.

A previous high-g packaging program, supported by the Office of Naval Research (ONR) and the Program Executive Office for Integrated Warfare Systems (PEO-IWS), focused on improving the manufacturing technology and supply base for MEMS-based IMUs for use in precision guided munitions. This program developed guidelines that increase the capability for the Navy to address high-g electronics packaging issues. Failures that occur during large scale qualification can be very costly from both an economic and a scheduling perspective. This risk can be mitigated by the use of inexpensive tests to screen components for survivability. A preliminary screening methodology was demonstrated in this program. This methodology could be employed not only to evaluate the high-g performance of an alternate MEMS accelerometer under investigation in this program, but is also applicable to evaluating electronics packaging and materials for future Navy high-g applications. The guidelines identify the packaging characteristics that are

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Affordable Antenna Technology
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quantify the performance and interference aspects of the digital pre-distortion algorithms in the RF environment. A co-site simulation analysis will then be done to establish parameters that define the utility of the proposed approach supporting the condensed antenna farm. SIMULINK® will be used to model the digital pre-distortion algorithm and the receive-analog cancellation algorithm. This model-based design platform will allow multi-domain simulation of dynamic systems in an interactive graphical environment.

The development program allocates time for prototype testing of critical system components. This includes the selection of antennas to perform mutual coupling tests based on system requirements. The spiral development approach will be adopted to incrementally build up to the most performance-based design. Testing of the prototype will take place and mutual coupling data will be generated. Various options for pre-distortion and receive cancellers will be assessed along with digital sub-band filtering.

Mechanical design analysis will be performed to determine survivability of the antenna in a combat environment. The mechanical characteristics of the system, such as stress, will be evaluated. Particular attention will be focused on low life cycle cost, and the use of open standard interfaces and COTS components where applicable. As a result of the analysis, the system is expected to demonstrate compliance with the E3, SWaP, and shipboard environmental requirements.

After development of the prototype, electrical tests will be performed on the critical components to simulate the actual operation to the extent required to prove concept feasibility and determine the system performance. Mutual coupling, digital pre-distortion, receiver cancellation, and digital sub-band cancellations options will be developed, modeled, and tested. During the whole development process, systems engineering activities will be conducted, which include requirements management, system design, systems integration and testing, and systems simulation and modeling.

Other relevant activities during the Flexible Antenna System Technology Insertion program are:

- Above Deck Antenna Integration – development of an RF penetrable shroud and RF bulkhead mountable antenna interface plate, ready configured for ship or test bed mounting.
- Below Deck Electronics Integration – development of an environmentally conditioned COTS rack containing the digital pre-distortion electronics, RF switches, and control hardware in a single mast solution.
- Transition Demonstration and Implementation – development and demonstration of a single mast system designed for a stealthy, space-optimized ship.

The US Navy's expectation for the flexible antenna system technologies is extensive and demanding. With the development of the new, affordable ship acquisition program, space conservation through the reduction of antenna count is a definite and necessary requirement. At the same time, the reduced antenna count must be multi-functional to compensate for the additional antennas that are no longer present. Therefore, the importance of the Flexible Antenna System initiative is paramount to the Navy to maintain current maritime dominance and effective joint operations.

REFERENCE

1. Walsh, Ed. The Next Step for Shipboard Electronics, Military & Aerospace Electronics. March 2006
2. Address by George W. Bush given at the U.S. Naval Academy, May 25, 2001

Author: Ravi Patil, Design Engineer

Soldering Skills Kits

J-STD 001 Certification
J-STD 0014 Recertification
IPC 7711/7721 Certification
IPC 7711/7721 Recertification
Lead Free Certification Kit
HDI Materials Qualification

Available online at www.aciusa.org/products

Packaging Affordability

Electronics packaging and assembly typically involve the use of many vendors within a support chain. They provide wafer sort, wafer dice, die packaging, package sealing and final testing. This business is very competitive, and pricing based on high volumes provides an economy of scale that enables the purchase of dedicated process equipment for each step in the sequence.

Prototyping operations for products that have high volume initial runs can find a packaging house. However, if initial volumes are small (1,000 pieces) it becomes very difficult to find an assembly house willing to package parts in a timely fashion. DoD electronics manufacturers need access to a low volume, dedicated prototyping house that is capable of designing and delivering moderate quantities of assembled packages utilizing design rules and materials sets, which can be transitioned to high volume manufacturing lines.

The EMPF's Power-Packaging Lab was set up to address the needs of moderate volume producers in direct support of Navy power packaging needs. The lab is capable of designing and delivering prototype quantities of packaged devices, and systems utilizing a wide variety of packaging options, and assembly methods. A list of assembly capabilities appears below:

- Eutectic die attach under an inert atmosphere to 350° C.
- Epoxy die attach
- Flip chip attach with solder reflow and underfill
- Flip chip attach with conductive epoxy dots
- Thermo-compression gold bump bonding
- Dam and fill or glob top encapsulation
- SMD placement capability using 0201 size passives
- Aluminum wedge bonding using wire from 4-20 mils in diameter
- Gold wedge bonding using wire from 2-4 mils in diameter
- Gold wedge bump capability (2 mils minimum today)
- Hermetic seal capability to 9x9 inch package size

Complimentary to the assembly capability are the package types and system level products that can be processed through the lab. Package and system level types are listed below:

- Ceramic Ball Grid Array (CBGA) all body sizes
- Ceramic hermetic packages all styles, all body sizes
- Single and multi-die laminate packages in Land Grid Array (LGA) and Ball Grid Array (BGA)
- System in package (laminate, ceramic, hermetic)
- Card Edge connector laminate systems (PCI, Mini PCI, SDIO, and others)
- Package on Package

The trend of electronic devices becoming smaller, which results in higher heat loads/unit area and lower maximum allowable junction temperatures is straining the capability of standard packages. Therefore the package selection process can no longer wait until the device is designed and the silicon is fabricated. Early engagement between the device designers and the packaging house must take place before the device is fabricated. Failure to do this can lead to many unfortunate issues including the following:

- Joule heating of die level flip chip solder bumps in high performance microcontroller packages resulting in an unacceptably low Mean Time Before Failure (MTBF)
- Poor electrical performance because the package design did not adequately address high frequency operation issues

Many package styles and lead options are available that mitigate thermal, mechanical, and electrical issues. Some packages were developed with a specific device in mind. For example, TO-220 package styles are commonly used for moderate voltage and current power transistors. As the package complexity increases, early engagement of the device designers with the packaging providers is necessary to ensure that the package selected meets the thermal, electrical, and mechanical requirements of the device and its intended use environment. Prototype package fabrication becomes essential to rapid product development. Packaging options can include multiple dies, or multiple dies and passive components. Figure 5-1 shows a System in Package (SiP) application. The Power-Packaging Lab is capable of designing and providing single die packages, multi-chip modules, and System in Package solutions.

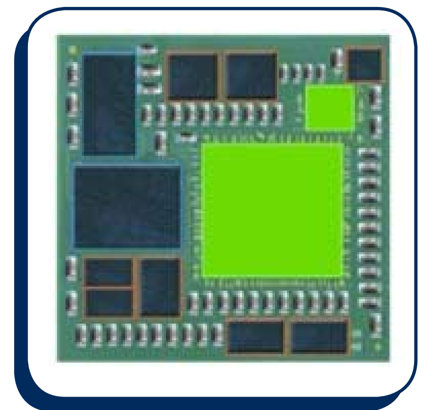

Figure 5-1 Image of a System in Package, green and black areas are where dies are placed. Passive components are soldered to the laminate package. Photo courtesy of Stats ChipPac

When combined with environmental and electrical testing, the EMPF can ensure that the chosen packaging solution passes the reliability requirements for the intended end use. Moreover, with ties to commercial packaging houses, the EMPF can utilize the design rules and materials sets of large packaging houses to ensure a smooth transition to a Higher Volume packaging contractor. Commercial linkages with an eye toward high reliability packaging provides the Navy significant potential improvement in affordability.

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High G Packaging
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conducive to high-g survivability.

These guidelines were based on both a literature search as well as a Design of Experiments (DOE) study. This DOE used a 20,000g screening drop test to demonstrate survivability of test vehicles that were designed with consideration of orientation, substrate material, component geometry, restraining materials such as underfills and encapsulants, and assembly fixturing. The screening DOE was generated using the JMP statistical program from the SAS Institute that utilizes algorithms based on providing the optimized design space for a given number of runs.

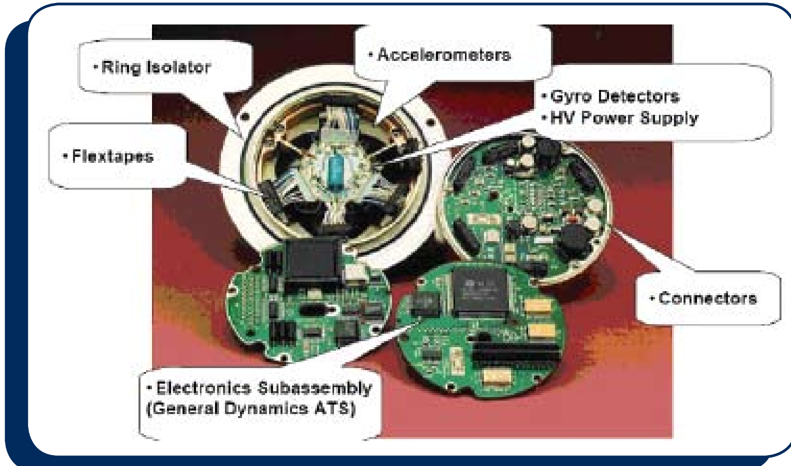

Figure 4-1 A typical IMU (Honeywell HG1700) showing the major components and circuit boards. (photo courtesy of Honeywell).

As initially proposed, this DOE incorporated studying the effects of factors such as the component type, component size, and orientation on the board, board substrate material, encapsulant, and underfill materials. These factors were chosen on the basis of testing samples launched by an air gun assembly that simulated the force, rotational movement, and durational time of actual projectile systems. Figure 4-2 shows a typical shock pulse used in this study. By design, the shock tester can simulate 20,000g acceleration with very short pulse duration. The final report of this program includes the information of more than 30 electronic packaging failure modes that occurred at various stages of high-g shock tests. It also includes information about the commonly used high-g shock tests, and the laboratories and groups that offer high-g testing and modeling services.

Currently, leveraging the US Army's investments in the Common Guidance IMU, Navy ManTech has been collaborating with Army program offices and developed a program "High-g Packaging and Miniaturization of Electronics for Deeply Integrated Inertial Guidance Units". This program will study the packaging of the BG1930G and similar products from the point of view of assessing its survivability to different gun launch environments, as well as suggesting improvements to the design. Another aspect of this program is the application of System on a Chip (SoC) technology to the discrete semiconductor approach used in the BG-1930G. The SoC approach is to combine the mission processor, inertial sensor assembly interface, and several other electronics functions onto a single substrate. Development and incorporation of SoC technology will effectively eliminate an entire printed wiring board from the product baseline. It will also enable the achievement of aggressive average unit production pricing objectives, producibility, reliability, weight, and volume objectives mandated by other Joint Navy/USAF program applications and a specific Army application.

As mentioned earlier, this program will be built on the BG-1930 Deeply Integrated Guidance and Navigation Unit that Honeywell Aerospace has developed under other Army contracts. Under this ManTech effort, the Mission Processor Board will be converted into a SoC using multi-chip packaging technology to meet a less than 300 mm2 form factor. A multi-chip module package that combines the BG-1930 mission processor, field-programmable gate array (FPGA) and corresponding electronics functions on a single substrate, along with RAM and flash memory into a package will be developed in this program. The major tasks in this program include: package concept design, package design implementation, SoC design integration, timing analysis of the design, prototype fabrication, high-g testing, and system integration. This program also includes a MEMS sensor evaluation, a high-g packaging materials evaluation, and static and dynamic high-g shock modeling. The high-g testing

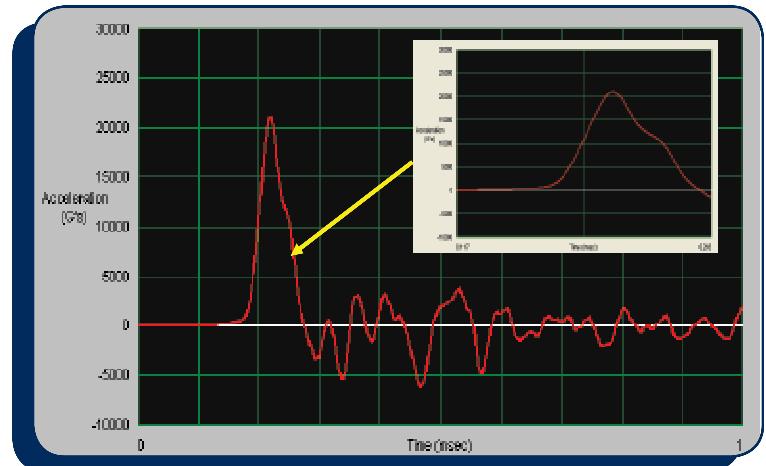

Figure 4-2 Typical Shock Pulse

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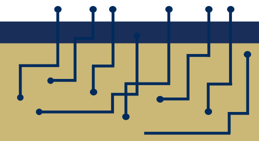
Tech Tips...

X-ray Systems



X-ray systems provide the capability to look inside opaque/solid substances. Many of today's microfocus x-ray system manufacturers offer either open-tube or sealed-tube technologies. A sealed-tube x-ray source is generally sealed in a glass tube containing a vacuum (analogous to a light bulb). An open-tube source is generally all-metal and maintains a vacuum with a two-stage pumping process.

To determine which type of system is required, several fundamentals must be considered: detail detectability, tube voltage, geometric/total magnification, cost of ownership, and system investment.

Detail Detectability - Also known as feature recognition, detail detectability is the ability to resolve the smallest feature. It can be estimated as approximately half focal-spot size of the X-ray source. Thus, the smaller the focal-spot size, the sharper the image at high geometric magnification. In general, most open tube systems will have a smaller focal spot size than sealed tubes and therefore a sharper image.

Tube Voltage - The voltage requirement depends on the sample. The greater the sample thickness, density, and mass, the higher the voltage needed to penetrate. The tube current controls the quantity of x-ray photons (flux) that is generated. The higher the current, the lower the noise levels allowing a higher contrast view. Since focal-spot size is directly proportional to power (voltage × current), the tube current is typically smaller at higher tube voltages to maintain image sharpness. Low-density samples typically require higher current and lower voltage. Maximum voltages for sealed tube X-ray sources generally range from 80 kV to 150 kV while open-tube systems vary from 100 kV to 225 kV.

Geometric and Total Magnification - Understanding the distinction between geometric and total magnification capabilities is essential. Geometric magnification is the actual magnification with no enhancement. Total magnification is the geometric magnification plus magnification enhancement tools such as digital zooming and software. Total magnification takes into account the optical characteristics of the detector and size of the display monitor. The larger the geometric magnification, the smaller the feature size that can be observed.

This is defined as:

$$M_{geo} = FID / FOD$$

where: FID is the Focus-to-Intensifier Distance, and FOD is the Focus-to-Object Distance.

Open tubes have a minimal focus-to-object distance and are best suited for applications demanding high magnification. Sealed tubes have a larger FOD resulting in a lower achievable geometric magnification. Because of this, open-tube systems provide a more complete package, yielding a higher level of electronic analysis capabilities including BGAs, flip-chip bumps, package inspection, and a wider range of failure analysis.

Cost of Ownership - The up-front costs of open-tube systems are generally higher due to added support systems such as the vacuum pumps and a more complex x-ray control. However, both technologies have their associated costs. Since all major components of open-tube systems may be exchanged, virtually unlimited tube life can be achieved. This is at the expense of a required scheduled maintenance program and consumables such as filaments, targets, and seals. Sealed-tube systems require minimal maintenance but eventually need a tube replacement.

System Investment - Ultimately, the system selected must meet the current needs as well as future applications. It also must allow flexibility when new technologies enter the market. Since image quality is essential, actual samples should be submitted to each of the qualified vendors for imaging comparisons. After determining which systems provide the best quality, go step by step through the features, further narrowing the list. Then, request a hands-on demonstration of each vendor's recommended configurations. Testing a system yourself will tell how well a system is going to fit the application and facility needs.

Author: Joe Kelly, Technician/Instructor

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Manufacturer's Corner
Dage X-Ray: Popcorning

The term 'popcorning', within the electronic manufacturing industry, is often defined as a catastrophic failure created by the presence of moisture within a component. Common 'popcorning' will occur when a small amount of moisture is heated during the wave solder/reflow process and turns to steam. As electronic manufacturing service providers transition to lead-free processes which require higher reflow temperatures, the potential for 'popcorning' increases substantially. Less common and more difficult to trace 'popcorning' occurs during test or power-up of the circuit board as the failure may be intermittent. When 'popcorning' occurs, regardless of the contributing conditions, the component damage is internal and may not be recognized by visual inspection procedures.

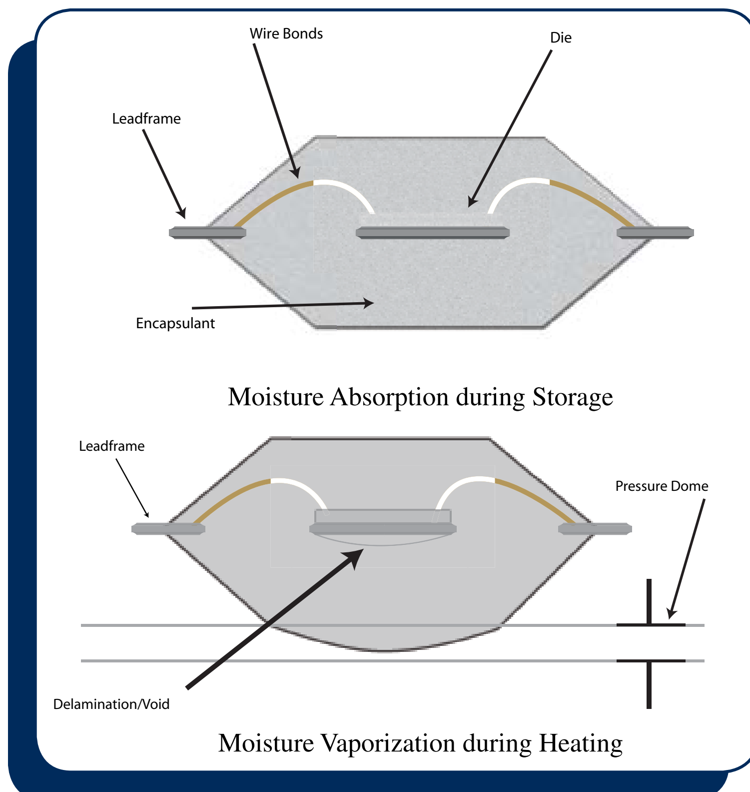

Figure 6-1: Mechanisms of Popcorning

X-Ray inspection permits a non-destructive inspection of components and presents a clear image of the component internal construction. However, cracks in the die are difficult to see since silicon is transparent to x-rays and provides little density or contrasting differences. A common method of identifying 'popcorning' is to x-ray the solder joints of the device; as the moisture within expands, the package swells and a high force is applied to the component leads and subsequent solder joints. The gull-wing leads of a QFP package, as an example, will distort from the internal expansion of the molding compound, forcing mis-alignment of the leads and disruption of the soldering joints during the reflow process.

X-ray inspection of the solder joints will readily discover a potential intermittent failure caused by 'popcorning'. Component leads may lift out of the paste during reflow yet remain in contact when the board cools. When the board is tested or when power is applied, the component and substrate will expand, creating an open circuit. Conditions of 'popcorning' may occur during repair and re-work of circuit board assemblies as any device will be at risk to 'popcorning' if it was not properly handled and stored. X-ray inspection of re-work and circuit board repairs should be implemented as a normal course of inspection and quality assurance with special attention to BGA package types. The 'popcorning' of BGA's is often recognized during the x-ray inspection process with the appearance of a bridge-like appearance. This physical distortion, caused by the internal expansion of the package during reflow, deforms the molten solder balls underneath. When the solder paste becomes liquid, the distorted solder balls will bridge with other solder balls.

The x-ray inspection of BGA solder balls is best accomplished with an oblique angle view as the difference in solder ball diameter between inner and outer balls is very clear and distinct. X-ray equipment offering solder ball measuring and solder ball comparison provides the best opportunity for the operator to identify conditions of 'popcorning'.

BGAs as with many other components, will continue to be at risk as industry migrates to lead-free materials and processes. To mitigate such issues, industry must recognize, develop and implement new measures within the manufacturing environment to prevent components from absorbing moisture. Many manufacturing centers have implemented a pre-bake process of the board substrate to reduce moisture. Additional information and recommendations for pre-baking can be obtained by contacting the Helpline at helpline@empf.org or telephone 610-362-1320.

For additional information on the above article or to schedule a demonstration of the Dage X-Ray equipment located at the EMPF, contact Robert N. Berta, 610-362-1200 ext 253 or via e-mail at rberta@aciusa.org.

Author: Robert Berta, Business Development Representative

High G Packaging
(continued from page 8)

includes a board level centrifuge and shock plate testing. In addition, Ballistic Rail Gun testing will be conducted with both non-functional units and functional SoC units.

This program is managed by the EMPF with Honeywell International as the major sub-contractor. Penn State Applied Research Laboratory, US Army Picatinny Arsenal, and the PEO-IWS are also members of the program team.

Author: Charlene Yao, Senior Materials Engineer

Ask the EMPF Helpline
(continued from page 4)

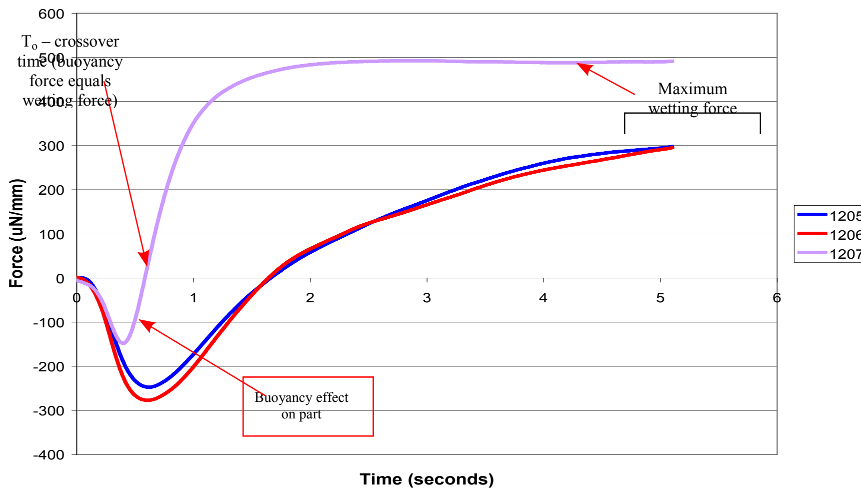

Figure 3-3 Wetting balance curves of tested pads

The EMPF recommends further wetting balance testing to confirm the observations. In order to determine a root cause, EMPF recommends analysis of the surface of the PCB by Scanning Electron Microscopy with Energy Dispersive Spectroscopy (SEM/EDS) and Auger Spectroscopy. X-ray Fluorescence Spectroscopy (XRF) is also recommended to confirm plating composition and thickness. Micro-sectional analysis with subsequent SEM/EDS analysis of failed assemblies is also recommended.

criteria within J-STD-003A. Wetting was slow when the standard RMA flux was utilized. Visually, the pads wet with the given standard activity flux (ROL1). Improved results were obtained with a more active water soluble flux (activity ORH1), suggesting an oxide or similar hard-to-remove tarnish was present, hindering wetting.

Conclusions/Recommendations:
The results were obtained with a eutectic Sn63/Pb37 solder and mildly activated rosin based flux. These results indicate that these PCBs may not be appropriate for a process which is not as forgiving as the one which had been used by the customer. As a result, a less active flux and/or lead free process may provide less than marginal results.

Author: Bill Riter, Digital Design Engineer.

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