

American Competitiveness Institute

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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government center and laboratories in the U.S.

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Wide Band Gap Semiconductors for Power Electronics

The high temperature operation and power handling capabilities make silicon carbide (SiC), a wide band gap (WBG) semiconductor, the material of choice for the production of power switching devices. For a long time the defense industry has been interested in the use of SiC technology for high power applications such as the all electric ship, high power weapon systems, the hybrid

compact, lighter, and more efficient, so they are ideal for high-voltage power electronic applications. These desirable device improvements will also substantially trim the power loss in electric motor drive power conversion applications. In addition, SiC high temperature electronic sensors such as Schottky Diodes, PIN diodes, IGBTs, and JFETs are used in automotive, under the hood applications. These are similar

to the high reliability requirements of many military applications. Such high power, high frequency and high temperature applications are the ideal uses for these SiC devices. The development of Gallium Nitride (GaN) Schottky diodes has recently been reported with comparable performance to SiC diodes.

One of the largest potential commercial applications for SiC Schottky rectifiers in the near future is in the continuous conduction mode (CCM) power factor correction (PFC) circuit. The performance improvements

include higher switching speed and lower switching loss. For example, in a test case power converter, replacing the best available 600 V Si diodes with a 1500 V SiC diode,

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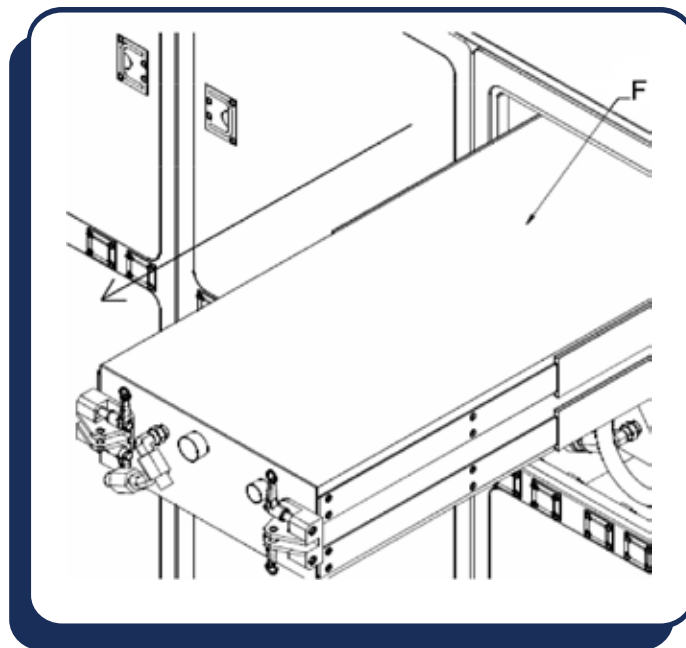


Figure 1-1: IFTP System modular power system building block (courtesy of DRS Technologies, Inc.)

electric vehicle, and highly electric aircraft. Power electronics converter systems with SiC-based power semiconductor switching devices are more

Wide Band Gap Semiconductors for Power Electronics (Continued from page 1)

results in an increase of power supply efficiency from 82% to 88% for switching at 186 kHz, and a reduction in EMI emissions¹. SiC Schottky diodes have been considered as replacements for silicon PIN diodes in many high-frequency motor drive applications. Just about any consumer or industrial electric motor in the world requires a power electronic drive — a drive that can be made smaller and more efficient with the use of WBG devices. However, WBG technology must become less expensive and more readily available, perhaps in the next five years, before it can compete in the commercial industry of motors and motor drivers.

For DoD applications, adopting advanced technologies for shipboard power electronic systems has become the focal point in the planning, designing, and manufacturing of next generation all electric vessels such as DDG1000 for the US Navy. DDG1000 requires power control, distribution and Integrated Power System (IPS) power conversion at multi-MW levels. IPS combines the power generation for propulsion and for shipboard services into a single unified electrical system, which provides a flexible architecture that makes propulsion power available to the other users such as the weapon systems and radar systems on the ship. The power conversion modules (PCM-1, 2, and 4) for use in the Integrated Fight Through Power (IFTP) of the IPS certainly would benefit from WBG technology. Figure 1-1 shows one of building blocks in IFTP system. A PCM-4 consists of a transformer and rectifier to convert 3-phase, 60 Hz AC power from the propulsion bus to DC power. The Ship Service Conversion Modules (SSCMs) in PCM-1 convert a higher DC input to a lower DC voltage output. PCM-2 contains DC-AC inverters (Ship Service Inverter Modules “SSIMs”) with a required rating in the megawatts range. Si IGBT modules with a 100 kw power rating are currently used.

A recent EMPF study using P-Spice modeling software compared the performance of a Si IGBT module and a SiC VJFET. In a test circuit similar to a power conversion module PCM sub-system, the saturation current and voltage, transient time, and power dissipation were compared. The modeling results reveal a great improvement in most cases when SiC devices replace Si devices. For example, use of a SiC VJFET instead of a Si IGBT in this test circuit has improved the power dissipation by a factor of 25x. The SiC VJFET switches much faster than Si IGBT because the transient time for SiC VJFET is over 200 times shorter than the transient time for the Si IGBT. In this study, the parameters of Si IGBT are based on a Eupec product and the parameters of SiC VJFET are obtained from SiCED, A Siemens Company. Figure

1-2 is an image of a SiC VJFET device. It consists of more than 2000 individual transistor cells on a SiC chip.

Overall, the implementation of SiC devices in high power systems

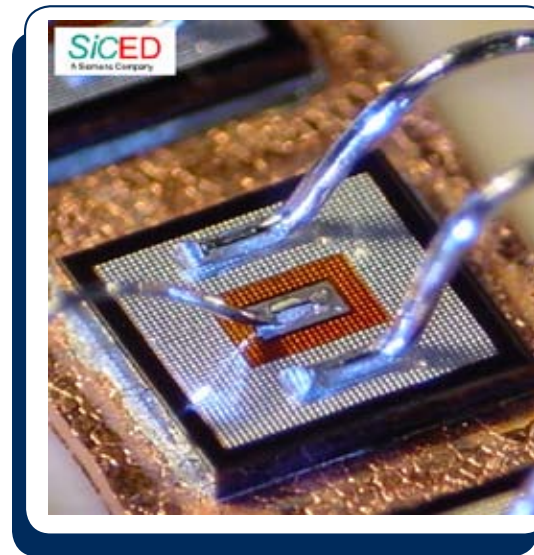


Figure 1-2: Image of SiC VJFET (Courtesy of SiCED, a Siemens Company)

is expected to significantly improve the system performance, reduce the system size, and reduce the power loss which can potentially lower the overall system cost. The challenges of implementing SiC device technology are lack of high quality of materials and

lack of suitable high temperature packages. The wide band gap semiconductor industry has been working aggressively to improve the quality of the materials. Over the past decade, device fabrication processes and device reliability have made impressive advances. The US government has also made sizable investments to advance WBG technology. Presently, SiC Schottky diodes are commercially available from a few companies, and SiC MOSFETs and JFETs have been demonstrated and are expected to advance even further in the next few years.



Charlene Yao - Charlene is an Engineer at ACI. Comments or questions pertaining to this article can be sent to cyao@aciusa.org

¹ Hefner, A.R., Jr.; Singh, R.; Jih-Sheg Lai; Berning, D.W.; Bouche, S.; Chapuy, C., SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications. IEEE Transactions on Power Electronics - March 01, 2001

EMTC: Boot Camp B

Boot Camp B, the second component of our comprehensive manufacturing training, provides students an opportunity to participate hands on in many of the processes used in electronic manufacturing. The lectures presented are coupled with lab exercises designed to allow students to operate process equipment. The week is finalized with a build of a double sided, mixed technology printed circuit assembly in which students participate in the programming, set up, operating and troubleshooting of process equipment. The skills and knowledge attained from the 2 weeks of Boot Camp enables students to demonstrate a working knowledge of electronics manufacturing processes in their work environment. It is recommended that students attend week A before proceeding with week B.

During the reflow and thermal profiling portion, students will acquire the knowledge and skill necessary to set up and operate a solder reflow process. In the hands-on segment, students will run real-time profiles using a thermal reflow profiler.

The wave soldering module allows students to apply theoretical and analytical skills essential for the efficient performance of wave soldering. These skills paired with hands-on troubleshooting and programming provide students with in-depth knowledge of the wave soldering process used for through-hole soldering.

An entire day is dedicated to hand soldering and rework of electronic assemblies. Students will manually assemble and solder a mixed technology assembly. Emphasis is placed on component tinning, lead preparation, and hand soldering techniques using a variety of hand tools and soldering equipment. Students will perform rework processes to remove a variety of through hole and surface mount components utilizing a variety of rework soldering tools. The acceptance criteria of the IPC-A-610 specification, the process control guideline of the IPC J-STD-001 specification and the rework procedures of IPC7711 are reinforced during these exercises.

Students will gain an understanding of the various types of conformal coating used in electronic manufacturing and the commonly used methods of application. Other topics covered include inspection criteria, removal techniques, identification methods, properties of various coatings, and a review of industry specifications. During the lab exercise, students will examine various conformally coated boards utilizing a black light.

The cleaning module covers the various methods used for

cleaning electronic assemblies including Solvent/Co-solvent, Semi-Aqueous, Emulsion and Plasma Cleaning Processes. Students will also have the opportunity to try out various types of equipment as part of the lab exercise.

The Cleanliness Testing segment introduces students to the commonly used testing equipment utilized for optimum process control. Lab time includes cleanliness testing of assemblies using bulk ionic testing and advanced techniques such as ion chromatography.

Students are exposed to some of the key characteristics of producing reliable boards through the Reliability Module. This module introduces some of the causes for poor circuit reliability including solder joint fatigue, voiding, and coefficient of thermal expansion. Students are also familiarized with some reliability test equipment and test methods, this promotes a comprehensive understanding of how environmental conditions affect circuit board performance.

The two hour Lead-Free module is a condensed version of our popular two day course. The course examines the current state of lead-free legislation and the upcoming requirements for compliance. Changes in the wave soldering, reflow, printing, inspection, rework, and cleaning processes that are required to convert to lead-free are important, so these topics are also presented. The conversion to lead-free soldering may also mean a change in surface finishes for boards and component leads. The benefits and disadvantages of these surface finish changes are compared in order to help students make informed decisions about their product. The lead-free demonstration includes a microscopic examination of tin-whiskers in the laboratory.



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Ask the EMPF Helpline!

A customer called into the EMPF Helpline with a problem shorting of a dual die transistor between pins 1 and 2 and between pins 4 and 5

The customer observed shorting of a dual die transistor between pins 1 and 2 and between pins 4 and 5, (source and gate on both die, Figure 2-1). Shorts between pins 1 and 6 and pins 2 and 6 were present (source and drain and gate and drain on die 1). The drains are located at pins 3 and 6.

Test Methods:

The failed transistor was provided by the customer and removed from the assembly along with a tape section of good components. The pin to pin I-V characteristics for the failed and good transistor were confirmed with a curve tracer. The good and failed transistors were soldered upside down (based upon the components wire bonding which was bottom side, refer to Figure 2-1) onto HASL coated copper coupons. They were then decapsulated using a controlled combination of fuming nitric and fuming sulfuric acid. The decapsulated components were examined optically and by SEM to determine evidence of the failure mode and mechanism.

Results:

- Based upon the component circuit diagram (technical data sheets), the substrate is tied to the source lead.
- Based upon the X-ray imaging, the wire bonds were oriented from underneath (Figure 2-1).
- Curve tracer analysis indicated a short between the gate and source, drain and gate, and source and gate on Die #1. Die #2 showed a short between source and gate and drain and gate. Drain and source curves for die 2 appeared typical.
- The drains, gates and sources are identified in Figure 2-2.
- Residual degraded encapsulant was present after extensive decapsulating steps indicating the material in this area was taken past its Tg (glass transition temperature), which is evidence of a thermal excursion (Figures 2-3 and 2-4).

- It was difficult to determine the presence of a specific failure mechanism (i.e. flash-over) because of the degraded residual encapsulant. However, die #1 does appear to be stressed based upon the cracked or wishbone appearance in the insulator layer areas where the degraded encapsulant resided (Figures 2-5 and 2-6).

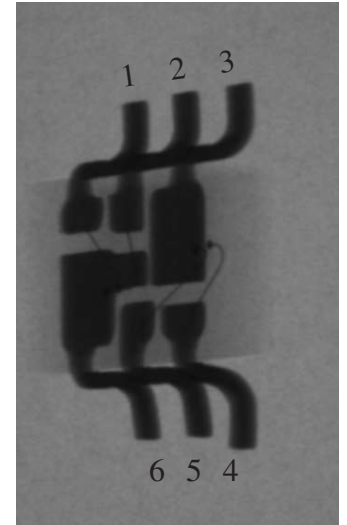


Figure 2-1: Oblique angle x-ray image of good part indicating a typical wire bonding

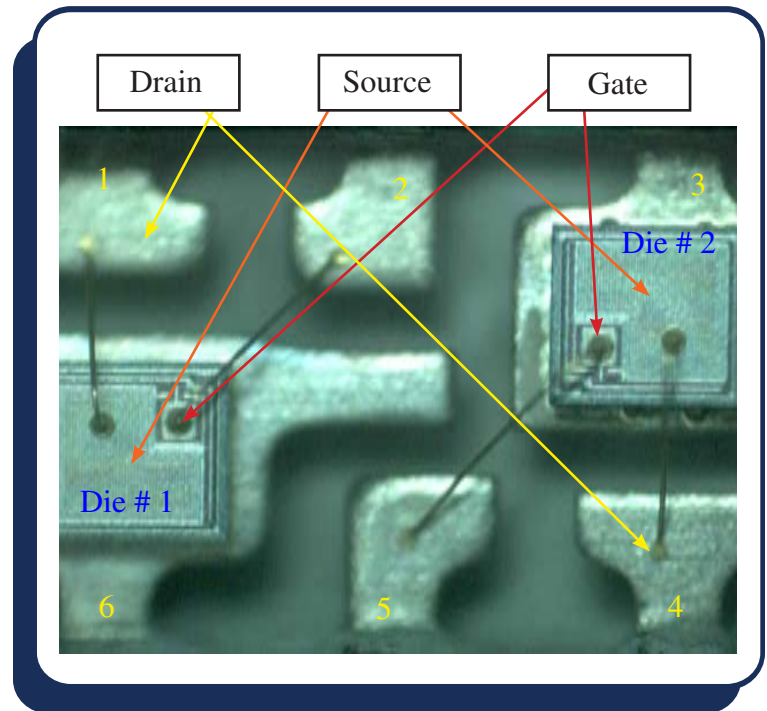


Figure 2-2: Metallographic microscope image of good transistor after decapsulation

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Ask the EMPF Helpline!

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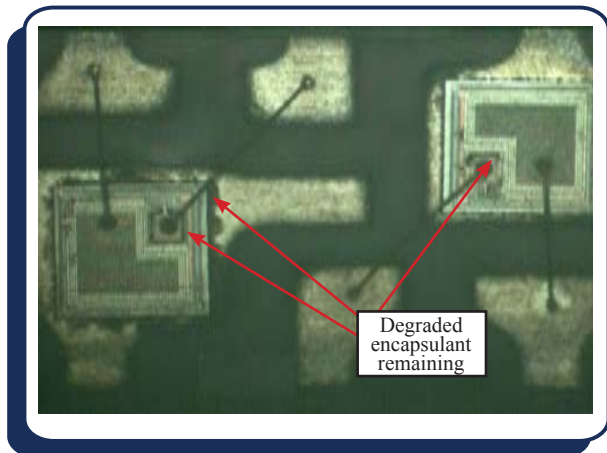


Figure 2-3: Metallographic microscope image of failed transistor after decapsulation

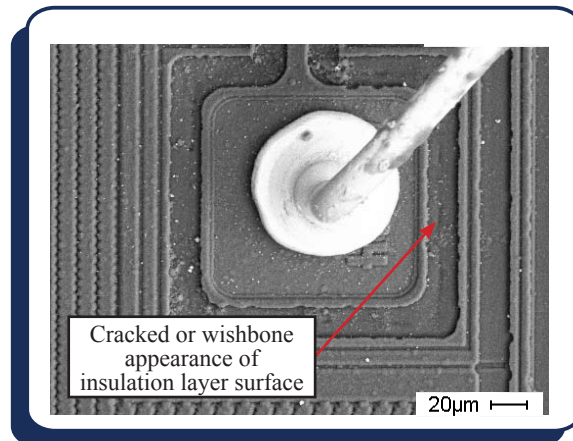


Figure 2-6: SEM image of die 1 at 450X

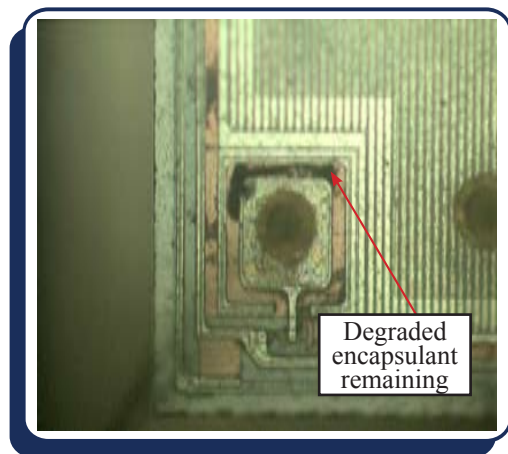


Figure 2-4: Metallographic microscope image of die 2 from failed transistor after decapsulation

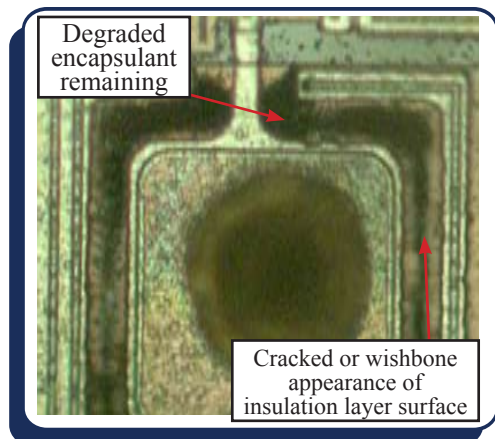


Figure 2-5: Close up metallographic microscope image of die 1 from the failed transistor after decapsulation

Conclusions/Recommendations:

The shorts observed on the transistors are the result of an electrical overstress (EOS), most likely an over current scenario as indicated by the damage observed on the failed transistor. The cause of the EOS could be from a number of the following:

1. Use of the component outside of its recommended specifications.
2. No current limiting was designed into the circuit board to prevent a circuit load from damaging the assembly.
3. Transient voltages in the circuit that could cause short durations of currents above specifications.

The degradation of the encapsulant suggests an overcurrent scenario, over some extended period of time.

As part of failure mode analysis, the EMPF recommended examining the circuit application for possible sources of over voltage and over current. In addition, a review of the specification requirements/limits for the transistor in this circuit was also recommended.



Sam Pepe - Sam is a Chemist at ACI. Comments or questions pertaining to this article can be sent to pepes@aciusa.org

Power Electronics Packaging Lab

Future surface ships will place extreme demands on power electronic systems. Power electronic component packaging used in many current and future power modules will require precise manufacturing processes to meet these tough operational demands. The objective of this project is to help meet these demands by creating a resident capability for packaging and testing power electronic devices for US Navy systems. This capability will specifically address the materials and assembly techniques used in power modules and high power RF device packages. The EMPF will design the Lab, procure the proper assembly and test equipment, and qualify the Lab's ability to create high performance, high reliability power electronic devices. The new power electronics assembly and packaging laboratory at the EMPF will help the US Navy obtain manufacturing capabilities needed to take advantage of the full potential of emerging advanced power electronics technologies.

The use of reliable power electronics is critical to future DDG 1000 and other future surface ship platforms. Furthermore, several demands will be placed on future power systems used in US Navy ship programs. Specifically, the following issues must be addressed when considering insertion of new technologies into advanced all-electric ship platforms.

- Power electronics used in advanced ship platforms must provide higher current density, switch at higher frequencies, and operate at higher temperatures.
- Power electronics packages available today are not designed or built to meet environmental and operational demands.
- The risks associated with inserting advanced devices on board future DDG 1000 and other future surface ships must be mitigated.
- Power electronic systems must be reliable, maintainable, and supportable.
- New technologies must be thoroughly tested and failures anticipated prior to implementation.
- Advanced power devices must be applied to power systems used in future surface ship platforms.

The power electronics assembly and packaging laboratory will analyze, repackage, and test advanced semiconductor electronics. The COE will also provide a source for the development of packaging materials for technologies such as wide band gap and advanced semiconductor devices. This development and testing

will be essential to aid and shorten the development cycle for future DDG 1000 and other advanced surface ships.

The Lab will house an impressive range of equipment and capabilities as listed in Table 3-1. This equipment set gives the power packaging lab the capability to produce a wide variety of prototype packaging options from hermetic single and multi-chip packages to System in Package (SiP) on laminate, ceramic, glass, AlSiC, CuSiC and other substrate materials.

The advanced cold plate development station offers rapid analysis of novel cold plate designs. Together with the simulation capability, the EMPF will be able to tune its thermal modeling based on real data, ultimately fostering a highly accurate

Equipment	Description	Special Capability
Datacon 2200 apm	Assembly, Die Bonding and Dispensing	Hot stage for eutectic die bonding to 350° C
Orthodyne 3600 wire bonder	5-20 mil Aluminum wire bonds	Built in wire pull capability ensures robust setup
Polaris Venus IV Hermetic Seam Sealer	Complete with bake out chamber, glove box and microprocessor control. Sets and makes MIL-883 welds	Square, rectangular or circular packages to 5.5 inches; Fixtures to 9 inches
Royce 580 shear Tester	Die shear, Bond shear, wire pull test capability	From 0.5g to 10kg range
APS GF-B-HT Reflow Oven	Table top high temp inert atmosphere reflow oven (Forming gas or nitrogen)	Topside view port allows for observations during reflow
Temtronics 315A Hot chuck and Suss Model 5 Prober	Hot chuck system for Suss Prober allows for wafer, die and packaging testing at temperatures up to 200° C	Ramped, programmable cooling and heating on the 315A hot chuck
Advanced Cold Plate Station	Integrated cold plate test station. Chilled water, or unique liquids. Basic design allows for drop in of novel cold plate designs test with thermal loads or evaluation of real devices on cold plate designs	Multiple temperature monitoring locations and thermal simulation using ALGOR
Hitachi S3400 SEM	SEM can examine samples without gold or conductive coatings	EDAX and Back scattering detector

Table 3-1: Equipment, descriptions, and special capability

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Power Electronics Packaging Lab (continued from page 6)

simulation model. This will reduce development cost and quicken discovery of better thermal management solutions.

The combination of best in class packaging equipment, thermal simulation, thermal measurement capability, and device level diagnostics are the foundations upon which future systems for power, RF, and advanced packaging technology will advance rapidly.



Dean Kossives - Dean is an Engineer at ACI. Comments or questions pertaining to this article can be sent to dkossives@aciusa.org

Electronics Manufacturing Training Center
BOOT CAMP

Boot Camp A:
April 16-20
June 4-8

Boot Camp B:
April 23-27
June 11-15

Contact the EMPF registrar at registrar@empf.org
or call (610) 362-1295

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IPS for the DDG 1000

The EMPF is currently working on a project sponsored by NAVSEA titled “Advanced R&D for Navy Integrated Power Systems (IPS)” that focuses on a series of advanced power electronics hardware devices. These devices are being evaluated for their performance to determine the effectiveness of these new technologies for direct use in high power Navy applications. To evaluate these new advanced technologies, the project is broken down into three major subtasks: fiber optic and advanced sensors, wide band gap (WBG) devices, and advanced heat exchangers. These new advanced technologies have the potential to increase system reliability, increase power densities and improve system performance monitoring. The objective is to validate these alternative technologies in suitable demonstration vehicles capable of providing typical IPS environmental extremes. Upon demonstrating the effectiveness of these technologies versus the current standard, The EMPF will assist with the implementation of these technologies within the Navy DDG 1000 IPS systems.

Task 1: Fiber Optic Sensors

Current sensor technologies are incapable of providing the depth of data necessary for today’s advanced power electronics. Fiber optic and advanced sensors presently available offer several advantages over conventional sensors:

- Higher Accuracy
- Higher Resolution
- Higher Sensitivity
- Lighter Weight
- Smaller Size

Fiber Optic Sensors (FOS) are immune to Electromagnetic Interference (EMI) and can operate in hazardous environments such as temperatures as high as 300°C, or pressures to 20,000 psi. Moreover, a single fiber sensor can operate in dual use, measuring both temperature and pressure.

The objective of the FOS task is to develop a conceptual design of a fiber optic and advanced sensor system (FOSS) utilizing these technologies to more accurately and reliably monitor the health and status of the onboard electric power systems. The EMPF is currently evaluating a number of advanced FOS and Radio Frequency (RF) sensor technologies. These have been installed in DDG1000 switchgear at the Land Based Test Site (LBTS) located at the Naval Surface Warfare Center (NSWC) – Philadelphia. After taking data to assess the benefits of specific placement and establish that the sensors present no increased hazards to existing systems, the sensors will undergo adverse condition testing.

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IPS for the DDG 1000

(continued from page 7)

By lowering alarm threshold levels, the repeated ability to observe and record sensor alarms will be established. The operational thresholds will be determined by exceeding operational limits in a controlled and monitored environment.

In addition, these sensor outputs will be tied into the Integrated Condition Assessment System (ICAS) for ship wide Condition Based Maintenance (CBM). An open architecture standard is being developed to enable different manufacturers' sensors to operate within and independently of the power system.

Task 2: Wide Band Gap Devices

Another task integral to the IPS project is the study of advanced wide band gap power electronic devices and their direct application within the different IPS topologies. Today's power system development demands that electronics demonstrate the ability to operate at higher

temperatures, frequencies and power densities. The benefits of these demands are reduced cooling requirements, smaller magnetics, reduced system weight and improved efficiency. To help meet these demands, The EMPF is studying the different power conversion hardware and power requirements within the IPS architecture and assessing the potential for applying wide band gap devices to those applications. This includes identifying the potential advantages and disadvantages for each application and a transition plan for implementing the devices. The EMPF is modeling IGBTs and SiC VJFETs in the current electrical system. According to results of the theoretical model, the saturation current of the IGBT was almost 50 times larger than the saturation current of the SiC VJFET. Therefore, a single IGBT is capable of producing significantly more current than a single SiC VJFET. However, the transient time for the SiC VJFET is over 200 times faster than the transient time for the IGBT. Hence, the SiC VJFET will change faster and will drive other devices more quickly than the IGBT. The power dissipation of the SiC VJFET is also 25 times less than the power dissipated by the IGBT.

Task 3: Advanced Heat Exchangers

The final task of the IPS project encompasses the assessment of advanced heat exchanger technology within the current Power Electronic Module (PEM) being developed for the DDG 1000 program. There is a need to extract the heat that is generated by

the operation of today's power electronics. Reducing the junction temperatures of electronic devices enables them to operate at higher current densities. Lower operating temperatures also reduce stresses on the device, which leads to improved efficiency and reduced failures.

In order to adequately measure effectiveness in the IPS environment, cold plates are being manufactured with a similar form factor as in the PEM but using different advanced cooling technologies (Figure 5-1). These will be tested side by side in identical environments to compare design effectiveness under identical heat loadings. Heat exchanger technologies being investigated include foamed graphite, micro-channeled copper, copper pin-fin and copper tubing. A variety of thermal interface materials are also being tested including phase change metal alloys, metal foils, and filled thermal pads and greases. This testing will help determine the heat transfer capabilities, heat transfer mechanisms and properties of these advance heat exchanger systems. In addition, the EMPF has already modeled candidates for heat transfer fluids and has selected three for actual testing; water, propylene glycol, and Dynalene HC. At the conclusion of testing, the EMPF will be able to determine the most effective combination of technologies directly applicable to thermal management in a Naval Integrated Power System.

The Navy has plans for advanced and integrated power electronics in future platforms. To fully exploit the electric power available on these new platforms, a fundamental change in how electric power is converted, delivered and managed will be required. The EMPF will utilize its facilities to complete low power testing of the advanced power electronics hardware. For high power testing, the EMPF will partner with NSWC-Philadelphia to utilize the Land Based Test Site (LBTS) facility to complete testing and analyses of these new technologies. Along with increased performance, decreased weight, and higher reliability, benefits to the Navy include reduced system costs, improved maintainability and decreased manpower requirements.

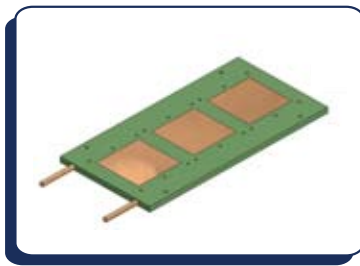
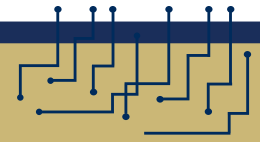


Figure 5-1: Cold Plate Design for Testing



Paul Bratt - *Paul* is an engineer at ACI. Comments or questions pertaining to this article can be sent to pbratt@aciusa.org



Packaging electronics designed to manage high voltage and high current requires specific design and manufacturing techniques. Most of the differences in packaging technologies are related to increased temperature and power handling capability. Standard power packages are currently being used to handle the most common power transistor devices. Component packages such as the TO-220 can be observed on countless assemblies. It is common to see these components coupled to a heat sink to help manage the high temperatures of operation. This package is excellent for smaller devices that process 20 amps or less. However, larger power devices may require some custom packaging to make them work efficiently. The EMPF Power Packaging Laboratory was developed to process high power and high reliability devices and offers these tips when considering packaging power devices:

The Right Stuff

Consider using metallic die attach materials in lieu of organic polymer die attach materials. The traditional polymer materials may experience some degradation at the higher temperatures generated by larger power devices. High lead materials used for die attach have shown to be able to handle the increased amount of strain at high temperature. Even eutectic tin-lead die attach materials are effective at relaxing the excess stress caused by power electronic temperature extremes. Gold-tin die attach materials should also be avoided for high-power applications because they may not absorb the stress of the die expansion at temperature. To help dissipate the heat generated by the high-power die operation, consider the use of aluminum silicon carbide (AlSiC) between any heat spreader and the die. AlSiC has excellent thermal conductivity properties and also matches well with the thermal expansion characteristics of the die.

Avoid the Void

The amount of voiding present in any thermally conductive material, such as die attach, should be kept to an absolute minimum. The presence of voids creates thermal losses that can lead to localized hot spots on the die. To minimize voiding in die attach materials, the EMPF utilizes die placement equipment that has scrubbing and ultrasonic capability. These operations promote wetting and help dissipate voiding in the die attach. Also, forming gas or nitrogen are the preferred bonding environments as they can allow for fluxless reflow and help eliminate the formation of new voids.

Bond Big

Aluminum wire bonds are the preferred method of interconnect between the die and leadframe pads. The wire bonds can range in size from 5-20 mils in diameter. Typical high-power aluminum bonding wire will be greater than 10 mils. The wedge bonders used to create these wire bonds must have capillaries capable of handling large wire and must have the ultrasonic power capable of creating reliable intermetallics through ultrasonic welding at room temperature. Gold wire is typically avoided in these applications because of the negative effects of diffusion and intermetallic formation at higher temperatures. If gold wire is bonded to aluminum pads in a power package, there is a risk of the following occurring:

- Kirkendall voiding at the bond connection increases the electrical resistance
- Purple Plague intermetallic formation decreases the mechanical strength of the joint
- Horsting voiding increases the resistivity
- White Plague at high temperature decreases the mechanical reliability of the bond

There is Safety in Numbers

Multiple wires at the same connection can be used for high-current applications to reduce the aluminum wire temperatures and increase long term reliability. However, increasing the number of wire bonds in the circuit will also increase the inductance of the circuit. The benefit of using multiple wires must be carefully weighed against the detriment of increased inductance. High-current applications may warrant the need for power ribbon. The larger aluminum power ribbons can carry more current than standard aluminum wire and therefore fewer number of wire bonds can be used for the same connection.

Successful electronics power packaging involves careful planning of the design, materials, equipment, and processes. Die attach, voiding, and wire bonding are three of the most critical parameters that must be addressed when working with power packages. Many conventional electronic practices, processes, and equipment are not applicable for packaging high reliability power devices.



Blaine Partee - *Blaine* is an engineer at ACI. Comments or questions pertaining to this article can be sent to bpartee@aciusa.org

Manufacturer's Corner

Lead Free Inspection: X-Ray

Current processes and procedures to clean electronic assemblies manufactured with tin-lead materials must be reviewed and updated when changing over to lead-free materials. Inspection procedures and processes, applicable to products built with tin-lead materials are now considered inadequate when using lead-free materials.

Electronic manufacturers converting to lead-free solder materials, are investigating x-ray inspection systems to enhance or re-build their acceptability/quality standards. X-ray equipment featuring a two-dimension x-ray process, provides basic x-ray shadow micrographs as the x-ray light source bombards the sample with x-rays. As different materials within the sample absorb the radiation, multiple shadows are captured by the detector. When subjected to an x-ray light source, solder and copper traces appear darker than the laminated circuit board substrate; the denser the material, the darker the shadow. The detector converts the resulting x-rays into an optical image for the operator to view and evaluate. Magnification of the sample is achieved by moving the x-ray light source closer to the sample.

X-ray settings, consisting of tube power and accelerating voltage, have a direct bearing on the quality of the resultant image. Although more power will produce a brighter image, there are technical limitations on the maximum power x-ray tubes can accept.

The image obtained from an x-ray light source passing through a sample is based on multiple factors including the density and atomic number of the sample materials. Solder materials containing lead are denser and have a high Z atomic value; solder materials without lead are less dense and have a lower Z atomic value. Usage of the same power tube setting to inspect lead-free solder material and solder material with lead will result in the lead-free solder material image being over exposed. X-ray settings must be appropriate for the types of material being inspected.

Leading manufacturers of x-ray equipment have developed and implemented advancements in technology for lead-free solder materials including comprehensive contrast and power adjustments, providing for more accurate and repeatable results. In the past many x-ray systems employed a closed x-ray tube which was sealed, preventing access to the tube components. Technology driven, x-ray equipment suppliers now offer open and/or changeable power tubes as these tubes provide higher magnification and resolution. Cost reductions pertaining to maintenance and serviceability are achieved by permitting access

to key components within the power tube.

The selection of x-ray equipment should be based on the product and production requirements, power tube configuration, operating system, reliability and physical location in the factory. One aspect of the equipment location that is often over looked is vibration. Image resolution can be significantly degraded by



Figure 6-1: Dage X-Ray Machine

the ambient factory vibrations. The solution can be as simple as shock pads under the legs or as complex as constructing an isolation mounting pad to eliminate the problem. Most x-ray suppliers can conduct a site survey to determine the best location and vibration mitigation strategy.

Two terms that are commonly used when defining x-ray capabilities are 'focal spot size' and "minimum feature size". Focal spot size has a direct relationship to achieving high image resolution; "minimum feature size" relates to a combination of object recognition processes. Focal spot size and image resolution are significantly influenced by the image- capture device, and the image processing system. When the focal spot size is reduced to meet the requirements of smaller component package types, exposure time must be increased to generate sufficient image quality. However, when the expose time is increased, thru-put is significantly reduced.

continued on page 11

Manufacturer's Corner

Lead Free Inspection: X-Ray (continued from page 10)

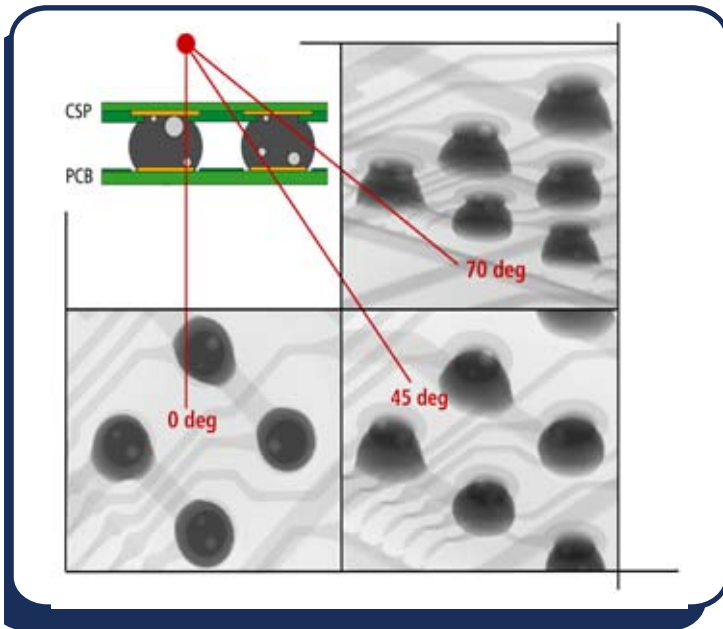



Figure 6-2: X-Ray Viewing Angles


The x-ray selection process should recognize and consider for value the many different features available on today's systems. Purchasing a high resolution x-ray system is not only a significant investment of capital but also represents a significant investment in analytical capability and is an invaluable process control tool for the factory.

For additional information on Dage X-Ray equipment or to schedule a demonstration of the Dage X-RAY equipment located at the EMPF, please contact Robert N. Berta by telephone at 610-362-1200 ext 253 or via e-mail at rberta@aciusa.org.



Robert Berta - *Robert* is the Business Development Representative at ACI. Comments or questions pertaining to this article can be sent to rberta@aciusa.org





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