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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government center and laboratories in the U.S.

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In this Issue

SiGe System on a Chip Cost and Parts Reduction

In the acquisition of new combat systems for the U.S. Navy, the challenge is to meet operational requirements while reducing cost and minimizing risk. System-on-Chip (SoC) is one solution to this challenge because it is a technology that includes the integration of all the necessary electronic circuits and parts for a system on a single integrated circuit (IC). This single IC may contain digital, analog, mixed-signal, and radio-frequency (RF) functions all on one chip.

The high integration levels offered by SoC can lower overall operating power, boost performance, and enable many new features not possible using standard components. This provides greatly expanded abilities compared to the performance limits of board-level systems based on off-the-shelf components. Since there is no physical prototyping during SoC design, systems designs which include complex logic, signal processing, and high power components, must use accurate simulations to provide design verification. Thus, the SoC Electronic Design Analysis (EDA) toolkits and design flows differ substantially from board-level design tools and flow. SoC based designs have a technological advantage in the market if they are done efficiently, but this requires more planning and effort during the design process. SoC technology is currently being used by the EMPF in the Silicon Germanium System-on-Chip (SoC) ManTech project. This includes development of transmit and receive ICs that will provide the capability to meet the low cost, weight and reliability requirements for phased array antenna solutions. These antennas will be designed for operation in the Ku band, which is suitable for radar in both surface and airborne applications. The EMPF, in partnership with Boeing (Phantom Works, Seattle, WA), will demonstrate manufacturability of the SiGe System-on-Chip devices, and the flip-chip-on-board (FCoB) interconnect technology suitable for use in Ku band radar antennas. This combination of SoC with flip chip provides the parts reduction, space savings and cost reduction necessary to provide the solution required for new radars. The reduction of the number of ICs and their size from the existing GaAs RF and Si logic radar circuit to a new single SiGe

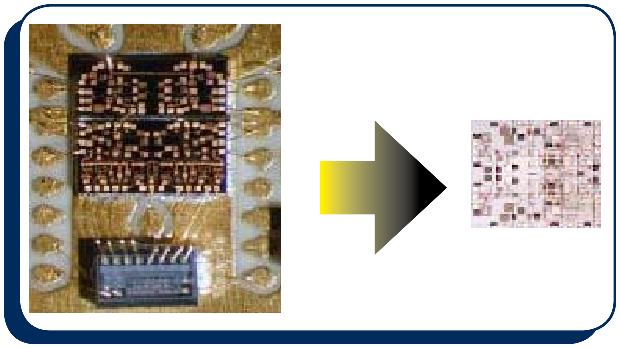

Figure 1-1: The IC size and chip count reduction (photo courtesy of Boeing Phantom Works)

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SiGe System on a Chip Cost and Parts Reduction
(Continued from page 1)

SoC radar circuit is shown in Figure 1-1. This technology can also be extended to satellite communication applications since the architecture utilizes very similar RF cell design.

Transmit/receive antennas have typically used GaAs chipsets. A key extension of this approach would involve the use of SiGe BiCMOS (Bipolar Complementary Metal Oxide Semiconductor) technology in lieu of more expensive GaAs. SiGe also offers the promise of higher levels of integration, combining the functions formerly accomplished by multiple GaAs chips plus a separate CMOS-based control chip onto a single SiGe Application -Specific Integrated Circuits (ASIC). Monolithic Microwave Integrated Circuit (MMIC) technology is a significant cost and size driver in phased array antennas, so this approach will help further reduce phased array antenna cost. This packaging approach is a revolutionary one based on the use of Chip-on-Board technology to provide a mass-produced solid-state replacement for the labor-intensive, heavy, and expensive traditional approach based on Multi-Chip Modules (MCM) and metallic waveguide structures. The packaging-related costs are anticipated to move downward over time, tracking well-established trends in the underlying technology. The use of SiGe for the ICs should also track similar established trends in the underlying semiconductor technology.

SiGe BiCMOS technology began manufacturing qualification in 1996 and has now completed at least 4 lithographic generations of development. This technology integrates high-performance heterojunction bipolar transistors (HBTs) with state-of the-art CMOS technology. Key technology characteristics for SiGe have been developed and are being used in current manufacturing processes with much success. Each generation of the technology leads to smaller feature sizes resulting in higher speeds and lower power consumption. When bipolar RF is integrated into the SoC with digital CMOS, this single chip solution allows up to 50mw of power savings through the elimination of intercommunication over the PCB. In addition to reducing power consumption, this integration also reduces cost (fewer pins) and PCB size (one chip instead of two), thereby significantly reducing the overall manufacturing cost.

One of the most quoted figures of merit (FoM) is the cut-off frequency - f_T of the HBT that increased from roughly 47 GHz in the 0.5 µm generation BiCMOS process to 210 GHz in the 0.13 µm process. The enhanced performance, along with the decrease in size, are the driving factors that promote a reduction in both the number of ICs required and the area needed to perform the required RF functions. Bipolar transistors give the speed required for the mixed and wireless applications, while the passives allow for the SoC integration, and the CMOS covers the logic requirements of the chip. Digital signals are also less sensitive to line noise, which also drastically increases board layout flexibility and permits the analog RF to be optimally positioned adjacent to an antenna. These improvements allow a decrease of the relative proportion of the RF area and more digital processing can be moved to the RF chip, enabling an integrated single chip solution. These design reduction factors are critical for RF radar applications that involve phased array antennas.

A key to manufacturability of SiGe technology is the use of existing high-volume CMOS manufacturing processes. The maturity of process equipment, level of factory automation, wafer handling, yield management and quality assurance for continuous improvement make it possible to deliver high quality wafers in complex process technologies. For similar process complexity (measured by the number of critical photomask layers or the number of process steps), the manufacturing cost and fab yield are comparable regardless of the details of the technology. The commitment to establishing a SiGe process within equipment capability makes it possible to deliver SiGe technology that is as repeatable and cost effective as mainstream CMOS.

In addition to the performance and die cost advantages that have promoted the growth of SiGe BiCMOS for RF transceivers, much lower product development costs are realized because of exponentially increasing cost of masks for each CMOS generation. Shorter time-to-market for SiGe BiCMOS products has been demonstrated because of the maturity of device modeling, the design platform, and the manufacturing capability that is possible when using well-established process modules and fab equipment.

The current Mantech project technology insertion improvement plans call for enhanced future performance and lower cost. The SoC and FCoB technologies enable use of low-cost Phased Array Antenna (PAA) architectures which will produce significant cost savings. Cost savings of as much as 65% and weight savings of as much as 25%, compared to current phased array antenna technology, can be achieved using the FCoB approach based on the use of GaAs technology. The use of SiGe technology can further reduce semiconductor chip-set costs by up to 90%. In addition, the FCoB technology currently in development at Boeing is limited to 20 GHz due to the lattice spacing requirements and the size of GaAs chips necessary to perform the module functions. SiGe has the potential to reduce the chip-set footprint, thus extending the

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Design For Manufacturing and Assembly

The terminologies "Design for Manufacturing "and "Design for Assembly" cover a very broad spectrum of operations that are intended to integrate the various elements of manufacturing into a cohesive system. Any DFMA system will account for different product manufacturing paths, which include alternate design, materials, process, and their respective impacts on production costs and product quality. Fundamentally, the premise for DFMA is to define the parameters at a very early stage, consider the advantages and disadvantages of pursuing a particular set of design rules, account for the various cost alternatives and assess the metrics used to deliver the final product.

There is no one unifying approach that is an unyielding tenant of DFMA. Reducing cost and cycle time, while maintaining or improving the quality and serviceability of a product, remains a central theme in the execution of a DFMA system. Ideally, the use of COTS materials would be preferred for reducing lead time, cost and maintenance as well as having an increased availability of components. In some cases where changes in the market have driven manufacturers toward a rapid assimilation of new technologies, the implementation of a DFMA program is vital to avoid the potential roadblocks that can impede rapid progress.

A prime example of where DFMA is now being employed is in lead-free manufacturing. The use of a suitable DFMA method can be instrumental for the transitional phases of package assembly, where the introduction of a lead-free solder can have a significant impact on the subsequent manufacturing processes. For instance, some of the factors to be considered in a lead-free package design, which can potentially cause risk, are:

1. Circuit design- What are the proximity and the locations of the active and passive circuits?
2. Component geometry – Are BGA's, QFP's or other devices going to be warranted, and how will they impact soldering operations?
3. Substrate materials – Are the substrate properties chosen for the design suitable for the higher assembly temperatures?
4. What specific alloys will be utilized as the replacement for SnPb? Will the alloy replacements cause issues for productivity and quality down the line?
5. Will there be additional environmental testing needed for the qualification of a lead-free process?
6. What additional equipment costs will be incurred by changes in process?

In answering some of these questions pertaining to lead-free manufacturing, a projected critical path is created. In doing so, DFMA allows for the identification of potential risks and benefits for each respective assembly process, while employing the design guidelines necessary to meet the performance metrics. A proper approach combines experience and prior knowledge, along with new research studies and tools, to bring the DFMA process beyond the abstract and into a working manufacturing model.

There are a variety of vendors and software configurations used to monitor and sustain the DFMA efforts, most of which organize and integrate all the various inputs from the contributing manufacturing sectors. In some cases, the resulting output is a theoretical index designed to gage the efficiency of the specific process as defined by the user. Some software is simply designed as itemized checklists or flow charts to ensure that the proper process parameters are entered. Others rely on internal design rules that integrate a good cross section of pertinent manufacturing and assembly information to deliver an effective system. In either case, whatever DFMA system is chosen, there is a need to guarantee that the proper inputs have been considered for the critical path chosen. The success of optimizing any manufacturing process is only as good as the information that is gathered through contributions from each individual, section, or department involved in producing the product.

At the EMPF, we are often engaged in the development of new electronic packaging technology. One of our goals is to keep re-educating ourselves on the importance of maintaining flexibility, quality, and cost for our valued customers. DFMA is another tool in the tool box that helps us achieve those goals through both our learning center and our manufacturing facility. For more information on the courses offered, please visit the EMPF website at www.empf.org and click on training.

Next Month - We will breakdown a DFMA case study.

Author: Carmine Meola, Senior Electronics Manufacturing Engineer.

Ask the EMPF Helpline!

A customer called into the EMPF Helpline...and asked what type of training and logistics would be needed to implement IPC/EIA J-STD-001 and WHMA-A-620 specifications in a shipyard located in the southeastern United States.

In late September 2006, a senior quality-assurance supervisor, working for a shipyard located in the southeastern United States, contacted the EMPF helpline. A number of time-critical needs were identified by the supervisor:

- The need to immediately conduct training in IPC/EIA J-STD-001 (Requirements for Soldered Electrical and Electronic Assemblies) onboard the ship, to a team of electrical technicians;
- The need to conduct an inspection of equipment in order to validate the capability to perform to applicable specifications;
- The need to supervise and validate that wire harnesses were being manufactured to J-STD-001 and inspected to WHMA-A-620 specifications.

Electrical specifications issued to the EMPF confirmed that J-STD-001 and WHMA-A-620 standards were specified for wire harness fabrication and soldering of connectors and inter-connects. These specifications had been implemented to supersede previous electrical fabrication standards. The J-STD-001 and IPC-A-620 standards better support the high-reliability requirements of the complex equipment scheduled for shipboard installation. Improved reliability reduces the need for repairs over the service life of the ship. Fewer repairs reduce maintenance costs and increase the affordability of operating the ship.

An experienced EMPF instructor/technician, trained and certified to J-STD-001 and WHMA-A-620 standards, was identified and made available to the shipyard. Arrangements were made for EMPF equipment to support product build requirements to be forwarded to the shipyard. Upon arrival, the EMPF technician conducted an inspection of the multiple shipboard compartments where the harnesses and interconnects would be fabricated.

After inspection, the shipyard supervisor briefed the EMPF technician on the tight shipyard build-schedule. The updated build-schedule did not allow time to train the shipyard electrical technicians prior to fabrication of the wire harnesses.

This time schedule was a change from the scope of work previously defined by the shipyard and accepted by EMPF. Within 24 hours the EMPF developed, submitted, and received authorization to modify the original scope of work. With the modified scope of work, the on-site EMPF technician fabricated the wire harnesses to WHMA-A-620 specifications, and made all solder connections under the supervision of a NAVSEA inspector. Among the different types of connectors were "J" plug connectors, which are locking connectors commonly used with avionics instrumentation. The J Plug connectors, located outside on elevated stanchions and bulkheads, required special procedures to insure that the solder iron tip was at the correct temperature for proper solder reflow. For example, a portable windscreen was designed and fabricated to enclose the immediate work area surrounding the J plug connectors.

Upon completion of the harness fabrication and the soldering of connectors and interconnects, the EMPF technician conducted J-STD-001 and Certified IPC Specialist (CIS) training. This training was tailored to the specific needs of the shipbuilder. The Training and Certification Program provides individuals with a valuable credential that recognizes their understanding of J-STD-001 and is valid for 2 years. This standard has emerged as the preeminent authority for electronics assembly manufacturing. It describes materials, methods and verification criteria for producing high quality soldered interconnections. The standard emphasizes process control and sets industry-consensus requirements for a broad range of electronic products.

Training to J-STD-001 and WHMA-A-620 standards are critical to the long-term success of businesses directly engaged in the electronic manufacturing industry. This case study is an example of how the EMPF quickly responded to a company's need to build wire harnesses to their application specific standards and train employees without impacting the build schedule. For further information on this training contact the EMPF helpline at 610-362-1320.

Author: Rebecca Morris, Production and Applications Engineer.

Cleaning Challenges for the Electronics Industry

The process of cleaning electronic assemblies is in a state of transition with the lead-free (Pb-free) movement and trend in the direction of paste/flux chemistries. The impetus to restrict lead within the US began with the EPA's proclamation to gradually reduce lead in gasoline starting in 1973. In addition, the Consumer Product Safety Commission began regulation of the manufacturer of paint with greater than 0.06% lead in 1978. Within the electronics industry the Environmental Protection Agency's (EPA) Toxic Release Inventory implemented a reduction in the reporting thresholds in 1999 for lead from 10,000lbs to the current threshold of 100lbs per year. Outside the US, the European Council and European Parliament started a ban on hazardous materials like lead affective July 1, 2006 as per the Waste Electrical and Electronic Equipment (WEEE) Directive and the Restriction of Hazardous Substances (RoHS) Directive. In Japan, the Japanese Ministry of Industry and Trade had a proclamation that lead usage will be reduced by 67% by 2005. As a result, the shift in PWA manufacturing overseas will and has impacted domestic customers.

Properties of Pb-free solders

Eutectic tin-lead solder (also known as Sn63) consists of 63% tin and 37% lead. In metallurgical terms eutectic refers to the lowest melting combination of these two metals, in this case 183°C. Historically, this ratio of tin- lead solder has dictated the types of materials which could be used in PWB base material and component packages.

Alloy	Melting Temperature
AnBi	138°C
SnAgCuBi	215°C
*SnAgCu	218°C
SnAg	221°C
SnAgCuSb	222°C
SnCu	227°C
SnSb	240°C

Table 4-1. Common lead-free alloys

** This alloy has been identified as a primary combination with two specific variations coming from Japan (96.5% tin/3.0% silver/0.5% copper) and North American Electronics Manufacturing Initiative (NEMI) (95.5% tin/3.9% silver/0.6 % copper)*

In combinations other than that of eutectic, solder does not melt or become liquidus at a specific temperature but has a melting range. As a result, the use of non-eutectic combinations means solder joint formation occurs over a range. The alloys shown in Table 4-1 are being evaluated by many manufacturers for future production applications or are being used in the field currently.

In the case of SAC (tin-silver-copper) Pb-free solders, the surface tension is greater than the standard eutectic Sn63/Pb37 [548 mN/m vs. 481 mN/m respectively], indicating this Pb-free solder type would not wet as easily.

Many of the Pb-free alloys have a tendency to readily oxidize since tin is often the major component and oxides of tin are more stable than those of lead (i.e. lower heat of formation [ΔH_f] SnO -69 cal/mol, SnO_2 -143cal/mol, PbO -53cal/mol, PbO_2 -67cal/mol). The presence of these stable tin oxides inhibits wetting. Another trend being observed with commercial customers is the use of Organic Solder Preserve (OSP) as an inexpensive answer to the Pb-free requirements in combination with Pb-free solders and no-clean chemistries.

These factors, in addition to increased use of no-clean chemistries have forced manufacturing engineers to modify their processes in order to obtain the appropriate soldering results with more flux being used in the case of hand soldering. These increased flux loadings and because hand soldering involves isolated heating of the board, more residue can be expected. Such residues can lead to dendrites, electrochemical migration (ECM) or corrosion (Figure 4-1).

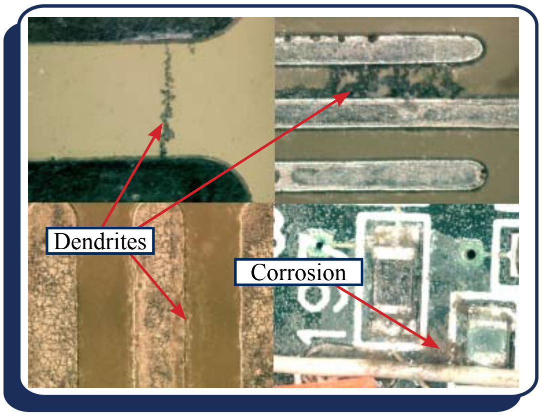

Figure 4-1. Examples of dendritic growth (ECM) and corrosion

The increased reflow conditions of Pb-free solders is another possible source of residues as polymerization of the flux can occur making cleaning difficult. The accepted guideline, J-STD-004, describes the different flux systems by type and activity. Activity refers to what gives the flux/paste its cleaning action. Historically activity was achieved through addition of halides. Halide residues are usually very corrosive by themselves and their level is important. There are other less aggressive means to achieving activity such as addition of a weak organic acid. This defined activity is broken up into halide activity as a percentage, and 0 or 1 (the absence or presence of halides respectively). The flux residue activity is represented by letters: L=low, M=moderate, H=high. The specific designations are:

- o Rosin (RO) or the traditional flux type is based upon tree sap (colophony)
- o Resin (RE) based are synthetic and contain some form of organic polymer as the matrix

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Cleaning Challenges for the Electronics Industry (continued from page 5)

- Organic (OR) are composed of weak organic acids (e.g. formic acid, succinic acid or adipic acid)
- Inorganic (IN) are synthetic and can be composed of salt-based (e.g. ammonium chloride), alkali (e.g. amines) or mineral acids (e.g. phosphoric acid)

The definition of what a no-clean is does not allow it to fall under one of these categories. The key with the no-cleans is they are designed burn off during soldering with little or no detrimental residue remaining which may or may not be cleaned.

No-clean fluxes historically provide different soldering results as compared to activated fluxes. In addition variation in the make up of such residues can be drastically different from manufacturer to manufacturer (Figure 4-2).

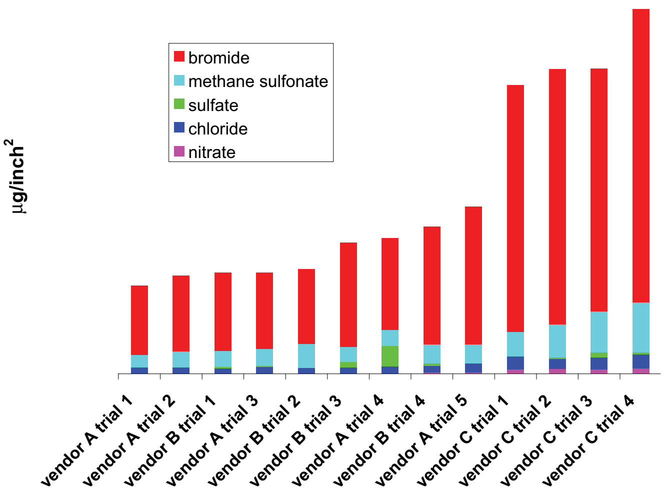

Figure 4-2: Ion chromatography analysis of residues from the three no-clean pastes

Cleaning trends

Cleaning chemistries have changed since the Montreal Protocol banned halogenated hydrocarbons. Those early chemistries worked very well for the flux residues of the day (activated rosin) by dissolving and washing them off the surface through direct immersion, spraying or vapor degreasing. The number of options available today is less as water is accepted as the "universal solvent".

Because of the limited solubility of many materials in water, the key to removal is a combination of time, water volume, temperature and efficiency of agitation. Ultimately, water alone may not suffice, thus additives (surfactants) are introduced to reduce surface tension, improve penetration, and induce one or more of the following phenomenon: wetting, emulsification, solubilization, saponification, deflocculation, and sequestration. When dealing with a cleaning dilemma, the key considerations are:

(1)Understand what you are trying to remove.
(2)Determine the limitations of the assembly. Are there any temperature, moisture or vibration sensitive parts?
(3)How densely populated is the assembly. Where are problem spots going to be where residue could collect or become trapped?
(4)What are the long term reliability goals?

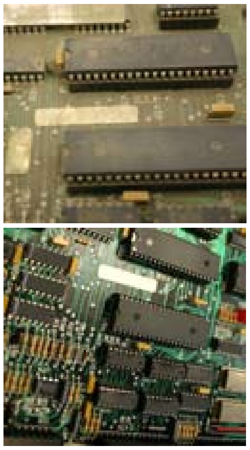

Figure 4-3. Photos of assemblies before (top) and after cleaning (bottom)

As the implementation of Pb-Free materials into electronic manufacturing centers continues to increase, the demand for products built with tin-lead materials declines, impacting the availability of tin-lead plated parts. This has required manufacturing centers to find alternative resources to obtain tin-lead components, often from warehouses and inventories where proper storage conditions were not always maintained. The ability to recover these materials for use will depend upon what surface contaminate is present (dirt or surface oxide). ACI has in the past demonstrated its ability to recover heavily oxidized parts through a process called ROSA (Reduced Oxide Solderability Activation). This recovery technique is expected to find increased demand as the previously mentioned trend takes effect. A more recent example of the EMPF's quick response to an emergency request involving recovery of urgently needed replacement parts is shown in Figure 4-3.

Ultimately, the Pb-free transition has begun. While most of the issues with Pb-free are recognized and being addressed, there are remaining issues still present that revolve around logistics and sourcing of parts. There will be instances of companies running both lead and Pb-free processes on the same floor until a complete transition to Pb-free occurs. In addition, there will be customers who maintain tin-lead processes for contractual reasons or exemptions as with the US military. As a result, they will still need support in this arena. The EMPF has recognized this and is making efforts to satisfy those needs.

Author: Sam Pepe, Chemist.

SiGe System on a Chip
Cost and Parts Reduction (continued from page 2)

practical frequency range for this architecture to 40 GHz or beyond.

In conclusion, the evolution of an RF transceiver from a set of chips tailored for each function and implemented in a variety of processes to a single, small, low power, low cost SiGe SoC chip has been the result of optimized process technology. This optimization has included integration of bipolar transistors with CMOS for low-power digital control and analog frequency synthesis. The known solutions for scaling provide an opportunity for significant die size reduction using SiGe BiCMOS technology versus industry-standard CMOS technology. This die size savings can be translated into smaller packages, lower weight and lower total cost depending on the level of analog and digital integration. Product yield can also be improved, in conjunction with mixed-signal integration, due to the reduction in the number of interfaces between ICs.

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Author: Mark Allemang, Lead Materials Engineer

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Thermal Improvements to Power Electronics Modules

The trend for reducing the size of power electronics systems requires smaller footprints for power Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) and Insulated Gate Bipolar Transistor (IGBT) modules. This has resulted in higher power dissipation densities for the IGBT die, as well as the module, due to a higher packing density of the die. Also, increases in switching frequencies and voltage ratings of IGBTs result in higher power dissipation at the die level. Some of the die power losses have been offset by advances in both MOSFET and IGBT chip design, but the cooling capabilities of present modules limit the device performance.

The Navy's next-generation multi-mission destroyers will reduce the size, weight, and cost of its power electronic modules. This requires components that have higher current densities, higher switching frequencies, and higher operating temperatures than current generation electrical systems. However, power electronics packages available today are not designed to meet ship-board environmental and operational demands due to an unacceptably high package thermal resistance. Additionally, commercial component suppliers are generally averse to the risks associated with developing new technologies for military applications. The challenge for the EMPF is to faciliate the development of advanced power devices that will be applicable to power systems used in future surface ship platforms.

In an effort to overcome the challenges of efficiently and economically cooling the increasing power dissipation densities, the EMPF has teamed with two thermal management companies to develop advanced cooling strategies for the DDG 1000 Power Electronic Modules (PEMs). The EMPF is providing expertise in power electronics packaging design and manufacturing in addition to its knowledge base of Navy applications. Additionally, the team is working with IGBT manufacturers to integrate the advanced thermal management schemes into their packages while maintaining a standard footprint. In this article, the two thermal management strategies will be reviewed and compared to the conventional methods.

Currently, most power modules are designed to be cooled by attaching the module to an external heatsink or cold plate and cooled by forced air or circulated liquid, respectively. As shown in Figure 5-1, the critical layers in the thermal path of a conventional IGBT module are the IGBT die, the die attach solder, a direct bonded copper (DBC) ceramic substrate, substrate attach solder, metal or composite baseplate, thermal interface material (TIM), and the external coldplate. The ceramic substrate provides electrical isolation between the die and the module baseplate. Aluminum nitride (AlN) is preferred over alumina (Al_2O_3) because of its higher thermal conductivity. Each layer contributes to the thermal resistance between the die and the ambient through the relationship:

$$R_t=\rho \times t/A$$

where R_t is the thermal resistance, ρ is the material resistivity, t is the material thickness and A is the contact area. In very general terms, the total thermal resistance is a sum of the resistances of each layer. With the many layers in the heat flow path, this configuration is not capable of adequately cooling devices with power dissipation densities beyond 250 - 300 W/cm².

Recently, two complementary strategies for improving the effectiveness of power module cooling have emerged. One method focuses on reducing the thermal resistance by eliminating layers between the die and the cooling medium and also reducing the thickness and/or thermal resistance of the remaining layers. The second method has been aimed at increasing the efficiency of the cold plate by improving the heat transfer from the body of the heatsink to the coolant. Cross sections of two examples of integrated heatsink concepts that utilize the combination of these methods are shown in Figures 5-2 and 5-3.

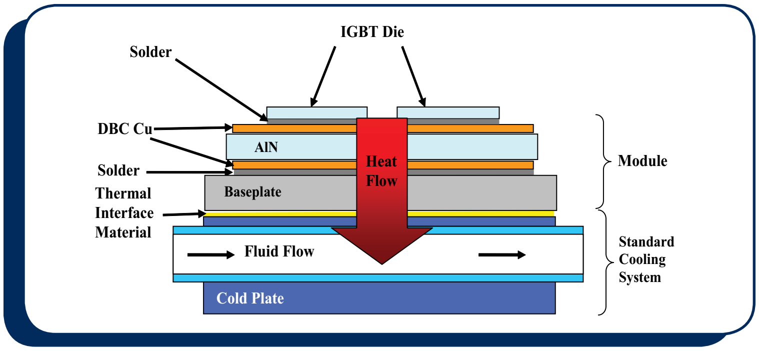

Figure 5-1: Cross section of a conventional liquid cooled module.[1]

Figure 5-2 is a schematic concept of a Normal Flow Cold Plate (NCP) developed by Mikros Technologies, Inc., Claremont, NH, as integrated within an IGBT package. The thermal path to the cooling fluid is reduced, replacing the baseplate and thermal interface material. The design of the NCP will address a potential mismatch of the Coefficient of Thermal Expansion (CTE) with the ceramic substrate. Another option that would not require CTE matching would be to micromachine the channels into the DBC copper, eliminating the solder interface to the cold plate. The latter

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Tech Tips...

Current Sensors

The US Navy's all-electric fleet will require tens of thousands of electrical sensors. A large percentage of these sensors are required to monitor and regulate power flow. Because power systems generally have fixed or stepped voltage outputs, current is often a variable parameter. As a result, current sensing is critical. The following tips list important advantages of several current sensor types in order to facilitate choosing the best current sensor for a particular application.

Sense Resistor current sensors

Sense resistors heat up in proportion to the resistance applied while conducting current. Therefore, sense resistors with lower resistance values are more likely to measure higher current levels without overheating. The response time for sense resistor current sensors is defined and limited by the instrument that measures the voltage drop across the resistor. The sense resistor tolerance determines the accuracy of the current reported by the system. The primary disadvantage of sense resistors is that they are direct measurement devices. This means that the sensor must be part of the high voltage circuit in order to measure current.

Current Sensor	Advantages	Disadvantages
Sense resistor current sensor	Sense resistors are compact in size and simple to operate.	Resistors generate heat while conducting current. The amount of heat is proportional to the square of current passing through the resistor. Therefore, sense resistors are not used for high current applications.
	For relatively low currents, sense resistors provide accurate measurements as long as the resistors have a small tolerance.	Sense resistors are not isolated from transient voltage potentials on the load.
	Sense resistors are also the cheapest current sensor technology.	Other circuitry, like instrumentation amplifiers, may be required to generate a distinguishable signal from sense resistors.
Hall effect current sensor	Hall effect current sensors are small and light in weight	The output from Hall effect sensors is highly temperature dependent.
	Sensors are electrically isolated from transient voltage potentials on the load	Hall effect sensors usually require a stable external current source.
	Hall effect sensors have a rapid response time and are highly accurate.	Closed loop systems are limited by how much restoring current they can draw.
Current transformer	Current transformers are relatively simple to implement and can sense hundreds of kilovolts of current.	The ferrite material used in the core of many current transformers can saturate at high currents.
	These sensors are passive devices and do not require external driving circuitry.	The accuracy of current transformers will degrade over time if the core is magnetized.
		Current transformers are large and heavy and have lower operating temperatures than other current sensor technologies.
Rogowski coil current sensor	Rogowski coil current sensors are small, light in weight, and can sense hundreds of kiloamps of current	Rogowski coil current sensors are among the most expensive current sensing technology.
	Sensors are accurate and do not saturate at high current levels	External circuitry is required to analyze the sensor output.
	Rogowski are also isolated from primary conductors.	
Interferometric and polarimetric current sensor	The size of both fiber optic sensors is independent of the measuring range.	Fiber optic sensors are expensive
	Sensors are highly accurate and can measure higher current levels than other current sensing technologies.	Polarimetric Optical current sensors are susceptible to external magnetic interference.

Table 6-1: Advantages & Disadvantages of each Current Sensor Type

Hall Effect current sensors

Hall Effect sensors are advantageous because they can eliminate errors such as offset drift, sensitivity drift, and saturation of the magnetic core. Therefore, select Hall Effect current sensors when utilizing small tolerances for current measurements.

Current Transformers

Current transformers (CT) are simple devices that do not require driving circuitry to operate and utilize a sense resistor for current measurement. Current transformers are generally of two classes: protection relay CTs and instrument CTs. The protection CT must saturate sufficiently high to allow a relatively accurate measurement of the fault current. Conversely, an instrument CT requires good accuracy around the nominal current. Instrument CTs by design cannot withstand currents as high as the protection CTs. Some CTs have secondary windings dedicated to protection and metering.

Rogowski Coil current sensors

Rogowski coil current sensors are advantageous because they do not suffer from voltage saturation. This makes the technology useful over a wide current range (30 amps – 300 amps) which results in a reduction of the number of sensors needed to cover a given application.

Interferometric Sensors

Interferometric sensors are not susceptible to external magnetic fields unless the sensor is encompassed by the fiber loop. Therefore, such sensors can be employed in areas where external magnetic fields may otherwise influence current measurements.

Polarimetric Sensors

Polarimetric sensors have the potential to be influenced by other magnetic fields residing nearby. This sensor is also sensitive to temperature. However, if the temperature is known, the sensor's response to magnetic fields can be removed from the current measurement by electronic means. Polarimetric sensors are advantageous because they may serve dual purposes as both a temperature sensor and a current sensor. Table 6-1 summarizes the advantages and disadvantages of each current sensor type.

Author: Joyelle Harris, Materials Engineer

cut here and save!

Manufacturer's Corner
Rework Equipment

Electronic manufactures, as they implement lead-free repair and rework processes, are quickly recognizing higher reflow temperatures can quickly damage array packages. To reduce damage to components, many companies are investigating suppliers of re-work equipment to validate their offerings will meeting lead-free re-work/repair requirements.

In the past, rework and repair equipment provided a basic process with results directly dependent on the skill sets of the operators. High cost, delays in production thru-put, component damage and quality assurance concerns were direct subsets of early technology circuit board rework or repair procedures.Today, leading manufacturers of rework-repair equipment have developed and implemented advanced technologies to mitigate the issues of component damage. With lead-free solders as an added variable, reflow temperatures are higher, time above the higher reflow temperatures are different, appearance of the joint is considerably different, and the need for process control is even greater than for eutectic solders. Reworking array package components using lead-free solder follows similar steps to leaded components with eutectic solder: establish and validate the thermal profile, remove the failed component, clean and prepare the site, prepare and place the new component, reflow, and inspect. As found in the assembly process, precisely controlled convection heating, not radiation, achieves a repeatable process.

Many different lead-free compositions exist; the most common are based on tin alloyed with small amounts of silver, copper or bismuth, with melting points in the range 206-221°C. Solder peak temperatures are higher, 217°C to 235°C. The window for lead-free processing is smaller than with leaded solder materials. The time above reflow is often reduced from 60-90 seconds for eutectic tin-lead solder down to 15-30 seconds for lead-free. Rework systems must be capable of ramping up and down very fast to achieve these temperature requirements. Using convection permits the development of a precise, repeatable thermal profile that will not overheat or over stress the package. Establishing the ideal profile is but a part of the process. Profile development requires knowledge of materials and usage of equipment designed to meet process requirements.

The higher temperatures needed for lead-free, coupled with the thermal sensitivity of BGAs and CSPs, demands precise temperature control and the addition of a ramp stage where temperatures rise at a rate that will not harm packages. Today's more sophisticated rework systems employ four heating zones and one cooling zone. Successful lead-free rework is difficult to achieve without this extra step. Higher temperature requirements and thermal sensitivity of area arrays can be problematic without the ability to ramp temperatures at a rate that will not harm components. Having a controllable pre-heater allows for efficient pre-heating that avoids the thermal damage risked when working with expensive, but sensitive, packages unsuitable for heating above 235°C with quick reflow times.

A typical lead-free profile would be to pre-heat to 140°C in 100 seconds, followed by a soak zone below 170°C for 90 seconds , then a ramp up to 225°C in 100 seconds, reflow up to 235°C for 20 seconds and then a cool down for 60 seconds. The differences between this and a tin-lead profile are substantial, and the key is system control with the ability to ramp up faster and cool down quicker. Another factor to consider with lead-free is the temperature difference, or delta T, across the soldering area. A ΔT of 10°C is considered acceptable to produce a good tin-lead joint, but this is halved to 5°C for lead-free. The wetting process and temperature profiles must be controlled to ensure the resulting joints are strong and not brittle. Improved heating regulation and faster ramp-up are needed with lead-free – particularly in the under-board heater, which means that hot plates should not be used. Temperatures must be high enough to melt and form intermetallics, activate flux and optimise wetting, yet low enough to avoid damaging the PCB and component.

While the basic rework steps remain the same, the substantial temperature differences between eutectic and lead-free solders mean tighter processes, better temperature profiles and the use of precise rework systems with closed-loop process control are required if high quality, low cost rework is to be achieved.

For additional information on OK Industries rework-repair equipment or to schedule a demonstration of the OK Industries rework-repair equipment located at the EMPF, please contact Robert N. Berta; telephone at 610-362-1200 ext 253 or via e-mail at rberta@aciusa.org.

Author: Robert Berta, Business Development Representative.

Thermal Improvements to Power Electronics Modules (continued from page 8)

option would further reduce the thermal path, as well as increase the efficiency of heat transfer to the cooling fluid. CTE matching would be less critical due to the thin, compliant copper layer.

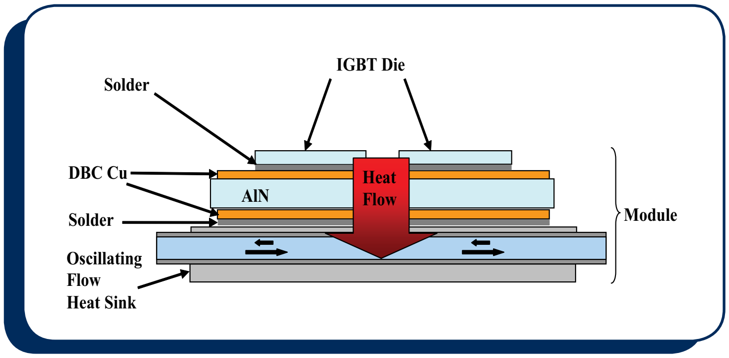


Figure 5-2: Integrated Normal Flow Microchannel Cold Plate.[1]

The Mikros approach offers a liquid-cooled heat sink with:

- High heat flux capability - can remove in excess of 1000 Watts/cm^2 with an approach temperature difference of only 30°C.
- Very low thermal resistance - as low as 0.03°C/(W/cm^2)
- High effectiveness - approaching theoretical limit
- Low pressure drop
- Scalability from millimeter sizes to tens of centimeters for IGBT power devices.

Another approach to integrated thermal management for high power devices has been developed by Advanced Cooling Technologies, Inc. (ACT), Lancaster, PA. The Oscillating Flow Heat Sink that they have developed, as integrated in an IGBT package, is shown in Figure 5-3.

ACT's oscillating liquid heat transfer technology incorporates a mechanical actuator to generate an oscillatory motion of the liquid. The oscillating liquid absorbs heat with a very high efficiency due to the disrupted liquid-wall boundary layers, which increases the effective thermal transfer from the heat source to the heat sink. The heat transfer performance can be controlled by adjusting the amplitude and frequency of the actuator output.

Fluid oscillations have been investigated over a frequency range of 0 to 20 Hz and amplitudes of 0 to 12". The oscillating flow heat transfer, with a proper combination of oscillating frequency and stroke, can remove heat fluxes in excess of 1,300 W/cm^2. This is equivalent to a thermal conductivity value approaching 250,000 W/m-K. For comparison, a 1/8" OD and 12" long copper/water heat pipe can only handle heat fluxes up to 40 W/cm^2. Additionally, the thermal conductivities of copper and diamond materials are on the order of 380 W/m-K and 1,200 W/m-K, respectively.

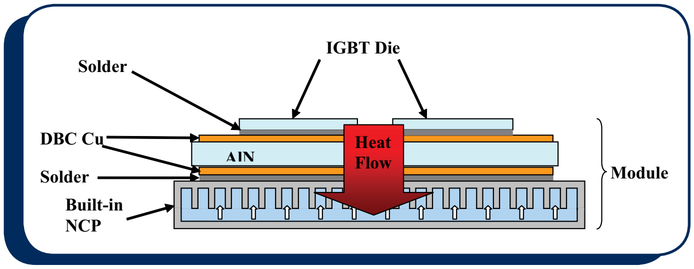
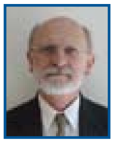


Figure 5-3: Integrated Oscillating Flow Heat Sink

At the current stage of the project, the effort is to demonstrate the effectiveness of the two technologies. The EMPF has identified candidate IGBT modules that would be compatible with the power electronic modules used in the Naval Integrated Power Systems (IPS) project (Empfasis, Aug. 2006). We are working with the manufacturers to develop strategies for technology evaluation and insertion into their product lines. The applications would extend into emerging commercial applications which could include electric vehicles, as an example.

These projects are a part of the EMPF's continued activity in the Navy's ship building affordability initiative. By developing collaborative projects that reduce the acquisition costs of ship board electronics, the EMPF can introduce advanced manufacturing processes, improved electronic devices, materials and system technologies. Expanded use of COTS, open systems and an increased use of electronic functional integration continue to be applied to ship board systems that will result in substantial savings to the Navy.



Author: Mike Barger, Lead Research & Development Engineer.

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[1] *Leslie, Scott G. "Cooling Options and Challenges of High Power Semiconductor Modules."* *Electronics Cooling* *12.3 (2006): 20-26.*

Training Course Schedule 2007

Skills

BGA Manufacturing, Inspection & Rework
April 3-4
June 18-19

Chip Scale Manufacturing
March 28-30
June 20-22

Electronics Manufacturing

Boot Camp A
April 16-20
June 4-8

Boot Camp B
April 23-27
June 11-15

Certifications

IPC J-STD-001 Instructor Certification
March 12-16
April 9-13
May 21-25

J-STD-001 Instructor Recertification
March 21-22
April 25-26
May 16-17

IPC-A-610 Instructor Certification
April 16-20
May 14-18

IPC-A-610 Instructor Recertification
March 19-20
April 23-24

WHMA-A-620 Wire Harness Manufacturing (Operator)
March 13-15

IPC-7711 Certified IPC Specialist (CIS) SMT Rework
May 7-9
August 13-15

IPC-A-600 PWB Acceptability
April 9-11
May 29-31

IPC Challenge
March 23
April 27

IPC-7711/7721 Certified IPC Specialist (CIS) SMT Rework and Circuit Repair
May 7-10

IPC-7711/7721 CIT Recertification
April 4-5

IPC-7711/7721 CIT Certification
March 5-9

IPC-7721 Certified IPC Specialist (CIS) Circuit Repair
April 30-May 1

IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCB's
April 30-May 3

Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing
March 26-27
April 30-May 1

Design for Manufacturability
April 11-12
May 24-25

Failure Analysis and Reliability Testing
March 6-8
May 21-23

For more information, please call (610) 362-1320 or email: registrar@empf.org

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