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*The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government center and laboratories in the U.S.*

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## Designing Silicon Germanium System on a Chip

Advanced RF devices, such as Silicon Germanium System on Chip (SiGe SoC) can be used in place of traditional RF components to lower overall operating costs, boost performance, and enable new capabilities. One key advantage of using Silicon Germanium in a System on Chip configuration is that an integrated circuit (IC) can be developed that contains digital, analog, mixed-signal, and RF functions on a single chip. An important application where SiGe SoCs can offer improvement is Phased Array Antennas (PAAs).

Phased Array Antennas (Figure 1-1) used by the Navy need to be made smaller, lighter, and more affordable. A Phased Array Antenna is constructed by arranging many small RF transmitting or receiving modules in an array. This enables the RF beam to be steered by controlling the phase of each individual module instead of mechanically steering a conventional RF antenna. The upper

limit of the range of frequencies to which an antenna may be applied is limited by the spacing of the array. This in turn is limited by the size of the individual modules. A module constructed using a SiGe flip-chip system-on-chip package enables the implementation of Phased Array Antennas that operate beyond the 15-20 GHz currently possible with chip-on-board and gallium arsenide (GaAs) chipset technology alone. The EMPF is partnering with Boeing to demonstrate manufacturability of the SiGe System-on-Chip devices. The first phase of the ManTech project evaluates the component architecture, producibility of SiGe wafers, and packaging of die using flip-chip-on-board (FCoB) interconnect technology.

#### Test Cell Design

An initial step in the SiGe SoC design is to break up the circuit into test cells that facilitate testing of the individual components that will be used in the full system. SiGe test cells were created to properly assess the suitability of manufacturable SiGe technology for high-reliability RF applications. The test cells contain several variants of a particular device to determine which will optimum for the design. In addition to inductor designs, the test cells contain phase shifters, polarizer combiners, multiple amplifier designs, and other antennae supporting devices. During layout design, special attention was paid to developing a procedure that allows testing of the die that is sufficient to determine if parts are operable prior to packaging. The die was also designed with 32 daisy-chained flip-chip contacts around the periphery to

continued on page 3



Figure 1-1: Phased Array Antenna

# Ask the EMPF Helpline!

A customer called into the EMPF Helpline asking for testing to confirm RoHS compliance...

A Tier-Two Electronic Manufacturing Service (EMS) provider, located in the Mid-Atlantic region, recently received a multi-million dollar contract to build RoHS compliant product. This contract required the procurement and integration of an electronic sub-assembly into the main product from a third party EMS provider. In order to certify the end product was manufactured to meet RoHS requirements, the EMPF was solicited to provide non-destructive inspection of the electronic assemblies of the third party EMS provider.

the ability to minimize the energy absorbed by the surrounding area by focusing the beam onto the location chosen for examination.

After reviewing the provided electronic assembly, the EMPF was able to quickly determine if the assembly process incorporated a SnPb solder by examining the solder joints and fiducials on the assembly. Figure 2-1 represents a solder joint on the electronic assembly while Figure 2-2 represents solder on the fiducial. The fiducial was examined for base line testing. Pb is the peak at approximately 10 keV and Sn is the peak at approximately 25 keV.

The customer was given the captured images in a one day turnaround and was able to discuss with their third party EMS provider the issues with their manufacturing processes.

In conclusion, XRF testing indicated that lead (Pb) was found in the solder joint of this product. The use of lead (Pb) demonstrates this electronic assembly's non-compliance with RoHS.

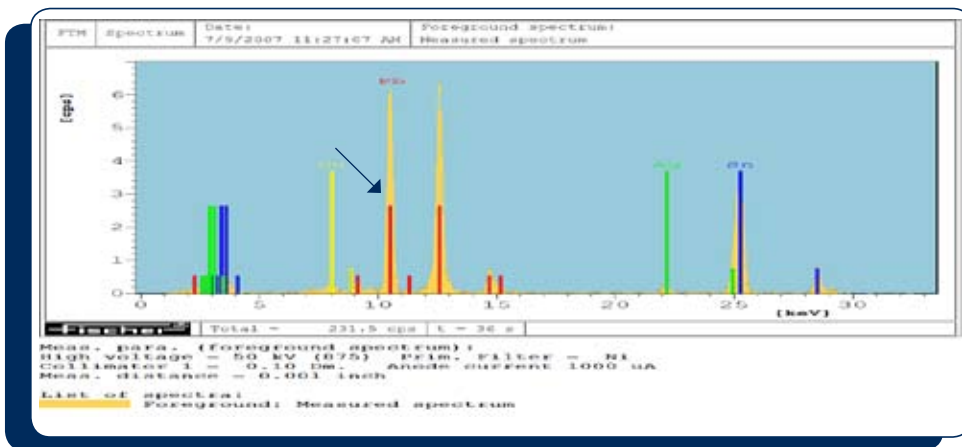


Figure 2-1: Representative solder joint on electronic assembly showing Pb peak at 10 keV.

The recommended testing to be performed was X-ray Fluorescence (XRF) which has the capability to complete an elemental analysis without damaging the electronic assembly. XRF operates through the emission of characteristic secondary x-rays by exciting lower level electrons to “jump” out of their orbit into higher orbits. This change leaves the atom unstable resulting in higher level electrons dropping down to these lower level orbits while simultaneously emitting photons equal to the difference between the two orbitals involved. The energy radiated is characteristic of the element under testing which is observed by a detector. XRF can be used for RoHS compliance by verifying the elements in solder or on pads on the electronic assembly. There are limitations to XRF analysis. Lighter elements have less detection sensitivity and the possibility of x-ray absorption by the area surrounding the test location exists. In the case of Pb, which is a heavier element, sensitivity is not an issue. The particular XRF instrument used has

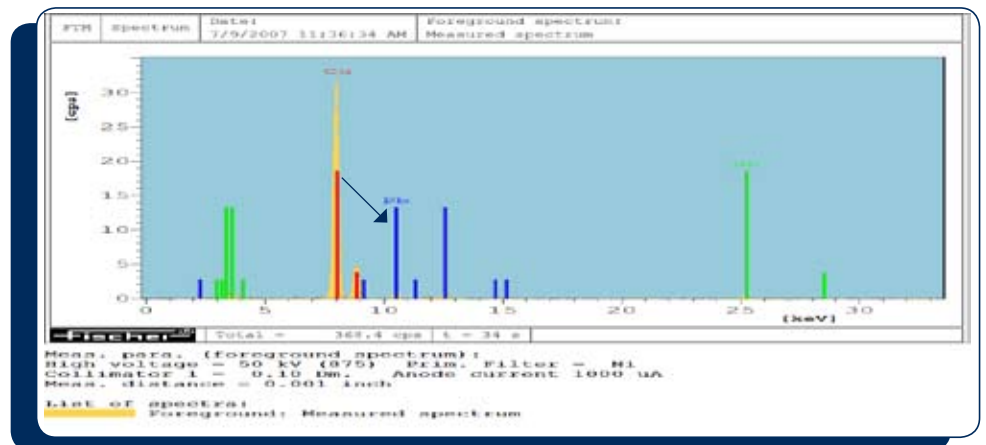


Figure 2-2: Solder on the fiducial on electronic assembly shows little Pb present at 10 keV.



Chris Deeble - Materials Engineer

# Designing Silicon Germanium System on a Chip (continued from page 1)

support reliability testing of the flip chip interconnect scheme. In order to limit costs, the SiGe fab runs were conducted sharing wafer real estate with other customers. These Multi-Project Wafers (MPW) were divided into 5mm x 5mm tiles enabling cost effective prototype runs. The tiles for this project were subsequently divided into 2.5mm x 2.5 mm test cells, 26 mils thick. Each test cell has four different architectures designed to test the various SiGe SoC devices. The test cells were designed with 3 mil pads and a 6-10 mil pitch.

## Mounting Substrates

The FCoB uses, in this application, low temperature co-fired ceramic (LTCC) “boards” to be used for reliability testing and RF testing of SiGe test cell flip-chips and eventually will be the mounting substrate on which the SoC will be mounted. The LTCC ceramic has excellent RF properties and is suitable for RF applications where the practical frequency range can be as high as 40 GHz or beyond. The pads and traces used on the LTCC substrates are fabricated using thick film gold.

## Packaging

Flip-chip packaging has many advantages in both cost and performance. High frequency RF components require low source impedances for both supplies and grounds. A comprehensive packaging study is being performed that evaluates the most suitable flip-chip interconnect technology for high-reliability RF applications. The study was designed to address the following areas in RF flip-chip packaging:

- Bumping technology
- Underfill material and process
- Environmental packaging
- Thermal expansion coefficient differences between SiGe die and the LTCC board.

Important to packaging design is the ability to create sufficient standoff height between the RF circuit and the ground plane on the substrate. This was needed to prevent RF field effects from affecting device performance. Based on computer models, a target of 3 to 5 mils was established for a minimum standoff height. One major goal of the SiGe SoC packaging study is to understand the effects of the board’s ground plane on the SiGe device’s RF performance.

A detailed test matrix was constructed that included multiple attachment methods and materials. Only materials and processes that were robust, RF compliant, and readily available were considered for inclusion in the test matrix. The attachment methods considered were gold stud bump bonding, solder bump attachment, and diamond particle interconnect. Each process has its advantages and disadvantages.

Solder bumps are reworkable; failed die can be replaced after

die removal, residual solder removal, fluxing and soldering of a new die. Solder bumps have a lower cost at high volume than stud bump bonding and uses standard soldering equipment; no thermal compression equipment required. Solder attachments also have a long history and demonstrated reliability and are well suited to high volume production. Solder bumps are not, however, well suited for fine pitch bond pads. They require fluxing, cleaning, and solderable under-bump metallization (UBM). Aluminum, standard pad metallization on SiGe die, is not a readily solderable surface, neither wettable nor bondable by most solders. Also, the cost of low-volume solder bump processing is more than the cost of low-volume stud-bumping. Gold wire stud bumping of flip-chip packages is a cost efficient and popular packaging option for many applications, particularly those with smaller pad and smaller pitch requirements. For the SiGe SoC application, stud bump bonding is a robust packaging option given the process restrictions that must be overcome. The EMPF, Boeing, and Palomar Technologies (Carlsbad, CA) have developed a gold wire stud bumping process compatible with the

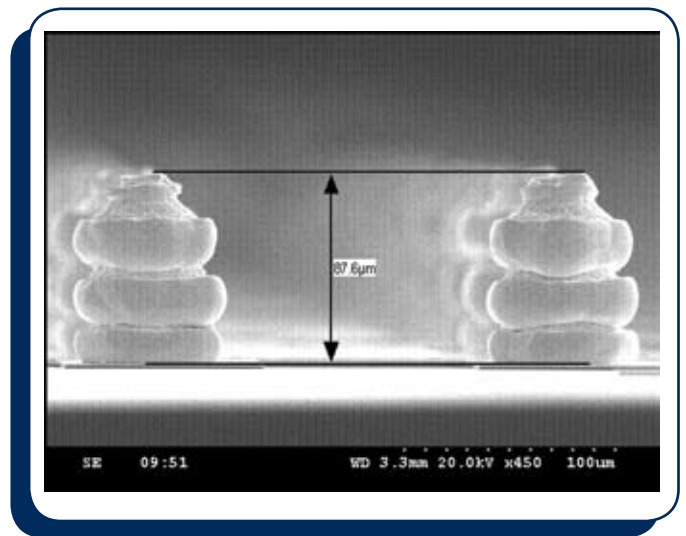


Figure 1-2 Triple stack stud bump

requirements of the SiGe SoC flip-chip application. The process involves the use of single and triple-stacked gold wire stud bumps formed with 1 mil gold wire in conjunction with conductive adhesive (Figure 1-2). The use of triple-stack bumps increases standoff height which helps mitigate some of the expected strain induced by the SiGe die and LTCC substrate.

Another packaging option that is being evaluated is the use of a single gold wire stud bump in conjunction with a novel connection technology called Particle Interconnect. Particle Interconnect utilizes sharp, metallized, diamond particles which have been screened by size. These particles are attached to substrate contact pads, under bump metallization or other conductor

continued on page 5

# Design of Experiment for Reflow Soldering in Inert Atmospheres

The EMPF is conducting a program to determine optimized gas mixtures for lead-free soldering. The experiment is aimed at enhancing the manufacturability of lead-free products manufactured using no-clean pastes, reflow ovens, and processing atmospheres used on the production line.

## Electronics Manufacturing of Test Samples

### Test Vehicle

The PCB assembly used throughout this experiment was a glass-epoxy (FR-4) substrate (P/N EMPF010, Figure 3-1) that was assembled using standard automated processing equipment. The test vehicle incorporates an industry standardized Surface Insulation Resistance (SIR), pattern within a convenient snap-off design. The test vehicle has flip chip features and SMT devices as well.

The IPC-B-36 Standard Test Board and Assembly is defined within the IPC-9201 Surface Insulation Resistance Handbook. (Often, IPC-A-36 is used to designate the artwork, and IPC-B-36 is used to designate the board.) This board design is an accepted test vehicle for MIL-STD-2000A and J-STD-001 and is also used in cleaning studies. For qualification, the substrate metallization is bare copper. The board has four isolated quadrants with top side interdigitated patterns that are routed to the edge card contacts through vias and circuitry on the bottom side of the board. There are ten surface insulation resistance (SIR) patterns on the board. There are four relatively large comb patterns that have 0.006 in. lines and spaces, and an area of 3500 squares. There are two patterns that utilize the SMT pads and have 0.025 inch spaces. There are also inner and outer perimeter patterns that have 0.006 inch lines and spaces referred to as Y-patterns. The PLCC28-TR-DC-Sn components placed on the SIR pattern and the 5 mil standoff height, presents a cleaning challenge.

For evaluation of a no-clean flux, the most important patterns are those on the SMT patterns. Flux is not expected to migrate to the comb pattern since there is no turbulent cleaning process. For evaluation of a cleaning process, particularly a water soluble flux, the low stand off height of the component poses a cleaning challenge and may cause entrapment of residues. The four large comb patterns are appropriate for this type of evaluation.

### Board Finish: ENIG versus OSP/Cu

Boards are being evaluated with electroless nickel followed by immersion gold (ENIG) plating and bare copper with an organic solder preservative (OSP) finish. The OSP finish approximates processes primarily used by users of quality gases, and since the surface is the most difficult to solder, these samples are expected to show differences within the range of the experimental design. IPC 9201 states that the contact fingers are normally gold plated for compatibility with edge card connectors. The remaining

metallization is normally bare copper or can be any other surface finish. Discussions with the IPC SIR committee have shed some light on the upcoming release of IPC 9201a, and they offered the following points:

- The B-36 board was originally designed to be bare copper because that was the cleanest finish back when the original work was conducted (circa 1988)
- J-STD-001 took a looser approach, allowing and encouraging the B-36 board to be closer to what was used in production.
- Since six mil lines and spaces have become routine, any of the plated finishes (ENIG, immersion tin/silver/PdAg), can be manufactured with good yield.
- OSP may provide an advantage since the copper etching can be controlled a little more precisely and has fewer plating steps than the other plated finishes. The uniformity on the tight 6 mil patterns might be slightly better.
- Lastly, the main suggestion by the committee was to approximate the process being used. If an ENIG board is being used in manufacturing, the SIR board should also have an ENIG finish.

## Manufacturing Equipment

A reflow oven processed the boards using five specific processing atmospheres that varied oxygen ( $O_2$ ) content. This allows a response surface plot to be created. The processing atmosphere oxygen content levels ranged from 100ppm to dry air. The partial pressure of oxygen was monitored from the reflow area in order to correlate for a given paste, the effects of  $O_2$  level and temperature on surface insulation resistance, wetting properties,

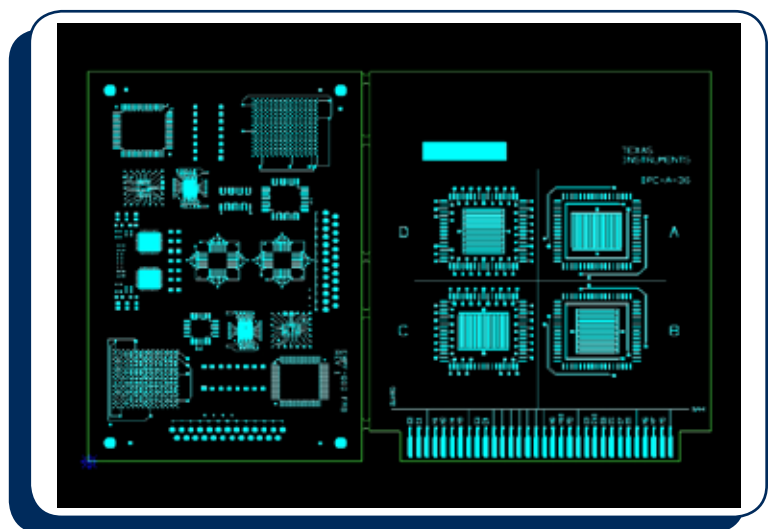


Figure 3-1: EMPF010 test board with IPC SIR patterns.

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# Designing Silicon Germanium System on a Chip (continued from page 3)

surfaces using a standard electroplating process. The contact areas are defined with masks or through the use of an interposer. The embedded particles are sharp and create a “microbed-of-nails” that makes many parallel electrical contacts. The particles penetrate through oxide or other thin contaminants to make contact without a wiping or scrubbing action that is required for many other conventional contacts. Gold-wire stud bumped die are attached to the substrate using the particle interconnect technology and flexible interposer. Particle Interconnect (PI) has been shown to provide RF bandwidth greater than 65 GHz and a lifetime of greater than 30,000 insertions. Detailed information about particle interconnect can be found in the November 2006 edition of EMPFasis.

Currently, test cells are being RF tested to ensure functionality prior to packaging the devices. The RF test results are compared to the computer generated models that were used in the test cell architecture design. Following packaging, these tests cells

and their various packaging methods will be environmentally tested.

## Conclusion

While this phase of the Silicon Germanium System on Chip project focuses on test cell design and packaging, many lessons are being learned about SiGe manufacturability, modeling, and electrical characteristics. Throughout the design, manufacture, testing and packaging operations, the EMPF is evaluating each process and material to evaluate a top performing, low-cost high-frequency solution.



Mark Allemang- Manager, Advanced Manufacturing Technology

# IPC-A-610 Acceptability of Electronic Assemblies

Course materials are now available for both Instructors/Trainers and Application Specialists for IPC-A-610 Acceptability of Electronic Assemblies (Revision D). The Certified IPC Trainer course covers the entire specification, while the Application Specialist course is now modular, offering companies the flexibility to select the areas of training which pertain to their specific needs. Following is a description of the courses, including requirements which must be met to obtain trainer and specialist certifications.

The Certified IPC Trainer course reviews the responsibilities of trainers and provides a thorough review of the entire specification. Students are tested on their knowledge of the specification by completing one open and one closed book exam. A minimum average score of 80% is required for certification (with a minimum single test score of 70%). Upon successful completion, students will be issued an IPC certification and the required course materials for certified IPC specialist training.

Modules 1 and 2 of the Application Specialist course review the introduction of the IPC Professional Policies and Procedures, the forward to the specification, documents applicable to the IPC-A-610, and handling of electronic assemblies (covering common ESD practices). These first two modules are a requirement for basic certification and for the remaining modules in the course. Students must pass an open and closed book exam. Students must score at least 60% on each exam and attain a minimum average

score of 70% (Duration: 2 hours).

The following are optional modules offered for the Application Specialist certification:

- Module 3: Hardware Installation
- Module 4: Soldering (including high voltage)
- Module 5: Terminal Connections
- Module 6: Through-hole Technology (including through-hole jumper wires)
- Module 7: Surface Mount Assemblies (including SMT jumper wires)
- Module 8: Component Damage and Printed Circuit Boards and Assemblies
- Module 9: Solderless Wire Wrap

(Modules 4 and 8 are prerequisites for Modules 5, 6, and 7.)

Module 3 covers hardware installation. Upon completion of this module, students will be able to recognize and identify acceptable mechanical assembly requirements. This two-hour module covers the following:

- Hardware installation
- Connectors, handles, extractors, and latches
- Connector pins
- Wire bundle securing
- Routing

continued on page 6

# IPC-A-610 Acceptability of Electronic Assemblies (continued from page 5)

Module 4 is a two-hour course which covers the requirements for soldered connections of all types, including high voltage soldering. This module is optional and is a prerequisite for Modules 5, 6, and 7 (Terminal Connections, Through-hole Technology, and Surface Mount Assemblies). The following topics are reviewed:

- Soldering acceptability criteria
- Soldering anomalies
- High voltage soldering

Module 5 reviews terminal connections. Students will gain knowledge of acceptance criteria relating to all terminal connections. This three-hour module covers the following:

- Edge clips
- Swaged hardware
- Wire/lead preparation and tinning
- Lead forming – stress relief
- Service loops
- Stress relief lead/wire bend
- Lead and wire placement
- Insulation
- Conductor
- Terminals – solder
- Conductor damage – post-solder

Through-hole technology is covered in Module 6. This three-hour section addresses acceptance criteria for hardware, adhesive, forming, mounting termination, and soldering criteria for supported and unsupported holes. The following topics are covered:

- Component mounting
- Heatsinks
- Component securing
- Component positioning
- Lead clinching
- Solder quantity
- Jumper wires

Module 7 reviews surface mount technology criteria for the most commonly used surface mount devices. Revision D includes the addition of plastic quad flat packs – no leads and components with bottom thermal plane terminations (Duration: 4 hours). The following topics relating to a variety of surface mount devices are covered:

- Staking adhesive
- Solder connections
- Jumper wires

Module 8 (Component Damage and Printed Circuit Boards

and Assemblies) is a prerequisite for Terminal Connections, Through-hole Technology, and Surface Mount Assemblies. This two-hour module combines several sections of the IPC-A-610 Specification. The following areas are covered:

- Gold fingers
- Laminate conditions
- Marking
- Cleanliness
- Conformal coating/solder resist

Module 9 (two hours) reviews the acceptance criteria for solderless wire wrap. The following topics are reviewed:

- Number of turns
- Turn spacing
- End tails, insulation wrap
- Raised turns overlap
- Connection position
- Wire dress
- Wire slack
- Wire plating
- Damaged insulation
- Damaged conductors and terminals

The total duration of the course for the Certified IPC Trainer (CIT) is four days (32 hours). The duration for the Application Specialist course will vary depending on the modules selected. The hours listed in this article are the minimum time requirements. Application Specialists are required to pass an open book exam for each module selected in order to obtain certification in those selected areas. Upon successful completion of the training session, the Application Specialist certificate will now indicate which modules the participant completed. Certification is valid for two years for both trainers and specialists.

Please contact the EMPF Helpline at (610) 362-1320 for more information about IPC-A-610 or to register for upcoming courses.

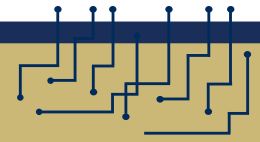


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## Black Pad

Assemblies manufactured with Electroless Nickel Immersion Gold (ENIG) plated PCBs and components can succumb to a failure mode known as “Black Pad”. Black Pad is a corrosion of the Ni layer during the immersion gold step. The end result can vary with complete de-wetting of the pad/component surface, to suitable wetting with weakened solder joints (that do not often reveal themselves until later in the field). As a result, routine IPC 610 inspection efforts are not sufficient for Black Pad screening.

There is some difference of opinion as to the Black Pad mechanism.<sup>1,2,3,4,5</sup> The end result is clear, with either weakened solder joints or complete solder separation at the interface between either the solder and pad or solder and lead. The characteristic of a Black Pad failure, as the name states, is a blackened appearance of the pad surface. As a result of the variation in the failure mode, the following is a list of characteristics that should collectively be observed to be considered a true Black Pad failure.

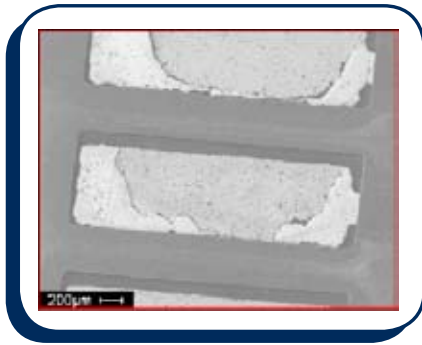


Figure 4-1 Solder joint fracture and SEM/EDS analysis

1. The fracture will occur at the interface and not within the bulk solder as indicated by the presence of Ni-Sn intermetallic compound (IMC) at the fracture interface (Figure 4-1).

2. High levels of phosphorus at the fracture interface as indicated in Figure 4-2 (in which the P content was 28.25%). It is known that at the IMC region, P levels do become naturally enriched. In Black Pad, however, the Ni corrodes as a result of increased activity of the immersion gold step. This hyperactive immersion gold step is induced by pH, solder mask contamination, and the electric fields on the board. The last affect can cause particular pads or regions on a pad to be selectively effected.



Figure 4-2 SEM image of a BGA ball fracture

3. Nickel on the surface of the PCB

pad is another indicator of Black Pad. Nickel corrosion is detected through Auger Spectroscopy.

4. Mud cracks at the fracture interface and a lack of Ni-Sn IMC compound as a result of the Ni being tied up as Ni-P compound. Figure 4-3 displays the “mud crack” appearance with very little Sn present at the fracture interface.

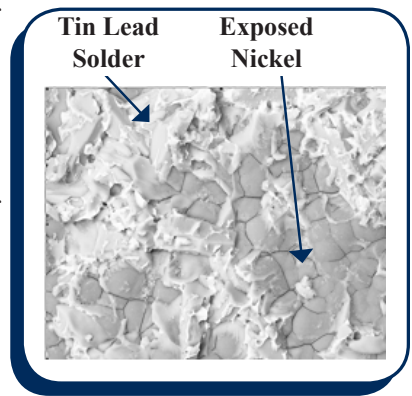


Figure 4-3: High resolution SEM image indicating black pad.

The difficulty in establishing a black pad mechanism stems from how the degree of Ni corrosion will influence what is observed. Figure 4-4 displays ENIG pads in which Ni corrosion was induced. (Note, the Au was removed by a cyanide etch). As result, a Black Pad failure may not be established, only that the Ni became corroded.

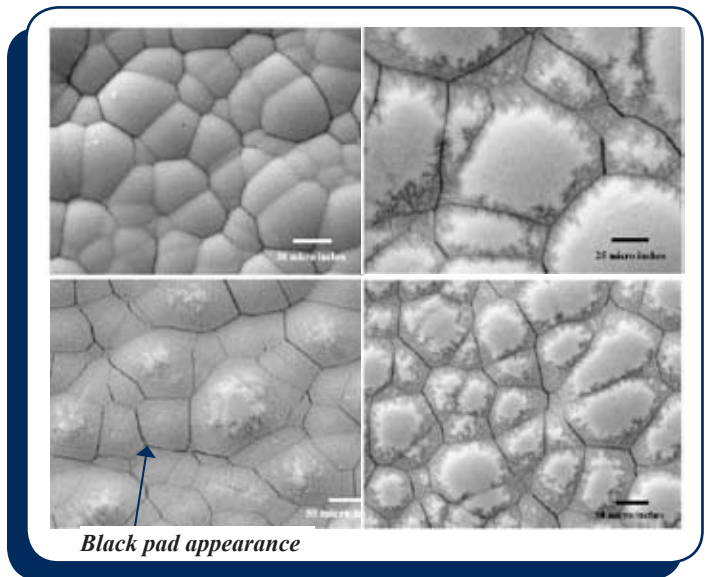


Figure 4-4: Progressive clockwise images of ENIG PCB pads treated to induce Ni corrosion



Sam Pepe- Chemist

- 1 <http://www.circuitsassembly.com/pdf/0301/0301raytheon.pdf>
- 2 <http://www.pwbr.org/members/pdf/works99/Houghton.PDF>
- 3 [http://www.sanmina-sci.com/Solutions/pdfs/pcbres/Blackpad\\_on\\_ENIG\\_Surface\\_Finishes.pdf](http://www.sanmina-sci.com/Solutions/pdfs/pcbres/Blackpad_on_ENIG_Surface_Finishes.pdf)
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# Manufacturer's Corner: Dispensing Equipment

**H**enkel is a market leader with brands and technologies that are present in many industry segments and carry very recognizable names. Henkel products can be found in industries such as laundry and home care, beauty and personal care, industrial sealants, surface treatments, and adhesives. Some of the recognizable brand names from Henkel are Purex, Renuzit, Soft Scrub, Right Guard, Dial and the industrial adhesive brand, Loctite.

The Loctite 300 series bench top robot (Figure 6-1) simplifies the dispensing of adhesives and sealants onto complex surface configurations, such as circuit boards and assemblies. This system allows the users to repeatedly and reliably dispense patterns of liquid material on a programmed basis resulting in

The Loctite 300 Series Bench top robot has a 300 x 320 mm (11.8" x 12.6") range of operation. There are 8 possible configurations of the system which can offer 3 or 4 axes. The simultaneous control over all axes provides for 3-dimensional linear arc interpolations that are required for complicated dispensing processes.

Programming the robot for specific functions and applications is not complicated with special user assist software. It operates in a Microsoft Windows environment and uses basic question and answer prompts for set up and application programming. The Q&A prompts are part of Henkel's teach-point programming and comes with 100 pre-set programs and a 6,000 point memory card.

There are other accessories from Loctite which are used in conjunction with the 300 series robot, such as bottle reservoirs, automatic dispense valves, diaphragm valves, and advancing slides. Loctite adhesive dispensing equipment is capable of dispensing and spraying a wide variety of adhesive sealant such as acrylic, anaerobic, cyanoacrylate, epoxy, hot melt, silicone, urethane, and other types of rapid bond adhesives.

There are two common types of curing devices associated with this robotic system. A hand held UV wand and portable bench top UV curing chamber. Both curing methods are available for demonstration at the EMPF.

The Loctite 300 series robotic dispensing system is designed to simplify and automate adhesive dispensing onto complex surfaces. This system is recommended for high precision and repeatable dispensing of a wide range of adhesive products, leading to improved process efficiencies and lower overall manufacturing costs

For more information related to this article, or to schedule a demonstration of the Henkel/Loctite 300 series robot located at the EMPF, contact Ken Friedman, 610-362-1200 x 279 or via email at [kfriedman@aciusa.org](mailto:kfriedman@aciusa.org).



Figure 6-1: The Loctite 300 Robotic Dispensing System.

improved process efficiencies, minimal material waste, and reduced overall production costs.

Bench top robots are beam or gantry style units designed specifically for bench top operation. These robots carry one or more parts that are captured in a fixture which is mounted on the work surface. Motion in the X axis is achieved by moving the work surface forward and backward. The Y and Z axis is achieved by moving the tool head or dispensing apparatus left and right as well as up and down respectively on the beam or gantry.



Ken Friedman - EAB Coordinator

# Design of Experiment for Reflow Soldering in Inert Atmospheres (continued from page 4)

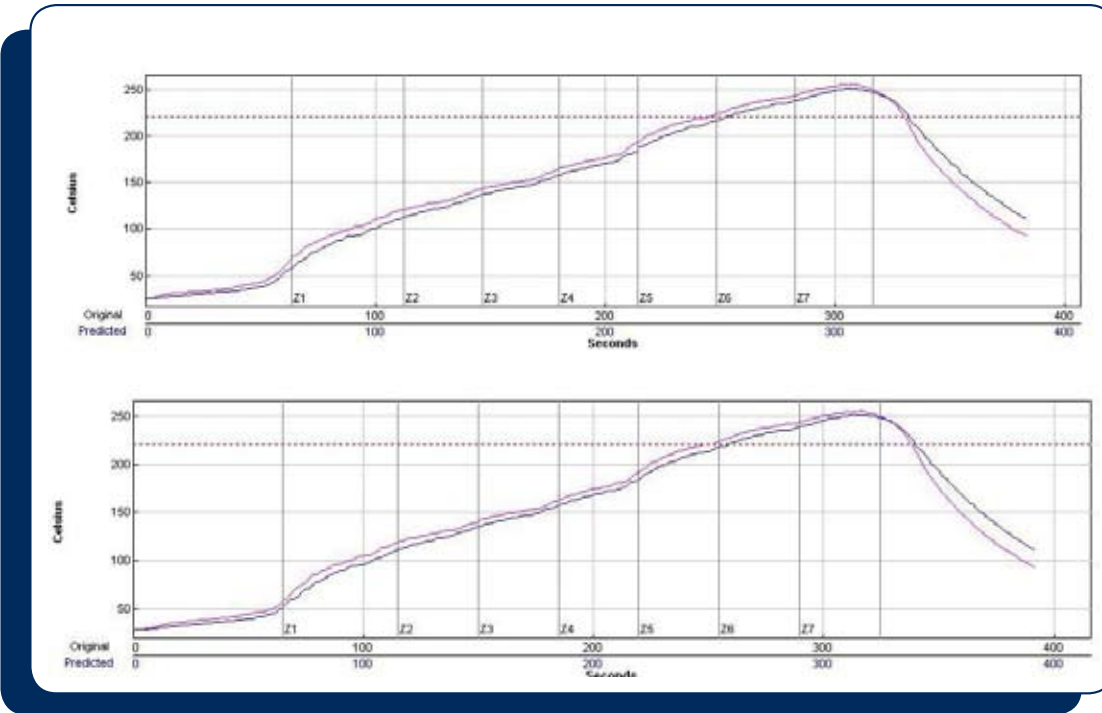


Figure 3-2 Profiles for air (above) and nitrogen (below).

visual appearance, and cleanliness. The oven has manual flow meters that control the main gas input and an Air Doping Leak Valve to control the oxygen ppm-levels. The gas flow rates for each of the zones were set for zones 1-6 at 130, 70, 100, 180, 80, and 50 liters per minute (LPM) respectively. The highest flow rate was in the reflow zone.

The external liquid nitrogen source pressure was increased in order to increase the flow rate through the oven. The main pressure was regulated at the machine to 80 psi. The pressure entering the oven was 60 psi, to overcome the back pressure, the nitrogen for the air doping was regulated to 70 psi. The external nitrogen tank was monitored so that its capacity was not depleted.

A Samsung SM3320 pick and place machine was used to accurately and quickly assemble the boards. Three types of Pb-free no-clean solder pastes were used, and a no-clean tacky flux was also used with the flip-chip components.

## Reflow

A typical reflow profile has an initial ramp, a soak, a spike to reflow, a reflow period, and a cool down zone. Profiles are classified either as a soak profile, where the assembly is subjected to the same temperature for a period of time, or as a continuous ramp profile where the temperature is steadily ramped. The melting point for SAC305 (Tin 96.5%, Silver

3.0%, Copper 0.5%) solder is 217°C, and the time above reflow (TAF) is referenced from there. Figure 3-2 shows an example of one of the profiles used. It shows that there is not much difference in peak temperatures between the air (above) and nitrogen (below) runs (nitrogen peaked about 1 degree lower on all settings).

## Preliminary Results

A battery of tests is being conducted to examine wetting characteristics, solder voiding levels, and relationships between the surface insulation resistances. Preliminary results show there are benefits to using specialty gas mixtures for solder reflow of lead-free components; the final results will quantify the process

windows for obtaining maximum benefits. For more information on how specialty gas mixtures may be used in an electronics manufacturing environment, please contact the EMPF.



Anthony Vigliotti - Senior Materials Engineer

## Soldering Skills Kits

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Modification of  
Electronic  
Assemblies

2007

IPC-7711/7721  
CIT Certification

January 29-February 2  
March..... 5-9  
May..... 7-11  
July ..... 9-13  
September..... 24-28  
November..... 26-30

2007

IPC-7711/7721  
CIT Recertification

February..... 20-21  
April..... 4-5  
June..... 25-26  
September..... 4-5  
November..... 15-16  
December ..... 3-4

Call the EMPF  
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610-362-1320  
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## Electronics Manufacturing

### Boot Camp A

January 29-February 2  
April 16-20  
June 4-8  
September 10-14  
November 5-9

### Boot Camp B

February 5-9  
April 23-27  
June 11-15  
September 17-21  
November 12-16

## IPC Certifications CIT/Instructor

### IPC J-STD-001

January 8-12  
February 12-16  
March 12-16  
April 9-13  
May 21-25  
June 18-22  
July 16-20  
August 20-24  
September 24-28  
October 22-26  
December 10-14

### IPC-A-610

January 22-26  
February 26-March 2  
April 16-20  
May 14-18  
June 11-15  
July 23-27  
August 13-17  
September 17-21  
October 15-19  
November 5-9  
December 3-7

### IPC-A-600 PWB

Acceptability  
January 3-5  
February 27-March 1  
April 9-11  
May 29-31  
July 31-August 2  
August 27-29  
October 10-12  
November 19-21

### IPC-A-610 Recertification

January 16-17  
February 20-21  
March 19-20  
April 23-24  
May 14-15  
June 4-5  
July 16-17  
August 20-21  
September 10-11  
October 29-30  
December 10-11

### IPC J-STD-001 Recertification

January 17-18  
February 21-22  
March 21-22  
April 25-26  
May 16-17  
June 6-7  
July 18-19  
August 22-23  
September 12-13  
October 31-November 1  
December 5-6

## CIS/Operator

### IPC/WHMA-A-620

Wire Harness  
Manufacturing  
March 13-15  
June 26-28  
October 2-4  
December 17-19

### SMT Rework & Circuit Repair IPC-7711/7721

(Modules 1 & 4-7)  
February 12-15  
May 7-10  
August 13-16  
October 29-Nov. 1

### SMT Rework/ IPC-7711

(Modules 1, 4-6)  
February 12-14  
May 7-9  
August 13-15  
October 29-31

### Surface Mount & Thru-Hole Rework of Electronic Assemblies IPC-7711 (Modules 1 & 3-6)

March 19-22  
July 30-August 2  
October 8-11

### Repair & Modifications of PCB's IPC-7721 (Modules 1 & 7-9)

February 5-8  
April 30-May 3  
August 6-9  
November 12-15

### Circuit Repair IPC-7721

(Modules 1 & 7)  
February 5-6  
April 30-May 1  
August 6-7  
November 12-13

### IPC Challenge

January 19  
February 23  
March 23  
April 27  
May 18  
June 8  
July 20  
August 24  
September 14  
November 2  
December 7

## Skills

### Chip Scale Manufacturing

March 28-30  
June 20-22  
October 22-24

### BGA Manufacturing Inspection & Rework

January 18-19  
April 3-4  
June 18-19  
July 23-24  
August 29-30  
October 15-16  
November 26-27

## Continuing Professional Advancement in Electronics Manufacturing

### Lead Free Manufacturing

January 16-17  
February 26-27  
March 26-27  
April 30-May 1  
May 30-31  
June 27-28  
July 25-26  
August 27-28  
October 17-18  
November 19-20  
December 12-13

### Design for Manufacturability

February 22-23  
April 11-12  
May 24-25  
August 6-7  
October 8-9

### Failure Analysis and Reliability Testing

January 3-5  
March 6-8  
May 21-23  
July 9-11  
September 5-7  
November 28-30

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