

American Competitiveness Institute

**ISO 9001-2000  
Certified**

American Competitiveness Institute  
One International Plaza  
Suite 600  
Philadelphia, PA 19113  
(610) 362-1200 • FAX: (610) 362-1290  
HELPLINE: (610) 362-1320  
WEBSITE: www.empf.org  
www.aciusa.org

The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government center and laboratories in the U.S.

**Technical Editor**

Michael D. Frederickson,  
EMPF Director

Please direct comments  
and/or questions to the Editor at  
empfasis-editor@aciusa.org

610-362-1336  
In this Issue

- Page 1: Package on Package Manufacturing
- Page 2: Ask the EMPF Helpline!
- Page 4: Clean Room Requirements for Advanced Packaging
- Page 6: High Quality/High Reliability Soldering
- Page 7: Tech Tips... Temperature Profiling for Advanced Packages
- Page 8: Manufacturer's Corner: Thermal Profiling - KIC
- Back Cvr: Training Center Course Schedule



**Industrial Advisory Board**

- Gerald R. Aschoff, The Boeing Company
- Dennis M. Kox, Raytheon
- Gregory X. Krieger, BAE Systems
- Edward A. Morris, Lockheed Martin
- Jack R. Harris, Rockwell Collins
- Gary Kirchner, Honeywell
- Andrew Paradise, Northrop Grumman
- Art Smedberg, ITT Industries, Avionics Division

## Package on Package Manufacturing

Miniaturization has driven the design of logic and memory integration using vertically integrated devices in a stacked configuration, where the top and bottom BGAs are mated to form Package

in the concurrent processing of both the top and bottom BGAs. This approach to assembling POP BGAs utilizes a conventional paste process for the bottom BGA and a flux transfer dip for the top BGA. The top side of the bottom BGA, where the pads are typically a plated NiAu finish, provides a wettable surface pad area for the top BGA. The reflow process employed will depend largely on the composition of the solder paste, and the top and bottom BGA alloy. In situations where the paste alloy and BGA balls are of varying compositions, the reflow parameters should be adjusted to achieve the liquidus temperature of the higher melt alloy.

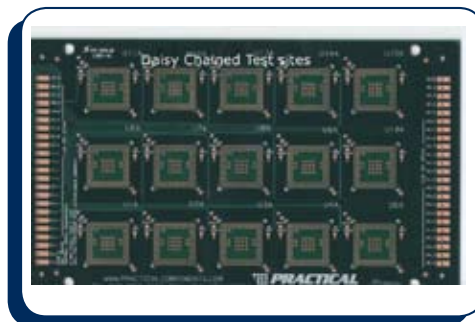


Figure 1-1: The POP PCBs used for the experiment

on Package (POP) assemblies (Figure 1-1). The advantages of such a design, beyond the reduction of the packaging footprint, is to incorporate functionality and cost benefits for electronic products, such as cell phones, PDAs digital cameras, and other handheld devices. The intrepid nature of this technology has spread beyond the package realm, spawning new stacked die and SOC (System on Chip) technologies that integrate a similar vertical stacking approach, while retaining the needed functionality associated with more conventional designs.

The advantages of the POP architecture are such that one step reflow can be utilized

For the purpose of exploring various process options, the EMPF is conducting an experiment which will eventually produce thermal cycling reliability data on POP assemblies. Utilizing a mixed and all lead-free SAC 305 solder composition

Manufacturing Process	# of assemblies	# of test sites	Solder sets	Underfill
1	25	375	SAC 305 BGA – SAC 305 Paste	None
2	25	375	SAC 305 BGA – Sn63/Pb37 Paste	None
3	13	195	SAC 305 BGA – SAC 305 Paste	Bottom BGA
4	13	195	SAC 305 BGA – Sn63/Pb37 Paste	Bottom BGA
5	12	180	SAC 305 BGA – SAC 305 Paste	Top and Bottom BGA
6	12	180	SAC 305 BGA – Sn63/Pb37 Paste	Top and Bottom BGA
7	6	90	SAC 305 BGA – SAC 305 Paste	Bottom BGA
8	6	90	SAC 305 BGA – SAC 305 Paste	Bottom BGA

Table 1-2 Experimental Matrix

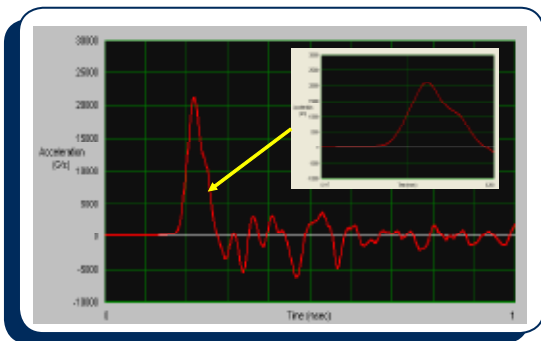
continued on page 3

# Ask the EMPF Helpline!

*A customer called the Helpline with a question regarding the available tests for an electronics package that would be subjected to a high shock environment, such as a gun launch...*

The customer wanted to conduct a series of tests to validate their package design and manufacturing processes. There is no single high-g test that can replicate the dynamics of a gun launch, which makes qualification of electronic components or hardware challenging. Two different types of launchers, which have nominally the same peak force, can produce significantly different effects on the projectile.

Commonly used high-g shock testing methods, such as centrifuge testing and high-g drop testing, have been used by a handful of test laboratories and companies. The actual gun shock tests, such as the Ballistic Rail Gun (BRG) test and Soft Recovery Vehicle (SRV) Test, can only be done at a limited number of military facilities. All these test methods have their pros and cons. As a general rule of thumb, the laboratory based tests are significantly less expensive than gun launch tests at military facilities. However, the laboratory tests do not simulate a gun launch environment as well as the actual gun shock tests. Depending on the application requirements, the design engineers can choose a special high-g test, or a combination of high-g tests, to perform an initial screening or a complete qualification program on the test articles.



*Figure 3-1: A typical shock pulse used by the EMPF in a previous Navy ManTech high-g packaging program*

Drop testing has been used by many companies to evaluate the effect of high-g impact on test articles. This test can produce g-levels as high as 100,000g with very short pulse durations. The g-force level is determined by the drop height and it is sometimes influenced by the secondary returning force. The primary advantages are availability, cost, and ease of test. For example, the high-g drop tester at the EMPF can simulate g-forces up to a 25,000g acceleration with less than 0.5 msec pulse duration (depending on the acceleration level).

After several detailed discussions with the customer, the EMPF developed a suitable test plan. In this particular case, a series of samples per the customer's requests and specifications were analyzed using an in-house drop tester. Since the articles to be

tested vary considerably in size and shape, the EMPF engineers worked closely with the customer to design and build the test fixtures.

During testing, the EMPF provided high-g drop test data in the form of shock pulse curves, and also provided the digitized test data in an Excel data format. Figure 3-1 shows a typical shock pulse generated by the drop equipment.

Typically, the EMPF integrates high-g testing capabilities as part of a comprehensive environmental test program that includes pre-conditioning tests, accelerated aging tests, environmental tests, high impact shock tests, post high-g evaluation and examination tests, electrical tests, failure analysis, statistical data analysis, and manufacturing design and process recommendations. The failure analysis may include X-ray examination, cross-sectioning, optical microscopy, and scanning electron microscope analysis, temperature cycling, etc. In addition to determining the areas requiring additional structural reinforcement, more than thirty (30) different types of electrical failures have been observed. These failures include:

- Internal failures within discrete crystal oscillator packages
- Wirebond failure due to inadequate pull strength
- Solder pad lift-off
- Improper or inadequate underfill for BGA packaged devices
- Cracked capacitors
- Improper elastomers
- Circuit conductor breaks due to poor adhesion
- Improper encapsulation materials
- Poor adhesion due to inadequate cleaning or surface preparation

These tests can be used to verify that an electronics module meets the design specification, or that additional design work is needed to improve the quality of the tested modules and to assist the product insertion process into a high shock systems application.



Charlene Yao - Senior Materials Engineer

# Package on Package Manufacturing (continued from page 1)

(Sn96.5Ag3.0Cu0.5), the experimental matrix will also be designed to include assemblies that will be underfilled, along with the more conventional approach of non-underfilled POP assemblies. The underfilled POPs will be further divided into bottom package only underfill, and top and bottom underfill. Typically, most POP architectures that integrate underfill as part of their process, underfill only the bottom package.

Process Steps	Manufacturing Process							
	1	2	3	4	5	6	7	8
Stencil Printing	X	X	X	X	X	X	X	X
Bottom BGA Placement	X	X	X	X	X	X	X	X
Oven Reflow			X	X	X	X		
Underfill Bottom			X	X	X	X		
Cure Underfill			X	X	X	X		
Apply Tacky flux	X	X	X	X	X	X	X	X
Top BGA Placement	X	X	X	X	X	X	X	X
X-ray verification	X	X	X	X	X	X	X	X
Oven reflow	X	X	X	X	X	X	X	X
Underfill Bottom							X	X
Underfill Top					X	X		
Cure Underfill					X	X	X	X
X-Ray verification	X	X	X	X	X	X	X	X
Electrical Test	X	X	X	X	X	X	X	X

Table 1-3 Manufacturing Process Matrix

free reflow temperatures. The solder pastes were composed of no clean flux and solder balls with a particle mesh of 300. The material used for underfilling was a high temperature, low CTE polymer, usually consigned for flip chip applications and ESS (Environmental Stress Screening) conditions where CTE is critical. The set of materials is listed below.

Solder Paste and Underfills used for the experiment:

<b>SnPb</b>	Multicore MP200 No clean Solder Paste
<b>SAC 305</b>	Multicore LF320 – No clean
<b>Underfill</b>	Hysol FP 4548FC

The test vehicle for POP processing included a daisy chained PCB with an OSP (organic solderability preservative) coating, and top and bottom BGAs composed of SAC 305 alloys. The Bottom BGA utilized a top pad finish of Au/Ni. The vehicle contained 15 independent daisy chain sites where the top and

One of the potential outcomes of the experiment the EMPF was commissioned to produce was an attempt at differentiation in reliability under thermal cycling conditions. The experiment was designed to use various materials and processes that would be encountered in the manufacturing of POPs. The materials of choice were selected for their ability to withstand Pb

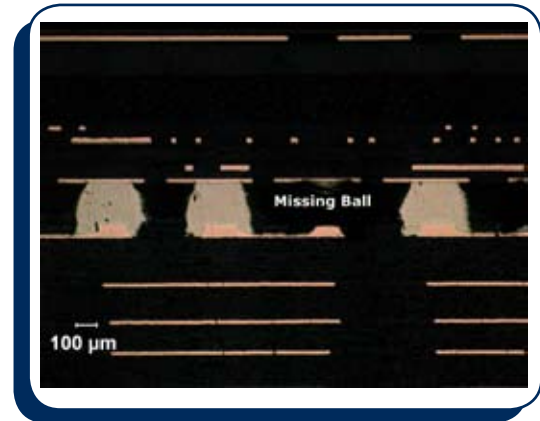


Figure 1-4: BGA photo showing missing ball

bottom BGAs continuity could be tested for open circuits while isolating the particular location and BGA on the PCB.

**PCB200 -OSP** A Daisy chained printed circuit board with an OSP coating.

**Top Package –A-FBGA 152.** A 152 ball BGA with 0.65 mm pitch on a 14 mm square package footprint. The balls are comprised of SAC 305 solder.

**Bottom Package – A-PSvFBGA353** a 353 ball count with 0.5 mm pitch on a 14 mm square package footprint. The balls are comprised of SAC 305 solder.

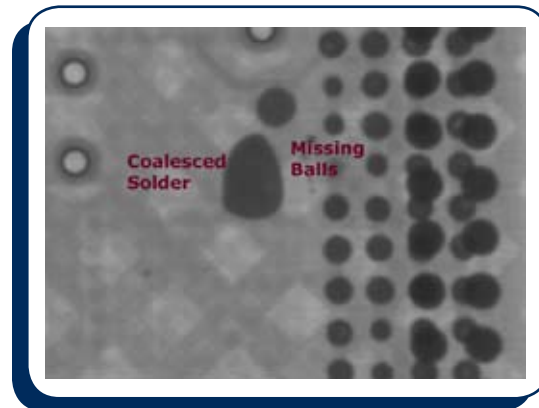


Figure 1-5 X-ray showing solder displacement

## Fixtures

The screen stencil for the solder paste was designed to apply a suitable amount of paste to obtain adequate wetting and contact between the BGA and substrate. A flux transfer

plate was utilized for assembling the top BGA to the top pads of the bottom BGA. The tacky flux was appropriate for Lead-Free processing and used the flux transfer plate as a shallow reservoir designed to hold a volume of flux that comprised 1/2 the diameter of the top BGA balls. The dimensions are below:

- **Top BGA- Screen printing Stencil** at a thickness of about 0.12 mm with an opening of 0.28 mm.
- **Bottom BGA Application - Flux transfer Plate** machined to a depth of 1/2 ball diameter, approximately 0.150 mm height.

continued on page 5

# Clean Room Requirements for Advanced Packaging

The term clean room has many implications. There are levels of cleanliness which are associated with classes of clean rooms. Class 1 is associated with integrated circuit manufacturing and Class 2 is where many disk drive manufacturing plants operate. Classes 3-5 are associated with assembly operations. Most standard semiconductor packaging occurs in a class 5 environment. However, a class 3 or 4 cleanroom area can exist within a class 5 environment by design. But what defines whether a room is classified as clean?

The first definition of a clean room came from the United States Government. Federal standard 209 states the following:

*“A Clean Room is an enclosed area employing control over the particulate matter in air with temperature, humidity and pressure control as required. To meet the requirements of a ‘Clean Room’ as defined by this standard, all Clean Rooms must not exceed a particulate count as specified in the air cleanliness class.”*

This standard, first issued in 1963, was revised in 1966 (A), 1973 (B), 1987 (C), 1988 (D), 1992(E), and was withdrawn in 2001. In 1992, The American National Standards Institute (ANSI) petitioned ISO to form a committee to develop international standards for facilities, equipment, operational methods, and establish limits on contamination. Formally commissioned in May 1993 as ISO TC 209, this committee established working groups (1-9) that developed the specifications for cleanroom particle contamination standards (1), testing standards (2), construction standards (4) and operation standards (5). Today ISO 14644-X (where x=1 to 9) contain these standards. Table X-1 shows the ISO classification and the number of allowable particles of a particular size.

The Federal and ISO regulations do not indicate what environmental, product, or facility parameters to control. The regulations only provide the standards a company must meet after it decides to build products in the cleanroom.

Examination of this issue has revealed an interesting challenge. A cleanroom is defined by a specification written to control specific parameters, such as air quality, temperature, or humidity. The term “monitored” requires a measurement of the controlled parameter on a regular basis, and “certification” is a process to verify that the parameters are under control.

By contrast, a controlled environment is defined as a working area that primarily controls physical, chemical, or biological variables. Although a controlled environment is similar to a cleanroom in that it is controlled and monitored, a controlled environment is not certified. Moreover, it is not subject to ISO cleanroom requirements for construction and operation. Given that a controlled environment is a cleanroom, but a cleanroom is not a controlled environment why would anyone build a cleanroom?

The answer is not always straightforward, and companies must weigh the decision carefully before deciding what path to follow. Although there are no hard and fast rules for what class of cleanroom is needed to package electronics, a generally good business practice, is to produce the products in the same class as your competition. Most standard packaging is performed in class 100,000 clean rooms, and by all accounts this works very well. However, for some devices such as very fine pitch flip chips and charge coupled devices (CCDs), a class 10,000 or 1000 room may be a better choice.

Within any class of cleanroom there can exist “cleaner areas” though use of laminar flow hoods, or by adding more HEPA filters to create islands of higher quality where specific operations take place.

The following guidelines and work practices can help limit the spread of particulate contamination, and can have a dramatic effect on particulate generation.

Things you should not bring into a cleanroom:

- Non-cleanroom paper
- Non-cleanroom wipes such as paper towels
- Pencils or non-cleanroom pens
- Makeup (should be removed)

Class	Number of Particles per Cubic Meter by Micrometer Size					
	0.1 um	0.2 um	0.3 um	0.5 um	1 um	5 um
ISO 1	10	2				
ISO 2	100	24	10	4		
ISO 3	1,000	237	102	35	8	
ISO 4	10,000	2,370	1,020	352	83	
ISO 5	100,000	23,700	10,200	3,520	832	29
ISO 6	1,000,000	237,000	102,000	35,200	8,320	293
ISO 7				352,000	83,200	2,930
ISO 8				3,520,000	832,000	29,300
ISO 9				35,200,000	8,320,000	293,000

Figure 1-1 ISO class and allowable particulate contamination levels

continued on page 9

# Package on Package Manufacturing (continued from page 3)

## Experimental Matrix

Table 1-2 illustrates how the 112 assemblies processed for the experiment were segregated and what manufacturing process and materials were chosen for each.

## Manufacturing process

The assembly process identified in the manufacturing process matrix (Table 1-3) with an “X” indicates the operation has been performed for the specific manufacturing process. As an example, the yellow shading highlights the manufacturing differences, specifically where the underfilling process was concerned. The underfilling for manufacturing process “3-6”, incorporated a two step reflow that allowed the bottom package underfill to reflow after the top package assembly. The manufacturing process “7-8”, underfilled the bottom package after the assembly of both top and bottom packages.

## Some initial results:

## Processing Issues

Data collected thus far indicates that any reoccurring failures are attributed to missing solder balls. When this issue was discovered, particular attention was given to the inspection of the BGA's for missing solder balls, so the packages that had dislodged balls were separated. Even after the segregation process, and subsequent step by step inspection, opens were occurring occasionally on different sites due to missing balls. A particular concern during the processing of POP assemblies, is the propensity of package warpage that would result in open solder joints, particularly in the bottom BGA. Co-planarity of the bottom package against the substrate becomes an issue as the corner edges of the BGA warp in a concave manner causing loss of contact between the BGA ball and substrate. This was also discovered in previous studies.

Figure 1-5 illustrates where a solder ball had dislodged itself sometime during the reflow processes.

In some cases, as the X-ray in Figure 1-5 illustrates, the solder ball displaces itself as the liquidus

stage is reached and coalesces in other areas. This occurs prior to the underfilling stage, even if the underfill is subjected to the reflow process. Once the underfill is cured, especially one

formulated with high filler content, the cross linked polymer would prevent the solder from wicking into adjacent areas, since it would be restrained by the underfill.

## Wetting

In the majority of the cases where the package sites have continuity, good wetting is evident even among the assemblies utilizing a mixed solder system and a two step reflow process. Figure 1-6 shows an example of good wetting to the substrate and BGA package. Inspection of POP assemblies for opens and shorts utilizing X-Ray techniques presents a bit of a challenge, since the staggered patterns of the top and bottom BGAs can potentially mask defects, or give a false negative reading due to its unusual appearance.

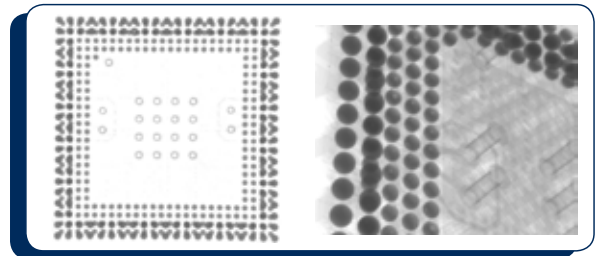


Figure 1-7: Normal & Oblique angle X-ray views of a BGA

It is sometimes necessary to view the oblique angles for verification of shorts, opens or acceptable ball collapse (Figure 1-7).

## Summary

Processing POP assemblies requires carefully controlled measures at each step of the process. Monitoring PCB warpage and BGA ball height will help mitigate the effects of the warpage caused by the CTE mismatch of package and substrate. Applying a controlled amount of tacky flux is also critical to ensuring adequate wettability to the pads, without creating a bridging effect. The use of underfill and its effect on reliability for POPs is not fully understood yet, but the application of a low CTE underfill is recommended for thermal cycling conditions.



Carmine Meola- Manager, Factory & Training Center

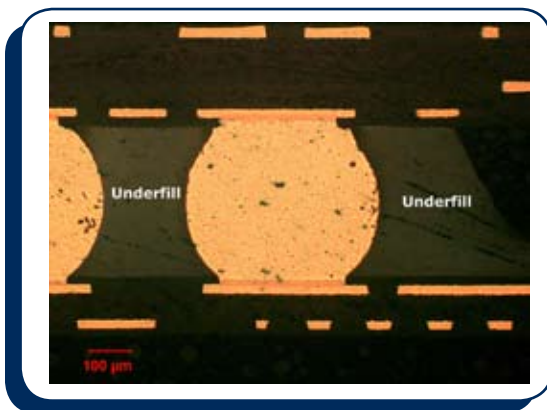


Figure 1-6: Solder ball with good wetting

# High Quality/High Reliability Soldering

In the electronics industry, when the terms “High Quality and High Reliability” (“High-Rel”) are applied to the soldering of components, a level of conformance is required that is suitable for the product’s design as it relates to its operational environment.

Over time, the Department of Defense, NASA, other government agencies, as well as some commercial companies where component or solder joint failure is not an option, have established standards (such as MIL-STD-2000A “Standard Requirements for Soldered Electrical and Electronic Assemblies”). These standards, when utilized in the manufacturing process, yield products with a high level of quality, a very low failure rate over time, high margins of safety, and low levels of risk.

There are certain key elements that are intrinsic to achieving the high level of quality necessary to meet the specifications and standards of a “High-Rel” Assembly. The metrics used to assess the acceptability of a class 3 and a class 1 assembly, differ in their requirements, with a more stringent set of specifications applied to meet IPC class 3 requirements. In the same vein, the “High-Rel” assembly would undergo a more rigorous set of standards, which would exceed the more conventional requirements as outlined by the IPC J-STD-001.

Some of the key areas that help define the differences between the “High-Rel” environment and the more conventional IPC specifications are as follows:

**1. Soldering Tool controls** - The Mil Specs have particular requirements for temperature, voltage, and current controls of the soldering equipment used for “High-Rel” assemblies. The IPC-J-STD-001 recommends guidelines in their appendix “B” for the isolation and temperature controls of soldering equipment, but does not specify requirements as does the MIL STD (45743, WS 6536, Mil STD 2000). A transient voltage of greater than 2V is not permitted under the Mil Spec guide, as an example.

**2. Visual Inspection** - Good workmanship and knowledge of the standards for high reliability assemblies, and certain visual acuity requirements are needed to meet the “High-Rel” Mil standard assembly and inspection qualifications. The J-STD-001 has no such requirements. Additionally, the level of illumination required for inspection of a “High-Rel” assembly requires 1000 foot candle / sqft of lighting. In the IPC spec, this is only a recommended value.

**3. Component Damage** - The “High-Rel” Standard will have limits to component damage and will specify the amount of allowable degradation. While the IPC-J-STD-001 refers to a degradation level below the part specification, the part specification is not always readily available to the inspection personnel.

**4. Definition of proper Solder Wetting** – Proper wetting of the solder joint is extremely important to the reliability and integrity of the connection. The “High-Rel” standard of desired wetting will call for angles of no less than 20 degrees and no greater than 60 degrees. The IPC J-STD-001D calls for wetting angles of less than 90 degrees, with certain exception allowing angles of greater than 90 degrees.

**5. Improving Stress Relief** – After the solder process, the requirements for the bend radii of component leads varies greatly between the “High-Rel” standard and the IPC standard. The IPC J-STD-001 allows solder in the bend radii as long as the solder does not touch the component body. The “High-Rel” standard only allows it on the inside bend of the component. This condition allows for better stress relief. The application of solder by hand soldering, wave soldering, or reflow soldering using solder paste, is done in such a manner as to obtain a concave solder fillet with a very low wetting angle. The lead, wire, terminal, or contact should be readily distinguishable in the solder. Solder coverage as to wire type, size and specific attachment as well as specific component type and lead/contact configurations, are described in the specification. There is also specific solder coverage issues related to the environment (salt or corrosive atmosphere), high voltage, or high frequency.

**6. Wire Insulation Removal, (Stripping)** - Use only tools and methods which impart NO DAMAGE or deformation to the insulation to the wire or wire strands. The IPC J-STD-001D for class 3 allows damage and severed strands for wires exceeding 7 strands. The “High-Rel” standard would not allow for “birdcages” or damage of any form that exceeds 5% of the wire diameter.

**7. Wire/Component Lead Preparation (Tinning)** - Tin stranded wires, in such a manner, as to assure solder penetration to the inner strands to obtain proper wetting without excessive solder on the exterior strands. This activity will enhance wetting and prevent strand separation during formation and attachment to terminals.

**8. Wire/Component Lead Forming and Attachment** - Form wires and leads for attachment to terminals in order to attain ideal mechanical contact, preventing movement during the soldering process. Also form and dress wires and leads in such a manner as to provide maximum stress relief. There are other considerations for both wires and component leads specific to size, type and specific attachment described in the specifications. The IPC J-STD-001 allows for misalignment for class 3 of 25% of the component / lead width. The “High-Rel” Standard does not allow for any side or toe overhang. Any solder build-up can only exist as thin film.

continued on page 9

# Tech Tips...

## Temperature Profiling for Advanced Packages



Soldering in surface mount electronic assemblies is accomplished by applying solder paste to the pad areas of the circuit board where components will be soldered, followed by heating to melt the solder particles in the paste, and then cooling to form the multitude of solder joints in the assembly. The times and temperatures used for this melting of the solder paste, also known as the thermal profile, is a key variable in the manufacturing process. This variable significantly impacts product yield. Over the past few years, the development of smaller, lighter, cheaper and more functional electronic component “advanced packages,” has pushed progress to be made in thermal profile development technology. These technology tips will help to ensure high quality and consistent results.

### Tip 1. Use the correct tools.

Two tools that are used to increase the accuracy and decrease the time necessary to generate a thermal profile for a product are the Mole and the KIC thermal profiling tools.

The Mole is a device that can travel, along with the electronic assembly being soldered, on the conveyor belt through the tunnel of the reflow oven. By placing multiple thermocouples at critical solder joint locations within the assembly, the Mole can collect data from areas where the thermal mass of larger components can affect nearby components and the activation of the solder flux component of the paste. This makes it possible to accurately document the temperatures and times experienced at the critical solder joint locations to achieve high soldering yield in the manufacturing process.

The second available tool is the KIC, a series of sensors permanently affixed inside the tunnel-like reflow oven, which can record the temperatures and times in the heating “zones” of the oven. This data, taken continuously during the manufacturing cycle (hourly to weekly), is combined with an initial, manually generated temperature profile within the assembly, to generate a “virtual profile” for the product that is continuously available during the entire production run. Results of this calculated “virtual profile” can be used as input to standard Statistical Process Control (SPC) software programs. This KIC input can then be used to continuously control the assembly process over the course of the production run.

### Tip 2. Ball Grid Arrays

The case of the Ball Grid Array represents a thermal profile challenge because there is often a significant temperature difference from the edge to the center of the array, especially for large arrays. It is necessary to place a thermocouple at the center of the BGA, beneath the component, to adjust for this effect. This discrepancy becomes more pronounced with

increases of the I/O (Input/Output) count and/or decrease of the pitch (center-to-center distance) of the BGA solder joints.

In the case of the Super BGA, which has a copper heat sink attached to the top (a 5 Watt continuous power dissipation package), the added thermal mass of the heat sink intensifies this issue and increases the need for a thermocouple under the center of the Super BGA for thermal profiling. Ultra BGA, the most thermally advanced of the BGA packages, carries the same concern as the Super BGA in thermal profiling because of its still larger copper content and resulting high thermal mass.

### Tip 3. Chip Scale Packages

Chip Scale packages (CSPs) are packages that are up to 20% larger than what the bare IC chip would be with no package around it. Because of their small size, care must be taken when thermal profiling assemblies containing this package to ensure that excessive heat is not applied to the CSP when reflowing the solder joints on the more massive components, such as the BGAs. A great danger here, is to exceed the moisture sensitivity level on the small CSP components in order to apply enough heat to reflow the more thermally massive Super or Ultra BGAs, connectors, inductors, or other thermally massive components.

This dictates that thermocouples be attached to the assemblies under CSPs to evaluate the extent of overheating of the smaller components that must be applied in order to reflow the solder joints of the high thermal mass components.

### Tip 4. Other Advanced Packages and their special Thermal Profile concerns

The newest of advanced packages, the TQFN (Thin Quad Flatpack No-lead) and the POP (Package-on-Package), have additional concerns. The TQFN has no elongated metal lead (J-leads or gull-wing leads), but only thin copper pads to be soldered. This requires a flat thermocouple or one that is embedded into the substrate board under the TQFN package.

POP requires definition of the process, as both of the stacked BGAs of the POP assembly might be soldered simultaneously, or only the bottom package with the second layer package added manually, later.

Thermal profiling of the newer advanced packages can be easily accomplished if one follows these special considerations.



Fred Verdi - EMPF Technical Director

# Manufacturer's Corner: Thermal Profiling

**K**IC, a manufacturer of thermal profiling instruments for the electronics assembly process, develops tools to help electronic manufacturers improve quality, productivity and traceability. At the Electronic Manufacturing Productivity Facility, the KIC 2000 is an indispensable tool in providing consistency of oven performance and thermal monitoring. The four areas in which KIC 2000 can add excellence to the manufacturing process are:

- Thermal profiling
- Thermal process development
- Continuous process monitoring
- Thermal process traceability

Thermal profiling involves measuring the time vs. temperature relationship as the subject board travels through the reflow chambers. The data relayed by the KIC 2000 includes statistics such as peak temperature, soak, time above liquidous, and more. The product's profile is crucial to understanding the "success" of the thermal process relative to the factors that limit the process. This is known as the process window.

Thermal process development deals with defining the appropriate process window and quickly setting up your thermal process device to achieve maximum effectiveness of the given process window. KIC recommends a three-step, analytical format: Define, Measure & Improve. A correct process window is primarily defined by the specifications for solder, components and substrate. KIC includes a built-in library of specs for hundreds of available solders. The operator can modify the limits of the application based on the tolerances for the specific application to arrive at the correct process window. To improve the process (or machine recipe), the process itself must be measured to determine its effectiveness. The measurement must include actual process data and the profile's "fit" to your process window. KIC's oven recipe search engine automatically selects the "One Best" oven setting by reviewing billions of alternative oven settings within a few seconds. You can choose to optimize the results and thereby improving the full scope of the reflow process.

Continuous process monitoring takes the error away from a time consuming process. Once the reflow process is up and running, a certain fluctuation or drift is unavoidable. KIC's automated and continuous process monitoring solution provides all critical statistics for every part that passes through the oven. As the real-time data is collected, KIC's system will warn if the process drifts out of control and it will shut down the feed conveyor if the process goes out of spec. This essentially ensures a zero-defect thermal process regardless of application.

Thermal process traceability is almost as important as the thermal process itself. Historically, product that has been manufactured

and delivered to the end customer does not carry with it information or documentation detailing the thermal process it experienced during production. Only information logging what recipe was used when a product entered and exited the machine may be stored. The KIC 2000 measures the profile for each processed product, the profiles "fit" to the established process window, relevant information such as date and time stamp, product name, oven recipe and so on. This information may be retrieved at any point in time by simply scanning the product bar code.

Since 1999, the year the KIC 2000 was first introduced, continued improvements and innovations have been added to this wireless profiler. Profiling can now be done in a matter of seconds; self triggering features are in place to automate a starting process. Upgraded features such as aluminum tape for attaching thermocouples greatly reduces prep time as opposed to laboriously soldering with high-temperature solders. Perhaps the most revolutionary additions to the KIC 2000 is called "Auto Focus". This utility builds an application library that is both intuitive and self evolving. Because it can detect solder paste and reflow ovens, simply enter loaded board dimensions as well as weight. The KIC 2000 will instruct the user of the starting procedure. By a single instruction from this starting point, users are guaranteed to be well within their process windows.

KIC has committed that future improvements will include the capability to optimize on energy use. The system will, within seconds, select the oven recipe that consumes the lowest level of energy to produce a product within specification. KIC designs, promotes and dedicates its products with an eye toward greener manufacturing processes.

Oven manufacturers are today building high-quality, stable machines. The KIC 2000 differentiates itself with value-added solutions for process traceability, documentation capabilities and a higher level of accurate and easy to use automation.

For more information related to this article, or to schedule a demonstration of the KIC 2000 thermal profiler located at the EMPF, contact Ken Friedman, 610-362-1200 x 279 or via email at [kfriedman@aciusa.org](mailto:kfriedman@aciusa.org).



Ken Friedman - EAB Coordinator

## Clean Room Requirements for Advanced Packaging (continued from page 4)

- Jewelry (hazardous for electrical, equipment, and bath contamination)

Things you should not do in a cleanroom:

- Remove anything from under your smock or cleanroom suit such as a wallet, money, or a cell phone
- Run or move fast (just walking in a cleanroom, creates or stirs up almost 5,000,000 particles (> 0.3um) a minute)

People are the largest contributor to particle contamination in any cleanroom. They account for about 46% of all particle contamination. Modern semiconductor fabrication cleanrooms have through-the-wall construction and clean tunnel operations that separate the person from the machines doing the work. This has dramatically reduced the particle contamination and improved yields. As the industry moves to tight-pitch flip chip packaging, the day will come (and has already for some

products), when the packaging line will have to move into a cleaner environment. Overall, the packaging industry has been driven to an ever-cleaner environment. In the future, older semiconductor fabrication plants may become the packaging lab for the next generation of devices.



Dean Kossives - Senior Packaging Engineer

## High Quality/High Reliability Soldering (continued from page 6)

**9. Plated Through Hole Configuration** - Plated through hole (PTH) component leads should be formed in such a manner that the component bodies are approximately centered within their hole span, and surface mount (SMT) devices approximately centered on their designated land patterns. Again, specific component types/lead forms have mounting requirements defined in the specification. The IPC J-STD-001 requires a 75% hole fill and a 25% depression, but does not require wetting to the land pattern on the primary side of the PWA. The “High-Rel” standard would require a wetted primary surface to re-enforce the plated hole bond.

**10. Cleanliness Requirements** - All soldered connections should be properly cleaned (and not damaged or further contaminated in the cleaning process), and be free of any surface contaminants or particulate matter, including solder balls of any size or shape.

While there are many other considerations as to “High Quality, High Reliability Soldering”, required to meet “High-Rel” standards, proper materials, process definition, process control and continuous process improvement, are the primary goals of

this standard to increase quality, improve first pass yield, and reduce costs.

In order to meet the needs of customers, agencies, and special clients for High Quality – High Reliability Soldering Training, the EMPF can provide custom “High-Rel” Soldering Technology Training. In addition to the current IPC J-STD-001 Training/Certification program, specific custom courses can be developed to meet the training requirements needed to equip employees with the necessary skills to produce “High-Rel” products

For additional information please contact the Training Center Registrar via email: [registrar@aciusa.org](mailto:registrar@aciusa.org), phone: 610-362-1320, or sign up on the web site at <http://www.aciusa.org>



Riley Northam - Master Instructor

# American Competitiveness Institute

National Electronics Manufacturing Technology Center of Excellence  
Monthly Class Schedule for the Calendar Year 2007



Contact the Registrar  
for course information  
and pricing:  
610-362-1295  
FAX: 610-362-1289  
registrar@empf.org

## NEW COURSE!

CIT/Instructor  
Certification

Rework, Repair, &  
Modification of  
Electronic  
Assemblies

2007

IPC-7711/7721  
CIT Certification

January 29-February 2  
March..... 5-9  
May..... 7-11  
July ..... 9-13  
September..... 24-28  
November..... 26-30

2007

IPC-7711/7721  
CIT Recertification

February..... 20-21  
April..... 4-5  
June..... 25-26  
September..... 4-5  
November..... 15-16  
December ..... 3-4

Call the EMPF  
Helpline  
for Free Electronics  
Manufacturing  
Assistance  
610-362-1320  
helpline@empf.org

## Electronics Manufacturing

### Boot Camp A

January 29-February 2  
April 16-20  
June 4-8  
September 10-14  
November 5-9

### Boot Camp B

February 5-9  
April 23-27  
June 11-15  
September 17-21  
November 12-16

## IPC Certifications CIT/Instructor

### IPC J-STD-001

January 8-12  
February 12-16  
March 12-16  
April 9-13  
May 21-25  
June 18-22  
July 16-20  
August 20-24  
September 24-28  
October 22-26  
December 10-14

### IPC-A-610

January 22-26  
February 26-March 2  
April 16-20  
May 14-18  
June 11-15  
July 23-27  
August 13-17  
September 17-21  
October 15-19  
November 5-9  
December 3-7

### IPC-A-600 PWB

Acceptability  
January 3-5  
February 27-March 1  
April 9-11  
May 29-31  
July 31-August 2  
August 27-29  
October 10-12  
November 19-21

### IPC-A-610 Recertification

January 16-17  
February 20-21  
March 19-20  
April 23-24  
May 14-15  
June 4-5  
July 16-17  
August 20-21  
September 10-11  
October 29-30  
December 10-11

### IPC J-STD-001 Recertification

January 17-18  
February 21-22  
March 21-22  
April 25-26  
May 16-17  
June 6-7  
July 18-19  
August 22-23  
September 12-13  
October 31-November 1  
December 5-6

## CIS/Operator

### IPC/WHMA-A-620

Wire Harness  
Manufacturing  
March 13-15  
June 26-28  
October 2-4  
December 17-19

### SMT Rework & Circuit Repair IPC-7711/7721

(Modules 1 & 4-7)  
February 12-15  
May 7-10  
August 13-16  
October 29-Nov. 1

### SMT Rework/ IPC-7711

(Modules 1, 4-6)  
February 12-14  
May 7-9  
August 13-15  
October 29-31

### Surface Mount & Thru-Hole Rework of Electronic Assemblies IPC-7711 (Modules 1 & 3-6)

March 19-22  
July 30-August 2  
October 8-11

### Repair & Modifications of PCB's IPC-7721 (Modules 1 & 7-9)

February 5-8  
April 30-May 3  
August 6-9  
November 12-15

### Circuit Repair IPC-7721

(Modules 1 & 7)  
February 5-6  
April 30-May 1  
August 6-7  
November 12-13

### IPC Challenge

January 19  
February 23  
March 23  
April 27  
May 18  
June 8  
July 20  
August 24  
September 14  
November 2  
December 7

## Skills

### Chip Scale Manufacturing

March 28-30  
June 20-22  
October 22-24

### BGA Manufacturing Inspection & Rework

January 18-19  
April 3-4  
June 18-19  
July 23-24  
August 29-30  
October 15-16  
November 26-27

## Continuing Professional Advancement in Electronics Manufacturing

### Lead Free Manufacturing

January 16-17  
February 26-27  
March 26-27  
April 30-May 1  
May 30-31  
June 27-28  
July 25-26  
August 27-28  
October 17-18  
November 19-20  
December 12-13

### Design for Manufacturability

February 22-23  
April 11-12  
May 24-25  
August 6-7  
October 8-9

### Failure Analysis and Reliability Testing

January 3-5  
March 6-8  
May 21-23  
July 9-11  
September 5-7  
November 28-30

Custom Courses  
and  
On-Site Training  
Available

Conveniently  
Located Next to the  
Philadelphia  
International  
Airport

All courses & dates subject to  
change without notice  
LD0010

