

American Competitiveness Institute

**ISO 9001-2000
Certified**

American Competitiveness Institute
One International Plaza, Ste. 600
Philadelphia, PA 19113
(610) 362-1200 • FAX: (610) 362-1290
HELPLINE: (610) 362-1320
WEBSITE: www.empf.org
www.aciusa.org

The EMPF is a U. S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

Michael D. Frederickson,
EMPF Director
Barry Thaler, PhD., bthaler@aciusa.org
EMPF Technical Director;
Technical Editor, Empfasis

In this Issue

- Page 1: Silicon Germanium System-On-Chip for Low Cost Phased Array Antennas
- Page 2: Ask the EMPF Helpline!
- Page 4: Applications for Adhesive Dispensing
- Page 5: Modeling Reliability of Lead Free Assemblies
- Page 6: Manufacturer's Corner: Aqueous Technology
- Page 7: Tech Tips: Microsectioning
- Back Cvr: Training Center Course Schedule



Industrial Advisory Board

Gerald R. Aschoff, The Boeing Company
Dennis M. Kox, Raytheon
Gregory X. Krieger, BAE Systems
Edward A. Morris, Lockheed Martin
Jack R. Harris, Rockwell Collins
Gary Kirchner, Honeywell
Andrew Paradise, Northrop Grumman
Art Smedberg, ITT Industries, Avionics Division

Silicon Germanium System-on-Chip for Low Cost Phased Array Antennas

Phased array antennas (PAAs, Figure 1-1) can enable high data-rate communications between large numbers of nodes, whereas fixed or mechanically steered antennas are less robust and may not satisfy future system requirements. The compelling performance advantages offered by phased array antennas are offset by their high cost, weight, and size. A silicon germanium (SiGe) System-on-Chip can provide low cost and low weight phased array receive and transmit antenna solutions. These antennas are being designed for operation in a frequency band that is suitable for radar communications in both surface and airborne applications.



Figure 1-1 Phased Array Antenna

Modern microelectronics manufacturing technologies are necessary to decrease the size and cost of the demonstration system. Flip-chip interconnect technologies are being used to replace wire bonding in multi-chip-module assemblies. Additionally, the development of a highly-integrated system-on-chip using SiGe process technology is

replacing gallium-arsenide (GaAs)-based microwave monolithic integrated circuit (MMIC) chipsets.

These technologies promise a breakthrough in phased array antenna cost, with significant improvements in size and weight, and have demonstrated feasibility for many of the necessary technology building blocks.

Complex Circuitry Fabrication Process

An advanced microchip is being fabricated with a SiGe epitaxial structure on top of silicon in a highly complex and involved process. A multi-process wafer (MPW) run allows costs to remain lower than large-scale processing with large chip fabricators. The MPW run incorporates functional units referred to as break-out cells. These are individual designs for circuit elements such as inductors and amplifiers. The less expensive commercial Jazz process will be used instead of the IBM 8HP process for fabrication of the SiGe die. The Jazz process was chosen because of the high non-recurring engineering (NRE) costs of the IBM process and the lack of design models for high frequency inductors.

The noise figure (NF) is an important parameter for any radar or communication system. It represents the difference in dB between a receiver's actual noise output, and that of an ideal receiver. The lower the NF of a system, the more closely it performs to an ideal system because it exhibits lower front-end losses.

Breakout Cells and Modeling

continued on page 3

Ask the EMPF Helpline!

A customer contacted the EMPF and requested a root cause analysis of a sensor failure...

Recently, a customer contacted the EMPF and requested a root cause analysis of an automotive sensor failure. After several conversations with the customer to discuss the failure modes and to determine the customer's requirements, the EMPF used the following test methods: electrical testing, optical microscopy imaging, Scanning Electron Microscopy with Energy Dispersive Spectroscopy (SEM/EDS) and Fourier Transform Infra-Red analysis (FTIR) for failure analysis. Several samples of the sensors were supplied by the customer to the EMPF, and analytical results were obtained.

Test Methods:

Optical Microscopy Imaging - The sensors provided by the customer were examined and several images were generated which facilitated the electrical measurements. These images were taken with an Olympus Stereo Microscope (Figure 2-1).

SEM/EDS Analysis - Scanning Electron Microscopy was performed using an Amray 1830 Scanning Electron Microscope to image the sensor for the determination of physical size, layout, and composition of the patterned resistor elements on the sensor element.

FTIR Analysis - The hot film sensor die was removed from the sensor base and the infrared spectrum of the residue was

determined through a Thermo-Electron Avatar 360 FTIR with the Inspect IR plus microscope.

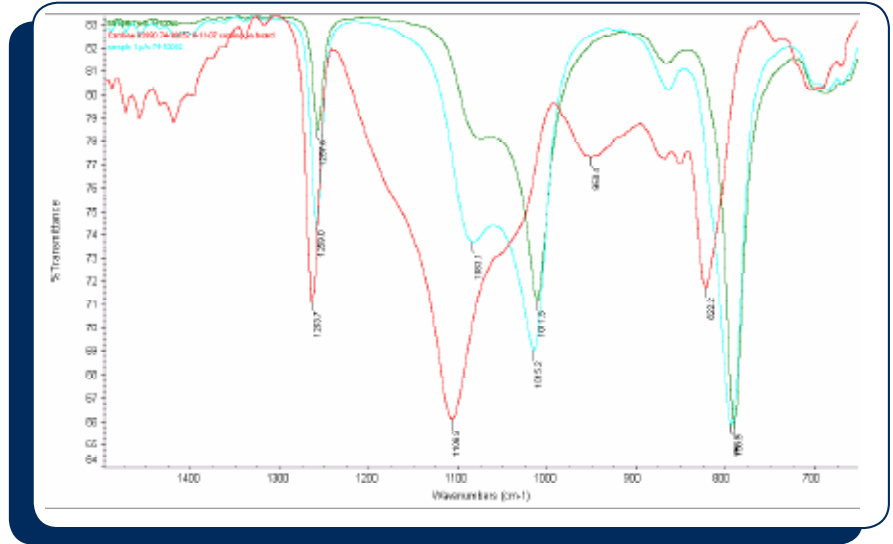


Figure 2-2: FTIR scans of sample 1, sample I and the conformal coating

Results:

▲ The SEM/EDS analysis of the sensor indicated the sensor was predominately platinum (Pt). Silicon (Si) was also observed, but may have been the result of a thin film of Pt.

- The amount of residue on the sensors varied
- The characteristic Infrared signature of the conformal coating following wave-number (cm-1) assignments:
 - 3284 (most likely moisture in the air or on the sample)
 - 2361 (CO₂ found in all spectra due to atmosphere)
 - 2341 (CO₂ found in all spectra due to atmosphere)
 - 1264 (due to Si-CH₃)
 - 1106 (due to Si-O-CH₃ asymmetrical stretch)
 - 950 (due to Si-O-CH₃ symmetrical stretch)
 - 822 (due to Si-C)

▲ The spectrum of the residue on each sensor was the same based finger print region (1500cm-1 to 500 cm-1).

- The characteristic Infrared signature of the residue included the following wave-number (cm-1) assignments:
 - 2360 (CO₂, found in all spectra due to atmosphere)
 - 2340 (CO₂, found in all spectra due to atmosphere)
 - 1259 (due to Si-CH₃)
 - 1083 (due to Si-O-CH₃)

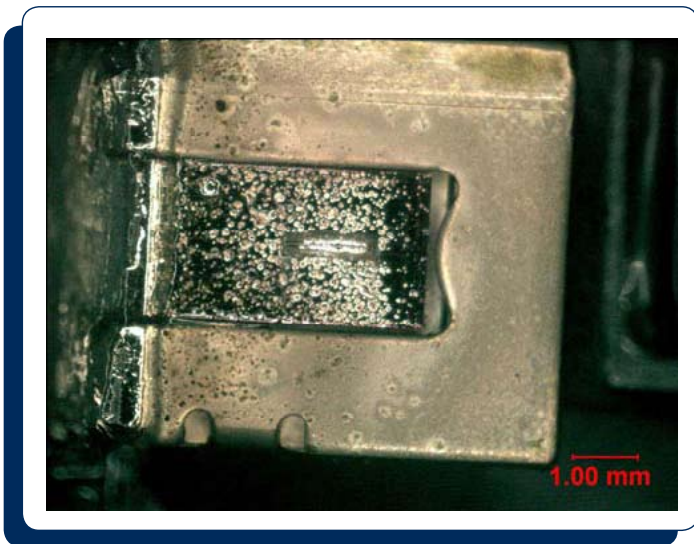


Figure 2-1: Optical image of one of the sensor samples

continued on page 9

Silicon Germanium System-on-Chip for Low Cost Phased Array Antennas (continued from page 1)

Components called phase shifters were modeled and measured: that was used to base line the design in order to shift the designs accordingly. Measured data for test chip components, such as low noise amplifiers (LNA), couplers, and inductors, are important parameters that are measured and then modeled using advanced design software. The break-out cells showed a good correlation between measured and modeled properties.

Silicon Germanium System-on-Chip Design

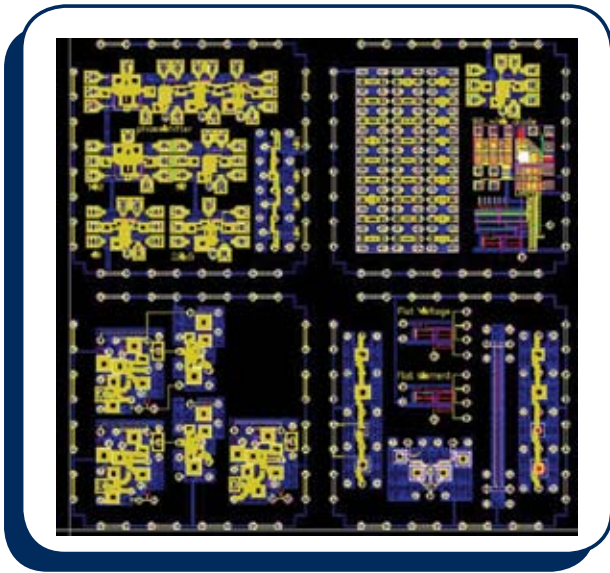


Figure 1-2: SiGe System on Chip

Many potential applications have requirements that the SiGe system-on-chip be a form, fit, and function drop in replacement for existing GaAs systems. GaAs has a greater energy band gap than SiGe, and a great deal of innovative design must be incorporated to ensure that the system operates properly.

Other engineering tasks that are being conducted include:

- Design of circuit schematics
- Simulations
- Chip carrier design
- Packaging and layout

Some of the most complex work is to ensure that there is proper uniformity and isolation between channels. Isolation is a measurable quantity stated in dB and is also a requirement for radar components, since the RF fields (i.e. signals) extend into the space between conductors.

Other challenging design tasks revolve around the trade-off between insertion loss and isolation. For example, a particular component may have an acceptable insertion loss but not an acceptable level of isolation; this will require that a similar component be modeled using calculations and placed into the circuit design. In many design scenarios, there are trade-offs between stability and noise figures.

The EMPF is reviewing the design of the SiGe system-on-chip cells, and is working on cell layouts in preparation for release of completed devices. Once fabricated and tested, minor design modifications may be incorporated to ensure that any performance deficiencies in the developmental versions are corrected before going into production. At that point readiness for production insertion will begin.



Anthony Vigliotti - Senior Packaging Engineer

Soldering Kits for

- J-STD-001 Certification**
- J-STD-001 Recertification**
- IPC 7711/7721 Certification**
- IPC 7711/7721 Recertification**
- Lead Free Certification**



Available online at
www.aciusa.org/products

Applications for Adhesive Dispensing

Flexibility in designing new printed circuit assemblies requires the use of both surface mount technology (SMT) and through hole technology (THT). There are many ways to deal with the mixture of the technologies to manufacture boards. Ideally, designers will attempt to keep the soldering technology consistent by going almost exclusively to a surface mount technology as recommended by DFM best practices. In many cases there is a need for THT components on one side of the PWB that must be concurrently processed with SMT components on the opposite side.

In cases where the mass of the component is greater than 4 grams, a heat cured adhesive can be placed on the bottom side components with an automated dispensing system that compliments the subsequent pick and place operation on the SMT side of the PWB. A dancer wave, or secondary wave, designed for SMT components, is typically used in this assembly model to “kiss” the secondary side with enough solder to form a proper fillet.

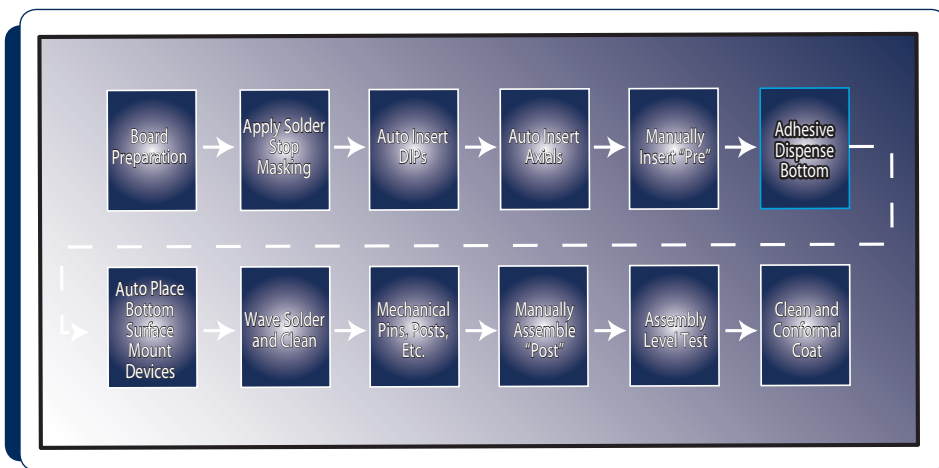


Figure 3-1: Typical Manufacturing Process

There are some precautions that must be considered in the dispensing of adhesive under components such as 0603 resistors and similar components. The volume of adhesive that is applied to the board must be enough to secure the component when the pick and place handler sets it on the board, while preventing excess adhesive to bleed under the pads and prevent the formation of an acceptable solder joint. According to IPC-A-610 section 8.1 (Staking Adhesive), “regardless of class, there is to be no adhesive present on solderable surfaces of the termination area, and that adhesive should be centered between the lands.”

The capability to apply adhesive in a precise manner is a critical manufacturing step for electronic assemblies, where the application of a gasket or the dispensing of an adhesive dot

becomes too expensive and inaccurate for hand operations. The complexity of the various designs, along with increasing component density, often necessitates the use of intricate applications of adhesive. Removal of unwanted adhesive due to excess deposits adds additional cost to the assemblies. Quite often, excessive or missing adhesive does not manifest itself until further down the process, where dewetting can occur as a result of extraneous adhesive deposits on pad and fillet areas.

Dispensing Systems

If a pneumatic dispensing unit is used, the adhesive dispenser settings must be experimentally determined to achieve a repeatable glue dot. Some of the variables that affect the dot size are tip diameter, dispensing pressure, actuation time and adhesive viscosity. As the adhesive in the dispenser is used, there will be a greater volume of air, resulting in a longer time to build up pressure. If the dispense time is short, the volume of adhesive dispensed with each pulse will be less. A control process, such as refilling the adhesive after a given number of cycles, will allow the unit to maintain a consistent dispense volume.

Adhesive dispensing can be versatile and cost effective, and may help simplify some of the more complex assembly operations which may require multiple thermal steps. For more information related to this article, please call the Helpline at (610) 362-1320.



Walt Barger- Senior Applications Engineer

**Call the EMPF
Helpline
(610) 362-1320**

Your Direct Connection to Manufacturing Support.

Modeling Reliability of Lead Free Assemblies

Simulation models have played, and will continue to play an important part in the predictive aspects of lead-free reliability. Thermo-mechanical modeling of the visco-elastic properties of lead-free solders including creep fatigue, elastic and plastic strain, CTE, elastic modulus, and stress relaxation, are critical details in the extrapolation of performance for a given set of environmental conditions. Presently, the ability to predict reliability solely on lead-free material attributes and behavior is not sufficient to warrant confidence in a result without verification of the mode of failure and the trigger mechanism responsible for the effect. A concurrent method of mathematical and FEM modeling, along with the important failure analysis mechanism, can be used until enough field reliability data can be accumulated to verify the accuracy of either method. Given the number of variables at numerous levels, this prospect is still a work in progress.

Modeling Approaches:

There are several types of models which differ based on the assessment of the failure apparatus responsible for creating the fatigue crack and fracture along the solder joints. They include strain, stress, fracture mechanics, and energy based models. The most widely used energy based model relies on calculated strain energy density accumulated during cycle times to calculate the fatigue life of solder joints. The various constituent elements of steady state creep and strain rates during cycling are used to calculate the number of cycles to crack initiation. Then the solder crack growth rate is computed and the fatigue life of the solder joint is determined. The Darveaux model has worked well as an indicator for joint failure on various BGA (Ball Grid Array) packages, but has limitations on smaller wafer level chip scale packages, where solder ball geometry is much smaller.

There are a number of FEA packages that offer various approaches to modeling. Some offer advantages in analyzing the behavioral responses of lead-free solder joints. They incorporate stress and strain effects of adjacent materials or layers, and integrate them by a series of constraint equations. Others focus on a Physics of Failure approach, which incorporates a combination of stress/strain and fracture mechanics.

When deciding on the nature of the model that is appropriate for lead-free solder joint life time reliability modeling, there are some consistent aspects that must be taken into consideration. It is very important to know which prediction models are applicable to the specific electronic packages whether using an energy density model, or a strain range method.

Some general considerations for assessing lead free reliability modeling include:

- Choosing the proper design and substrate can play an

equally important part as the selection of solder alloys.

- Consider the characteristic visco-elastic properties, such as primary and secondary creep, elastic modulus, and elongation, in the selection of a lead-free alloy. Attempt to predict the application of strain on the various locations of the package, and mitigate excessive strain by adaptation of restraints or stress decoupling interfaces.
- Components should be chosen on the basis of their suitability to the design constraints imposed by the selection of the lead-free solder. Low strain versus high strain applications may warrant differing device geometries.
- Minimize the CTE (Coefficient of Thermal Expansion) mismatch between adjacent materials to moderate the effect of high elastic modulus solder alloys.
- Limit the selection of alloys to binary or tertiary compositions, since many intermetallic formations have not been identified as being innocuous to joint integrity.
- SAC is suitable for designs that exert low strain rates, where SnPb fares better at designs where higher strain rates are expected.
- Substrates should match the solder CTE, if possible. Since many substrates designed for low CTE may have inferior copper adhesion, choose the copper tooth profile suitable to the substrate selection.
- Identifying where failures occur after environmental stressing is an important aspect of assessing the value of experimental results.
- Design experiments incorporating a robust range of factors and levels, while minimizing runs.

At the EMPF, classes are offered to assist engineers in making decisions that will help mitigate the unknown reliability factors associated with the implementation of a lead free manufacturing process. The classes offered cover the various aspects of reliability and design, as well as material selection and manufacturing.

For more information on this class or any others, please call the Training Center Registrar at (610) 362-1295.



Carmine Meola- Manager, Factory Services & Training

Manufacturer's Corner: Aqueous Technology

After the implementation of the ban on chlorofluorocarbons (CFC) in 1987, no-clean fluxes emerged in the marketplace. Most commercial manufacturers converted their assembly processes to no-clean, but the high reliability industry (military, aerospace, medical, etc.) continued to remove the flux residues from their assemblies.

In the early days of batch defluxing equipment, the technology more closely resembled household dishwashers than

industrial defluxing machines. After the CFC ban and subsequent decline of commercial defluxing, manufacturers of inline defluxing equipment focused on the high reliability market. Inline defluxing systems, while capable of removing flux residues, were large, loud, expensive, and consumed high quantities of electricity, water, and chemicals. These were not significant issues with commercial assemblers given the high volumes



Figure 5-1 Aqueous Trident batch defluxer

of commercial products produced. There are several reasons why batch technology has caught up to other cleaning technology for high reliability devices, including cleanliness, dryness, Statistical Process Control (SPC), environmental footprint, and throughput.

Cleanliness: Batch format defluxing systems do not rely on a fixed conveyor speed setting to determine the amount of wash, rinse, or dry time an assembly requires. Each process is independently controlled. For example, long washes may be combined with short dry times allowing unique cleaning profiles to be developed for a particular batch of assemblies. Batch machines are also uniquely capable of providing real-time cleanliness testing. Aqueous Technologies calls this technology “Predictive Cleanliness”. Because each process cycle is not interdependent on another, Aqueous Technologies developed a technology that allows the rinse water to be collected and subjected to ionic testing in real time. The real time cleanliness analysis allows the machine to expand or contract the cycle time in order to meet the user’s cleanliness requirement. Predictive cleanliness is highly desirable for high reliability assemblies, which tend to be more costly than commercial products. By knowing how clean the boards will be before the end of the defluxing process, post clean cleanliness testing becomes more predictable while producing

drastically lower failure rates.

Dryness: Drying is often the most overlooked segment of a defluxing process. Because the drying time is independently controlled, assemblies may be subjected to the actual time required to eliminate all moisture, both from the assembly’s surface, below components, and in between layers. Most batch format machines provide a rapid bake-out process, combining convection and radiant heat technology rather than a mechanical removal of moisture. For example, a batch process allows a user to single out the drying process requirements from the rest of the defluxing parameters, ensuring that the specific drying temperature and time are achieved for thorough drying.

Statistical Process Control (SPC): SPC is a required element of any high reliability assembly process. Common SPC mandates can be found in all quality standards. Because each process element is independently controlled, each process step and result can be individually recorded for statistical analysis. This becomes more evident as more and more companies are subjected to strict process audits.

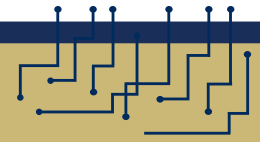
Environmental Footprint: This is an area where batch processes provide an advantage. Batch defluxing systems require about thirty gallons (114 liters) of water every hour. Inline processes, for example, may require as much as three hundred gallons (1135 liters) of water per hour. With batch defluxing technology requiring only one tenth of the water and disposal requirement of inline, as well as a fraction of the electrical current, it is logical that batch technology is less environmentally intrusive than most inline processes.

Throughput: The new high-yield batch technology preserves all of the advantages associated with batch processes, while providing throughput rates equal to or better than an inline alternative. The “digitalization” of medical, military, flight and other high reliability products have created a higher demand for higher volume defluxing systems. Increasing expectations of reliability and rising concerns over liability has significantly increased the use of defluxing technology equipped with the highest degrees of process control including real-time cleanliness testing.

For more information related to this article, or to schedule a demonstration of the Trident series batch defluxer from Aqueous Technologies located at the EMPF, contact Ken Friedman, 610-362-1200 x 279 or via email at kfriedman@aciusa.org.



Ken Friedman - EAB Coordinator



Micro-sectioning is a powerful failure analysis technique when coupled with Optical and/or Scanning Electron Microscopy (SEM) because it allows the examination of a variety of failures which could not be seen without this destructive analysis. Some of the electronic assembly areas that can be investigated through micro-sectional analysis include component defects, thermo-mechanical failures, processing failures related to solder reflow, opens or shorts, voiding and raw material evaluations. The process of microsectioning is delineated in the following steps:

Step 1: Identify the area of interest (Figure 6-1). If the sample is an assembly, some adjacent components may need to be removed as their presence may physically hinder access to the area of interest. A common tool used to remove components and section the area is a variable speed Dremel® rotary tool. A cross-section slightly larger than the area of interest is cut out to reduce damage to the adjacent areas.

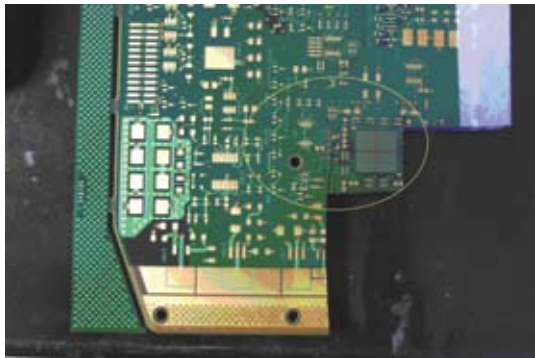


Figure 6-1 Cross-sectioning of PCB. Area of interest is circled in yellow.

Step 2: The sample is mounted (potted) to provide a matrix from which a highly polished surface can be obtained without damaging critical areas. The type of potting material will be dependant upon the sample. The EMPF uses both epoxy and acrylic mounting materials. These systems both incorporate a two part combination of resin and hardener, the ratio of which will affect the final characteristics of the mount. Epoxy is used whenever possible because of its lower shrinkage during curing and because the final mount is clear to allow viewing the internal features of the mount during polishing. The drawback of epoxy is that it requires an overnight cure as compared to the acrylic which cures in 2-4 hours.

Step 3: The section or sample is held in the appropriate orientation with either a plastic or metal clip to prevent movement of the sample during curing. The supported sample is placed into a molding cup pre-sprayed with a dry release agent to facilitate removal of the mount after curing. The potting material is carefully poured into the cup making sure to completely surround the sample and minimize entrapped air.

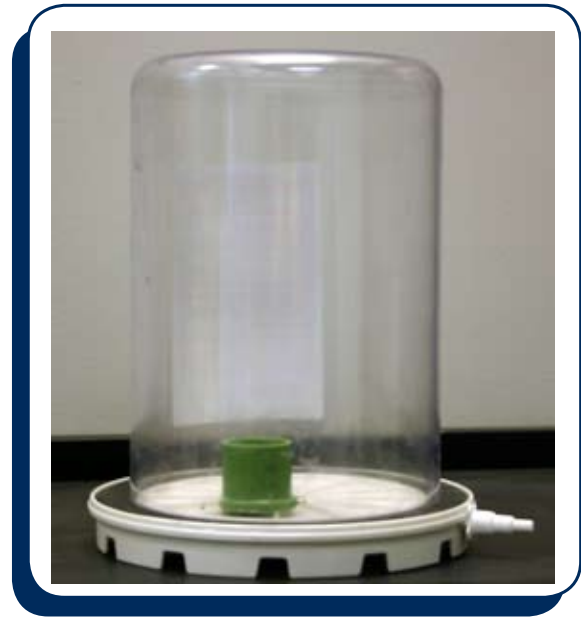


Figure 6-2: Vacuum apparatus with molding cup inside.

Step 4: The sample is placed into a vacuum for approximately five (5) minutes to assure the mounting material pulls into all the cracks and crevices and to remove any entrapped air. (Figure 6-2).

Step 5: The sample is progressively ground and polished with silicon carbide (SiC) paper of progressively smaller grit sizes that is fixed to a rotating platen. Polishing techniques can vary, but the objective is the same, to remove the scratches from the previously larger grit paper through a successively smaller grit paper. Final polishing is done with a rotating felt pad saturated with either alumina or diamond slurry. Figure 6-3 is a fully polished sample.

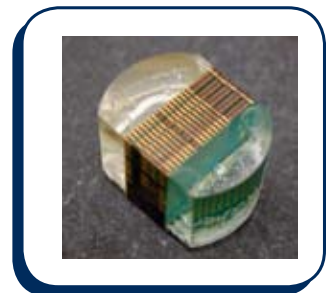
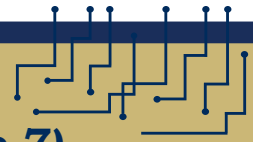


Figure 6-3 Polished sample

continued on page 8



ELECTRONICS MANUFACTURING BOOT CAMP TRAINING

A comprehensive, two week course featuring hands-on experience setting up screen printers, programming and placing components using automated equipment; profiling reflow ovens and wave soldering machines using the latest technology profiling systems; setting up various types of cleaning processes and more.

BOOT CAMP A

JUNE 2-6

SEPTEMBER 8-12 • NOVEMBER 3-7

BOOT CAMP B

JUNE 9-13

SEPTEMBER 15-19 • NOVEMBER 10-14

SIGN UP TODAY!

Step 6: Optical and/or SEM imaging is used depending on the failure. (Figure 6-4).

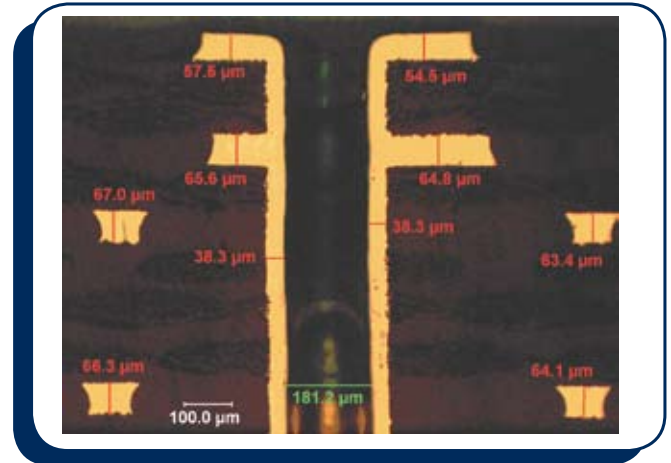


Figure 6-4 Optical image of a micro-sectioned via.

Micro-sectioning requires development of good technique to be able to section exactly into the desired area of interest. During failure analysis, only a single sample is available for analysis. Since micro-sectioning is a destructive test, care must be taken not to destroy critical evidence.

The EMPF has the capability and experience to perform microsectional analysis of both boards and components in addition to non-destructive testing, cleanliness testing, and reliability testing. If you would like additional information please contact the EMPF helpline at 610-362-1320 or log onto the EMPF website at www.empf.org.



Chris Deeble- Materials Engineer

Ask the EMPF Helpline (continued from page 2)

- 1015 (due to Si-O-CH₃ asymmetrical stretch)
- 864 (due to Si-O-CH₃ symmetrical stretch)
- 793 (due to Si-C)

▲ A comparison of the finger print region (1500cm⁻¹ to 500 cm⁻¹) of the samples and the conformal coating (Figure 2-2), indicated slight differences in the spectra between the coating and the residue. The characteristic absorption bands can shift depending upon the number and type of groups surrounding the functional group. For example, the spectrum for a polymer will have slightly shifted bands versus the monomer (starting material).

Conclusions:

The residue collecting on the sensor consisted of silicone and is most likely due to outgassing from the silicone conformal coating on the hybrid sensor. This residue is a distribution of molecular weight fragments consisting of monomer and oligomers (di, tri, and molecules consisting of multiple repeating groups).

A polymer can revert back to its raw materials, or a shift in the distribution can result from the volatilizing of lower molecular weight components depending upon the polymer. This can be affected by temperature and humidity and is dependant upon the type of polymer, degree cross-linking, and the degree with which the polymer is cured. In this application, the environment is such that a breakdown of the conformal coating is reasonable.

Recommendations:

This particular conformal coating may not be the best choice for this application. There are numerous low volatile organic compound conformal coatings available. A silicon conformal coating is a good choice because of its low mechanical stress properties, using very low VOC materials such as those used by the aerospace industry would eliminate outgassing residues. Viscosity, operating temperature range, and optical clarity requirement will also guide material selection.



Yin hao Wu - Senior Design Engineer

ANALYTICAL SERVICES LABORATORY

- *Failure Analysis*
- *Verification*
- *Cleanliness Testing*
- *High G Testing*
- *Solder Analysis*
- *Plasma Cleaning*
- *Counterfeit Component Analysis*
- *X-Ray Fluorescence*
- *Thermal Shock Testing*
- *Vibration Testing*
- *Thermal Sectioning*
- *Microsectioning*
- *HAST*

Need a service? Request a quote.

Call the EMPF Helpline today

(610) 362-1320

helpline@empf.org

www.empf.org

American Competitiveness Institute

National Electronics Manufacturing Technology Center of Excellence
Monthly Class Schedule for the Calendar Year 2008



Contact the Registrar
for course
information and
pricing:
610-362-1295
FAX: 610-362-1289
registrar@empf.org

Call the EMPF
Helpline
for Electronics
Manufacturing
Assistance
610-362-1320
helpline@empf.org

Custom Courses
and
On-Site Training
Available

Conveniently
Located Next to
the Philadelphia
International
Airport

Electronics Manufacturing

Boot Camp A
January 28-February 1
April 14-18
June 2-6
September 8-12
November 3-7

Boot Camp B
February 4-8
April 21-25
June 9-13
September 15-19
November 10-14

IPC Certifications CIT/Instructor

IPC J-STD-001
January 7-11
February 11-15
March 10-14
April 7-11
May 19-23
June 16-20
July 14-18
August 18-22
September 22-26
October 20-24
December 8-12

**IPC J-STD-001
Recertification**
January 17-18
February 21-22
April 24-25
June 5-6
August 21-22
October 30-31

IPC-A-610
January 21-25
February 25-29
April 14-18
May 12-16
June 9-13
July 21-25
August 11-15
September 15-19
October 13-17
November 3-7
December 1-5

**IPC-A-610
Recertification**
January 15-16
March 18-19
May 13-14
July 15-16
September 9-10
December 9-10

**IPC-A-600 PWB
Acceptability**
January 8-10
February 26-28
April 8-10
May 27-29
July 29-31
August 26-28
October 7-9
November 18-20

**Rework, Repair, &
Modification of
Electronic Assemblies
IPC-7711/7721 CIT
Certification**
January 28-February 1
March 3-7
June 9-13
July 7-11
September 22-26

**IPC-7711/7721 CIT
Recertification**
February 18-19
April 1-2
June 23-24
September 2-3
November 17-18
December 2-3

CIS/Operator

IPC J-STD-001
Call for Availability

**IPC/WHMA-A-620
Wire Harness
Manufacturing**
March 11-13
June 24-26
September 30 -October 2
December 16-18

**SMT Rework &
Circuit Repair
IPC-7711/7721
(Modules 1 & 4-7)**
February 11-14
May 5-8
August 11-14
October 27-30

**SMT Rework/
IPC-7711
(Modules 1, 4-6)**
February 12-14
May 6-8
August 12-14
October 28-30

**Surface Mount &
Thru-Hole Rework
of Electronic
Assemblies IPC-7711
(Modules 1 & 3-6)**
March 17-20
July 28-31
October 6-9

**Repair &
Modifications of
PCB's IPC-7721
(Modules 1 & 7-9)**
February 4-7
April 28 - May 1
August 4-7
November 10-13

**Circuit Repair
IPC-7721
(Modules 1 & 7)**
February 4-5
April 28-29
August 4-5
November 10-11

IPC Challenge
January 18
February 22
March 21
April 25
May 16
June 6
July 18
August 22
September 12
October 31
December 5

Skills

**Chip Scale
Manufacturing**
March 25-27
June 17-19
October 21-23

**BGA Manufacturing
Inspection & Rework**
January 17-18
April 3-4
June 19-20
July 23-24
August 27-28
October 15-16

Continuing Professional Advancement in Electronics Manufacturing

**High Reliability
Certification**
Call for Availability

**Lead Free
Manufacturing**
February 27-28
May 28-29
October 16-17
December 10-11

**Design for
Manufacturability**
February 20-21
April 9-10
May 21-22
August 6-7
October 8-9

**Failure Analysis and
Reliability Testing**
January 9-11
March 4-6
May 20-22
July 8-10
September 9-11

Wave Soldering
January 22-23
April 1-2
September 2-3
December 16-17