

American Competitiveness Institute

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*The EMPF is a U. S. Navy-sponsored
National Electronics Manufacturing Center
of Excellence focused on the development,
application, and transfer of new electronics
manufacturing technology by partnering with
industry, academia and government centers
and laboratories in the U.S.*

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Development of a Digital Receiver Exciter RF Architecture

Today's digital radars are designed to provide optimal performance in support of multiple simultaneous missions. As technology evolves, so must capability, and thus next generation radars must provide increased dynamic range and bandwidth in support of new capabilities.

Radars using open architecture distributed structure at each sub-array are considered

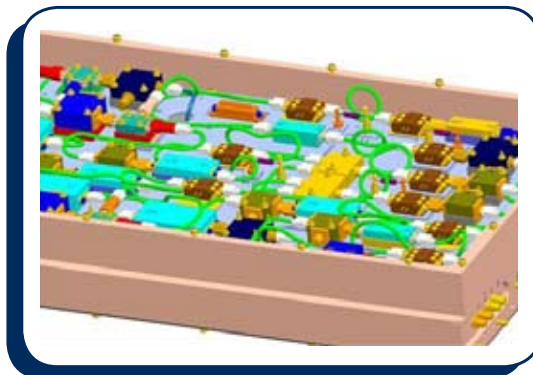


Figure 1-1: Current REX downconverter design

instrumental and necessary for achievement of this kind of unprecedented performance in the presence of jamming and clutter. In order to incorporate open architecture into these radars, development of digital receiver and exciter (DREX) subsystems is essential. Digital array radars require many DREX subsystems in order to support performance needs.

Reduction in size of hardware is essential in the implementation of DREX technology, as many radars contain hundreds to thousands of sub-arrays, each requiring at least one DREX subsystem. Obviously, size, cost, and weight immediately become a huge focal point of concern. In most cases, the minimization of

size, cost, and weight of a subassembly must also be traded with form, fit, and function of whichever existing receiver exciter (REX) technology that is to be replaced.

Fabrication and assembly processes must also be developed in support of a low-cost DREX for distributed architecture antenna sub-array. Key trade studies in support of this development shall focus on design, fabrication and packaging options. Optimal use shall be made of readily available, low cost, commercial off-the-shelf (COTS) and military off-the-shelf (MOTS) subsystems and components in the design trades.

Present REX assemblies in the higher frequency ranges, such S-Band, use high performance connectorized component packages to meet requirements (Figure 1-1). Increased volume and weight in addition to the higher costs associated with connectorized packages, cables, and specialized assembly are all undesired aspects of present REX technologies. Surface Mount Technology (SMT) can lead to significant savings in size, weight, and cost. While UHF DREX assemblies using SMT technology have been proven to be cost effective, achieving similar results at higher frequencies requires improved performance from the functional component packages and interconnecting substrates. One goal of a new REX design would be to fully model and optimize the characterization of the RF performance of the DREX assembly. New package configurations and tight control of assembly features must be

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Ask the EMPF Helpline!

A customer observed issues with through-hole technology (THT) components soldered with no-clean paste and no-clean flux.

The push to make product faster and cheaper without losing quality has forced manufacturing to examine ways to become more efficient through modifying, streamlining or completely eliminating processing steps. This particular assembly incorporated a “pin through paste” step to allow for attaching THT components at the SMT reflow step. This “pin through paste” process deviates from the normal SMT process to include apertures in the stencil for paste to be deposited in through-holes. SMT components are then placed and THT components are forced through the paste-filled vias and both types of technologies are reflowed in one step.

The EMPF was tasked with performing a Root Cause Failure Analysis on an assembly that displayed failures at three locations. The first, a five leaded connector was placed “pin through paste” as a SMT step, but reflowed again as part of the wave soldering step; a spray fluxer that was utilized as part of the wave soldering system; and a significant amount of flux was noted around the leads after wave soldering. Secondly, a three leaded triac – a high thermal mass location incorporating a Selective Solder Pallet with a large thermal mass. As a result, reflow temperatures only reach 205°C vs. the expected 230°C. And finally, a two leaded torroid Choke – a similar issue to the second location.

The following was a part of the Root Cause Failure Analysis:

Ionic cleanliness testing of an assembly as per IPC TM 650 2.3.28A “Ionic Analysis of Circuit Boards, Ion Chromatography Method”

Dynamic ionic cleanliness testing of an assembly as per IPC-TM-650 2.3.25C “Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract (ROSE)” - Ionograph method

Micro-sectioning and metallurgical analysis of the three components mentioned above through Metallographic microscopy and Scanning Electron Microscopy with Energy Dispersive Spectroscopy (SEM/EDS).

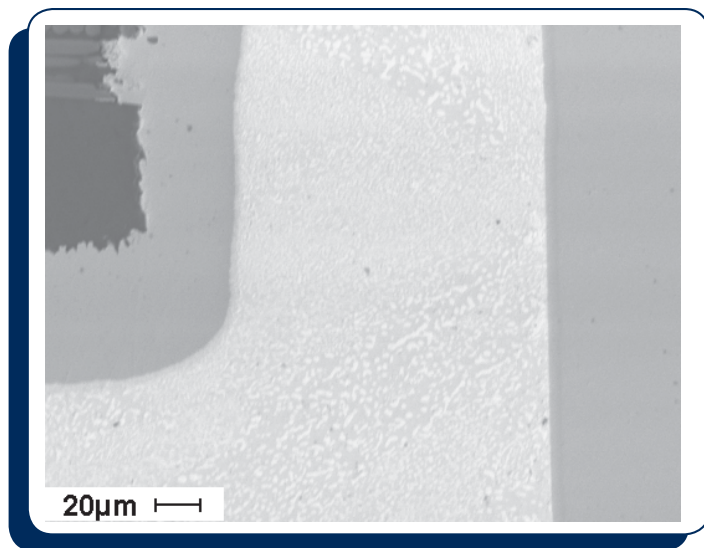


Figure 2-1: Metallographic images of THT component

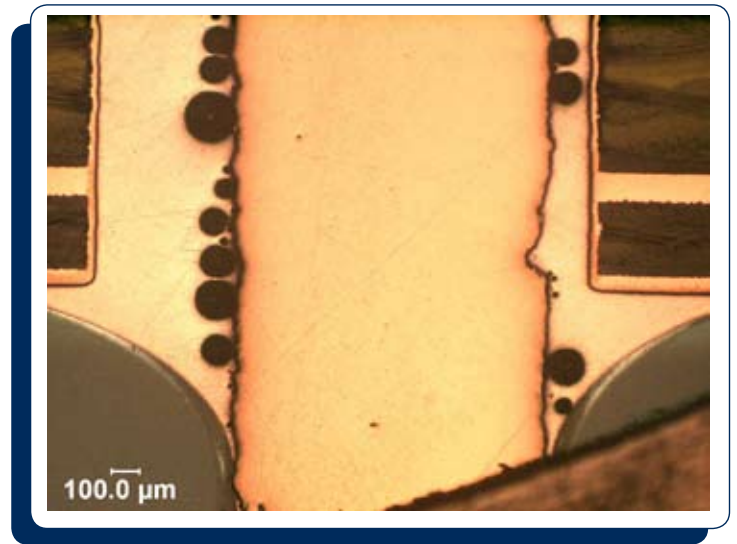


Figure 2-2: SEM image of 1st solder joint

Results:

Ion chromatography analysis indicated the PWA displayed the presence of 3.2µg/in² of chloride, 2.6 µg/in² of bromide and 102.4 µg/in² of succinic acid. The chloride and bromide levels do not exceed the EMPF recommendations for assemblies. However, there are no recommendations provided on the level of succinic acid, a common weak organic acid used in no-clean pastes/fluxes.

Ionograph testing indicated a second assembly displayed 45.69 µgNaCl equivalents/in². The pass/fail criteria of 10.06 µgNaCl equivalents/in² is only applicable to Rosin based chemistries. It was not determined if the no-clean flux was Rosin based or not. Both Ion Chromatography and Ionograph testing suggest significant flux residue.

Voiding was not observed at the five leaded connector and some voids were noted at the Torroid component. Significant voiding was observed at the triac device (Figure 2-1).

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Development of a Digital Receiver Exciter RF Architecture (continued from page 1)

equally developed to achieve repeatable RF performance at high frequency bands. Additionally, particular attention to the SMT process must be considered to ensure assembly yields for new package features and for achieving acceptable product reliability.

Established and innovative DFM (Design for Manufacturability) techniques can be employed to help achieve a high-yield surface mount DREX downconverter design. The DFM task would give the DREX more robust manufacturability by improving functional yield, reducing cost and increasing the reliability of the modules. Design for testability (DFT) methods should also be integrated into the DREX design review to ensure that certain testability features are included in the hardware product design.

Another important trade study necessary for a DREX design is the development of fabrication and assembly processes to extend current surface mount technology to the desired frequencies. Multilayer printed circuit boards incorporating microwave compatible materials would be utilized to develop processes capable of providing the required etching tolerances and parts placement accuracies. A top level functional manufacturing process flow would also need to be established, detailing the fabrication steps that accommodate a number of SMT package styles. Materials, such as ceramic and PTFE-based materials for microwave/RF functionality, and FR4 and polyimide for non-RF functions, should be taken into consideration. Blind vias, buried vias, standard vias, and via-in-pad for BGAs should also be evaluated within some trade space. The use of materials compliant with Restriction of Hazardous Substances (RoHS) regulations should also be considered, depending on the application. The EMPF has been a leader in providing technical expertise regarding lead-free strategies to industry for years. Additionally, reliability and quality management would need to be addressed for the SMT components.

Cost reduction goals are envisioned from the use of SMT techniques on microwave/RF quality multilayer circuit boards to integrate module and MMIC circuit functions. Processes would need to be developed for the assembly of the DREX modules which will involve a high level of automation to reduce assembly costs and deliver a consistent high level of quality complying with J-STD-001 class III requirement. Additionally, evaluation of available component packaging options must be performed, for components used in conjunction with RF signal bearing substrates. The packaging study should investigate reliable integration of components in the DREX substrate, utilization of integrated passive devices, robust flip-chip attachment methods, high frequency compatible underfill materials, reliability of RoHS compliant materials, and packaging / substrate testability.

Once the aforementioned trades are concluded and evaluation is complete, fabrication of a SMT prototype (Figure 1-2) can enable demonstration of the technology transition. A comprehensive cost model of the DREX module must also be developed, in order to minimize the cost-size-weight-and-powerfigure of merit upon completion of the project. The target process goal should be to reduce cost per DREX module by around 50%. The EMPF could contribute to the development of a low-cost DREX module in areas of:

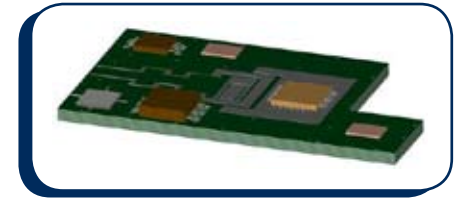


Figure 1-2 Conceptual DREX downconverter

- Flip-chip die bonding capability
- Evaluation of low underbody clearances on miniature components, and associated cleaning challenges
- X-Ray inspection to guarantee compliance to J-STD-001 class III requirements
- Solder paste printing
- Impact of RoHS compliance on fabrication processes

In order to identify areas of improvement, the DREX SMT downconverter can be simulated, targeting process optimization, cost reduction, and process flow volume. These simulations are designed to identify process bottlenecks, perform producibility risk analysis, perform plan versus actual schedule analysis, and facilitate supply chain collaboration.



Nick Fardella - Packaging Engineer

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Head on Pillow Defects on BGA Assemblies

The growing use of lead-free soldering in electronics manufacturing has introduced new types of defects that require proper identification and troubleshooting. One specific type of defect that has become more prevalent on lead-free ball grid arrays (BGAs) is called “head-on-pillow”. Head-on-pillow is a defect where both the paste deposit and the solder bump reach a full state of melt but fail to coalesce. It is important to differentiate head-on-pillow from a defect caused simply by insufficient reflow temperature, which is characterized by distinct solder spheres from the paste that have not been properly melted on the pad and BGA solder bump. With head-on-pillow the soldering temperature is sufficient to fully melt the solder bump and paste deposit, but an impediment to the formation of a proper solder joint exists. One or both ends of the failed interconnect will show evidence of displacement while it was melted, forming a shape that resembles that of a pillow with an indentation of one’s head.

A “dye and pry” test is used to identify the presence of head-on-pillow. The dye applied during this test can penetrate the gap formed between the two ends of the poorly connected solder joint and can be identified when the component is removed from the PCB. An example of the results of a dye and pry test on an assembly with head-on-pillow defects is shown in Figure 3-1.

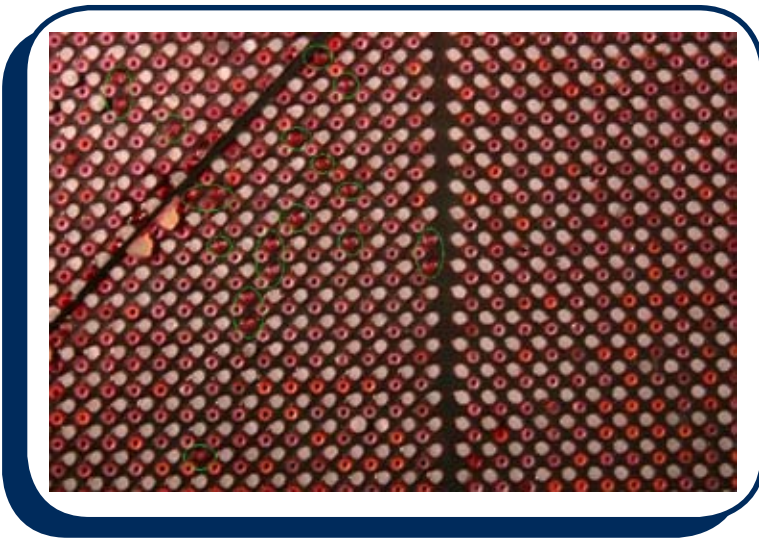


Figure 3-1 Dye and Pry Test

Another method to identify head-on-pillow defects is through visual analysis. Some head-on-pillow defects are readily apparent using relatively low-magnification optical inspection. If those defects are located on the outer rows of the assembly, an endoscopic inspection system may be sufficient to definitively identify head-on-pillow as the cause of a failure. If the defect is

present at an interior location on the interconnect array, a cross-section may be necessary to optically verify the presence of head-on-pillow. Once the solder joint is exposed, low magnification may be sufficient to identify head-on-pillow depending on the severity of the defect. Figure 3-2 shows an example of a head-on-pillow defect that was verified optically without the aid of mounting and polishing.



Figure 3-2: A head-on-pillow defect that was verified optically without the aid of mounting and polishing.

Some examples of head-on-pillow may not be severe enough to allow identification with low magnification optical inspection. These may still be verified optically, but require polishing and high magnification optical inspection. Figure 3-3 shows an example of head-on-pillow that required high magnification to be clearly identified.

Verification of the presence of head-on-pillow leads to an investigation into the cause. The ultimate root cause of head-on-pillow is a barrier that prevents the coalescence of the solder bump and the solder paste deposit. That barrier may be contamination on the surface of the solder bump that the flux in the solder paste is not able to remove. Testing to ensure that the components are not entering the facility with the suspected contamination present is an important first step. The recommended tests for contamination of this type is an extraction based (non-destructive) method suited for detection of non-ionic contaminants, such as UV-Vis Spectroscopy or Gas-Chromatography/Mass Spectroscopy. If no contamination is found on raw materials in as-received condition, a careful assessment of the factory’s handling practices is required. It is not difficult for contamination from factory personnel, whether in the form of body oils, hand lotions, or machine lubricant to

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Department of Defense Workforce Development

The EMPF is frequently asked for guidance in selecting the appropriate electronic manufacturing skills that are suitable for a customer's particular application. An employee may request course guidance for personal skill growth, subsequently adding value to their company. A manager may need to train a number of manufacturing associates to meet their quality needs. A training director may be required to start a program which will meet the skill needs across the various departments of the company. The EMPF, in cooperation with many of its partners, has initiated training programs that include many of the elements of our engineering courses (Boot Camp, Design For Manufacturability, and Lead Free), as well as the standardized IPC certifications (IPC 610, J-STD-001, 7711/7721, IPC 620, and IPC 600). These partnerships are created with our customer's trust to act as an advocate in validating their path forward for a successful training program.

The EMPF has always been in the forefront of instructing IPC and engineering courses to the electronics industry for both the DOD and industry related ventures. Our latest offering includes three levels of training classes that were developed for government personnel who manufacture electronics, at various skill levels, and across various government positions.

Level I Intern/Pre Journeyman

This level is focused on a one week experience for the intern and pre journeyman engineer/technologist, GS-12 or below. The session was conducted at both the EMPF facility and at the customer site. The students start with design concepts and end with a good hands-on experience on the manufacturing of electronic assemblies. Some of the topics that are covered include:

- Manufacturing and documentation review
- Computer-aided Design files
- Review of various design techniques
- Reviewing Manufacturing bill of materials
- Review Standards and Specifications
- Validation of revision compliance
- Understanding product requirements
- Fundamentals of Surface Mount Technology (SMT) and Mixed technology Manufacturing

Additionally, the student builds his own assembly using the manufacturing methods and equipment employed in SMT, and plated through hole processes.

Level II Journeyman Course

Level II is a comprehensive program designed to educate participants on the many different processes and materials used in through hole and surface mount technologies. The course is

designed to give an overview of the critical skills, requirements, and technical attributes needed for the working level staff in the Department of Defense, while acquiring the necessary training for an electronic manufacturing operation. The student also gains an understanding of the skill sets needed for career advancement to a Level III certification pertinent to the defense acquisition process. It is an intensive program that provides students with the opportunity to learn and understand the processes, tools, and materials used to properly manufacture electronic assemblies. It includes topics such as Design For Manufacturing, Lead Free, Design of Experimentation, and Statistical Process Controls for electronics, Chip Scale and Ball Grid Array technology, and other leading-edge electronic technologies that are presently used.

Level III Manager's Course

A one day course developed to provide training for senior level personnel (GS14 to SES/GO), this course provides an overview which will identify the key functional and physical characteristics critical to the infrastructure of an electronic assembly and manufacturing plant. The course covers the three main sections dealing with material management, new technologies, and critical legislation. The course is designed to help the individual clarify the significance of implementing controls in various areas such as configuration management, sustainment of product, control change, documentation, prohibitive material process, and the effects of Commercial Off The Shelf (COTS) products on the material infrastructure.

This program was a response to a need that helped our partners maintain the necessary skilled personnel to effectively produce quality products. The EMPF has worked diligently to invest its expertise for such projects, and will continue into the future.



Carmine Meola- Manager, Factory Services & Training

IPC Certification Classes

- J-STD-001 • IPC-A-600 • IPC-A-610
- IPC 7711/7721

Call or check the website for availability
http://www.aciusa.org/training_ipc

Manufacturer's Corner: Pace ThermoFlo TF-2700 Rework Station

PACE's ThermoFlo TF 2700 rework station is a very popular automated, cost effective solution for area array package rework. Designed for today's PCBs, this system can safely install and remove a wide variety of components such as ball grid arrays, chip scale packages, quad flat non-lead, ceramic ball grid arrays, and other surface mount devices.

The PC based software allows the easy creation of thermal profiles and guides the operator through an intuitive interface that virtually automates the process. All operations, component pick-up, alignment, placement, and reflow are completed in a single axis, eliminating the risk of component movement after placement. Component pick-up is achieved by placing the component into an adjustable nest above the optics assembly. The reflow head automatically picks up the component and moves it to the proper focal position for alignment. A high-flow vacuum pump holds the component securely. Flux dipping and stenciling can also be incorporated into the component pick-up procedure. The PCB holder features a fine micrometer adjustment for the most delicate X and Y-axis alignments. Precise and accurate, within 25 μm (.001"), Z axis movement is ensured through a twin rail, linear bearing motion control assembly that is similar to those used on automated pick and place equipment. The component is placed on the PCB with a controlled, minimum pressure.

VOS from dirt and contamination that are common intrusions in some work environments. Independent lighting controls for the ultra white, high power, LED based lighting provides maximum overlay contrast for the component and PCB. This lighting eliminates shadow and has wide dispersion angles to adequately illuminate large components.

ThermoFlo systems combine a convective topside 1200 Watt heater with stable and powerful IR bottom-side heating. This closed loop temperature control and unique vented nozzle design helps maintain uniform temperature distribution during reflow. High power heaters allow for successful, safe and repeatable reflow at low temperatures. The rework station is self-contained and does not require an external air supply or vacuum connections.

For more information related to this article, or to schedule a demonstration of the Pace ThermoFlo TF-2700 located at the EMPF, contact Ken Friedman, 610-362-1200 x 279 or via email at kfriedman@aciusa.org.



Ken Friedman - EAB Coordinator



Figure 5-1 Pace ThermoFlo TF-2700

The TF-2700 optic system utilizes advanced digital, Sony color cameras and a high quality dichroic prism for very fine image clarity. This is achieved through Pace's high resolution Vision Overlay System or VOS which does not require routine calibration. The images are viewed using the PC in standard or full screen viewing modes. The Sony camera features 72X magnification and both auto-focus and manual capability. The automatically controlled, retractable optics housing protects the

Upcoming Workshops

Conformal Coating Processes
Graham Nesbit, Gen 3
May 27, 2008

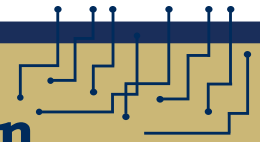
Advanced Stencil Techniques
Jason Fullerton

ACI Senior Products & Applications Engineer
June 3, 2008

For more info, contact
Ken Friedman, EAB Coordinator 610-362-1200 ext 279
kfriedman@aciusa.org

Tech Tips...

Conformal Coating Inspection



As modern electronics assemblies continue to use ever greater packaging densities and are subjected to increasingly hostile operating conditions, the use of high performance conformal coating materials will become increasingly commonplace for many manufacturers.

When high reliability is desired, a conformal coating should be applied. Conformal coating is a thin polymeric layer which “conforms” to the topography of the PWB and components. It acts as an insulator protecting the circuitry and components against shorts and contact with moisture as well as other contaminants. It also provides mechanical protection from such things as vibration and thermal shock.

Choosing the right conformal coating for the specific PWB design application is critical as there are a variety of different materials available. PWB cleanliness and optimal application methods are also very important to ensure good adhesion and reliability.

Inspection

Any conformal coating production process can be visually inspected in production using a UV microscope (Figure 6-1). All approved coatings contain a UV trace that glows with a bright blue luminescence under UV light to make coated and uncoated areas easily detectable. With experience, operators can use the degree of luminescence as a measure of both presence and volume of coating at different locations across a board’s surface.



Figure 6-1 UV Inspection of Conformal Coating

The necessity for inspection becomes evident when a single void or bubble provides a path for moisture to reach the substrate and reduce the coating effectiveness. With automatic coating, a random or pre-selected interval test may be adequate, but 100% inspection is always recommended and is mandatory in high reliability and safety critical applications.

It is also important to inspect boards after rework to ensure any reapplication of coating material doesn’t end up on the inside or underside of devices that should not be coated. The IPC-CC-830 and IPC-A-610 specifications demand

inspection be carried out and define conformal coating defects as:

Ref: IPC-A-610D Section 10.5 - “Non conforming defects... Voids, bubbles, adhesion loss, de-wetting, ripples, fisheyes, orange peel, or foreign material that expose circuitry, or adjacent conductive surfaces.” It is generally recommended that inspection be done visually with UV and at 4X magnification.

Conclusion

Choosing the right conformal coating and application process is not easy. It is advantageous to work with a vendor that has the experience of solving hundreds of specific coating problems and can give advice on relevant reliability standards and specifications. The correct approach will result in the reduction of end product failures in the field. These can be the most expensive problems a company will ever experience, and in safety critical applications, life threatening

When inspecting conformally coated PWBs, understanding the materials and processes used in production, and the acceptability criteria, will assure a high degree of reliability.



Carmine Meola- Manager, Factory Services & Training

Soldering Skills Kits

- J-STD-001 Certification
- J-STD-001 Recertification
- IPC 7711/7721 Certification
- IPC 7711/7721 Recertification
- Lead Free Certification



Available online at
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Head on Pillow Defects on BGA Assemblies (continued from page 4)



Figure 3-3: Head-on-pillow that required high magnification to be clearly identified

be transferred to a raw component when improperly handled. Tasks such as removing or replacing BGAs on a matrix tray or loading and unloading of trays from placement equipment can be avenues of contamination if personnel are not trained and disciplined in the proper handling of electronic components.

More commonly with lead-free soldering, an occurrence of head-on-pillow is related directly to the reflow process. During a reflow soldering process, the flux present from the solder paste is required to clean the initial oxidation from the parts to be soldered, as well as protect the materials against continued oxidation during the reflow process. This oxidation prevents proper homogeneity between the solder ball and the solder paste deposit and will result in head-on-pillow.

One possible cause of excess oxidation is insufficient solder paste (and thus flux) volume present. In this case, the solder paste printing process may need to be optimized to ensure that sufficient paste is present. Another potential cause of flux failure during reflow is poor material control. Solder paste materials need to be stored and handled properly to ensure that they function as expected. Careful observation of shelf life control, storage conditions, factory environmental conditions, and stencil life performance are important to ensure that the flux constituent in the solder paste is able to perform all of its functions in the reflow process.

The reflow profile can be a cause of head-on-pillow defects by exposing the flux to excessive temperatures for durations beyond what it is designed to withstand. This causes the flux to exhaust its oxidation cleaning abilities well before the completion of the

reflow cycle, regardless of the amount of flux present, and even if the raw component and the solder paste have been properly handled for their entire life. The obvious change that can be made to the process to prevent this occurrence is to reduce the profile length and/or modify the profile temperatures to prevent the premature exhaustion of the flux.

A case of head-on-pillow was recently encountered during a project undertaken at the EMPF. The project involved the attachment of a large BGA component (approximately 2 in² with over 2000 solder balls on a nearly full array) to a large PCBA using the Metcal/OKI APR-5000 hot air rework equipment. The BGA incorporated a heat spreader as a die cover and utilized lead-free tin-silver-copper solder balls. A no-clean solder paste was applied to the PCBA prior to installation of the BGA and was to be reflowed along with the BGA during the attachment process.

Due to the sensitive nature of the PCBA, and the warpage that had been previously observed when attempting an attachment with a reflow cycle of standard length, an extended profile was designed to minimize thermal gradients across the PCBA. This profile extended for over 1000 seconds from ambient temperature to peak. Although excessive thermal gradients across the PCB were no longer present on the longer profile, an unintended consequence was a large number of head-on-pillow defects on the assembly due to the extended duration of the profile and the exhaustion of the flux during the reflow cycle. This was verified by optical inspection after performing a dye and pry operation, followed up with a cross-section; the results of this analysis by the customer are shown in Figures 3-1 and 3-2.

Since reducing the length of the profile would increase the risk of PCBA warpage, another strategy had to be employed to prevent this defect. The use of an inert atmosphere would prevent the formation of an oxide on the solder bumps after the flux was exhausted during the reflow cycle and allow the solder to coalesce. For verification, another attachment was performed after outfitting the rework machine with a nitrogen source. No changes were made to the temperature settings of the rework equipment. A dye and pry analysis of the soldered part showed no examples of head-on-pillow and demonstrated that the use of nitrogen successfully mitigated head-on-pillow defects on this extended length profile.



Jason Fullerton- Sr. Product and Applications Engineer

Ask the EMPF Helpline (continued from page 2)

The solder was confirmed to be a eutectic 63Sn/37Pb. The presence of intermetallic compounds (IMC) were observed at the hole-wall/solder interface and solder/lead interface, indicating good wetting was present.

The solder joints at the five leaded connector did not have a uniform grain structure (Figure 2-2) with regions where the Pb grains appear coarsened.

Conclusions/Recommendations:

The IPC 610 calls out a maximum of 25% by volume of allowable voiding within BGA balls. There are no pass/fail criteria for voiding within THT components. Based upon our opinion and the experience of the customer, these voids are a potential issue and could compromise the mechanical strength of the solder joints. In addition, such voiding may influence functionality, specifically in high power or RF applications where current carrying capacity and solder joint geometry play a role.

The issues observed by the customer appear to be complex and not related to one aspect of their assembly process. Despite the assembly's relatively small size, there is a significant thermal mass due to the components. The customer does recognize this issue and has attempted to mitigate the problems.

The pin in paste or through-hole reflow technology has found industry favor. The pin in paste process can be problematic. The assumption is that complete or partial vertical fill is achieved (J-STD-001 calls for 75% minimum). The process of stencil printing paste may not provide sufficient paste to fill a hole. Depending upon the aspect ratio of the hole, a smaller aspect ratio results in more hole fill issues. To further complicate matters, there is also a reduction in the volume of the paste as the flux volatilizes during reflow.

In the case of these samples, vertical fill does not appear to be a problem. However, the cleanliness tests, visual observations, and circular voiding within the solder joints, point to an excess flux issue. It is recommended that for these locations the appropriate volume calculation be confirmed. The references below provide example calculations. If too much flux is being left on the board, a redesign of the stencil apertures at these locations should address the issue.

The non-uniform grain structure suggests uneven cooling/heating of the solder joint. This is not a major concern, but does corroborate what the customer has already observed and may have contributed to the trapped flux. This should be confirmed through further examination of other locations and at different points in the process flow. Along with further testing, the EMPF can assist with review of the SMT reflow profile and Wave Solder

parameters along with the Selective Soldering steps to confirm processing conditions are appropriate.



Sam Pepe - Chemist

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May 13-14
July 15-16
September 9-10
December 9-10

**IPC-A-600 PWB
Acceptability**
January 8-10
February 26-28
April 8-10
May 27-29
July 29-31
August 26-28
October 7-9
November 18-20

**Rework, Repair, &
Modification of
Electronic Assemblies
IPC-7711/7721 CIT
Certification**
January 28-February 1
March 3-7
June 9-13
July 7-11
September 22-26

**IPC-7711/7721 CIT
Recertification**
February 18-19
April 1-2
June 23-24
September 2-3
November 17-18
December 2-3

CIS/Operator

IPC J-STD-001
Call for Availability

**IPC/WHMA-A-620
Wire Harness
Manufacturing**
March 11-13
June 24-26
September 30 -October 2
December 16-18

**SMT Rework &
Circuit Repair
IPC-7711/7721
(Modules 1 & 4-7)**
February 11-14
May 5-8
August 11-14
October 27-30

**SMT Rework/
IPC-7711
(Modules 1, 4-6)**
February 12-14
May 6-8
August 12-14
October 28-30

**Surface Mount &
Thru-Hole Rework
of Electronic
Assemblies IPC-7711
(Modules 1 & 3-6)**
March 17-20
July 28-31
October 6-9

**Repair &
Modifications of
PCB's IPC-7721
(Modules 1 & 7-9)**
February 4-7
April 28 - May 1
August 4-7
November 10-13

**Circuit Repair
IPC-7721
(Modules 1 & 7)**
February 4-5
April 28-29
August 4-5
November 10-11

IPC Challenge
January 18
February 22
March 21
April 25
May 16
June 6
July 18
August 22
September 12
October 31
December 5

Skills

**Chip Scale
Manufacturing**
March 25-27
June 17-19
October 21-23

**BGA Manufacturing
Inspection & Rework**
January 17-18
April 3-4
June 19-20
July 23-24
August 27-28
October 15-16

Continuing Professional Advancement in Electronics Manufacturing

**High Reliability
Certification**
Call for Availability

**Lead Free
Manufacturing**
February 27-28
May 28-29
October 16-17
December 10-11

**Design for
Manufacturability**
February 20-21
April 9-10
May 21-22
August 6-7
October 8-9

**Failure Analysis and
Reliability Testing**
January 9-11
March 4-6
May 20-22
July 8-10
September 9-11

Wave Soldering
January 22-23
April 1-2
September 2-3
December 16-17