empfasis

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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government centers and laboratories in the U.S.

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In this Issue

Flip Chip Assembly

The intense competition in the electronics industry generally serves to drive down the size and cost of electronic products while improving their performance, flexibility, and reliability. As a part of this effort, packaging methods are constantly being improved and new, innovative methods are being developed. One area of focus is highly integrated chip-level electronics assembly, using multiple unpackaged dies and electrical components in a single package. One of the most popular methods is known as flip chip assembly.

Flip chip microelectronic assembly is the direct electrical connection of face-down, or flipped electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip input/output (I/O) pads. In contrast, wire bonding uses face-up chips with a wire connection to each pad (Figure 1-1). Flip chip components are predominantly semiconductor devices; however, components such as passive filters, detector arrays, and microelectromechanical systems (MEMS) devices are also used in flip chip form. IBM still uses the flip chip interconnection that they introduced in the early sixties for their mainframe computers. The assembly process has proliferated in many other applications, including automotive electronics, smart cards, radio frequency identification (RFID) cards, electronic watches, cell phones, and high speed microprocessors.

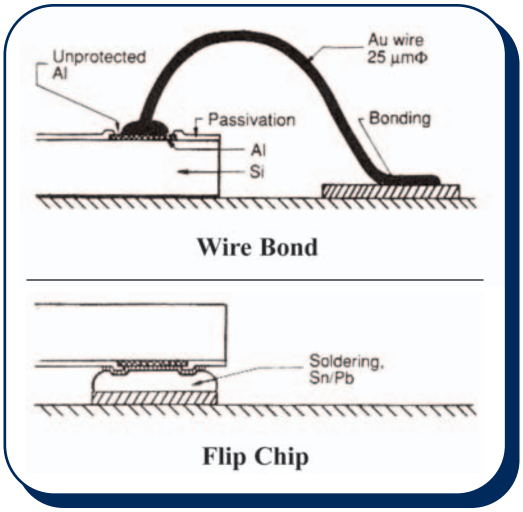

Figure 1-1: Wire Bond versus Flip Chip

Figure 1-2: Solder Balls

The popularity of flip chip packaging results both from flip chip's advantages in size, performance, flexibility, reliability, and cost over other packaging methods and from the increased availability of flip chip materials, equipment, and services. Eliminating package molding and bond wires reduces the required board area by up to 95%, and requires far less height. Flip chip offers the highest speed electrical performance of any assembly method due to reduced signal inductance. This is because the interconnection path is much shorter in length (0.1mm versus 1-5mm) greatly reducing the inductance of the

continued on page 4

Ask the EMPF Helpline!

Recently, a customer contacted the EMPF helpline to investigate imperfect wetting on printed circuit boards.

Solderability Analysis of Printed Circuit Boards

An electronics assembly manufacturer observed imperfect wetting on printed circuit boards (PCBs) that were purchased from a new vendor. The PCBs in question were manufactured with a hot air solder leveling (HASL) process. To investigate the solder wetting problem, the EMPF suggested solderability testing per J-STD-003B, Test F 4.3.1, Wetting Balance testing.

Wetting balance analysis involves dipping the pad areas into flux prior to applying solder using the Kester® KWB-1000 Wetting Balance with the conditions in Table 2-1. Flux residue is removed post testing with isopropyl alcohol before final inspection at a magnification of 40X.

Parameter description	Specific value/type J-STD-003B 4.3.1 Test F
Pre-test specimen cleaning	None
Flux type (J-STD-004 activity)	Kester® RMA 185 (ROL1)
	Alpha Metals® Purple flux Organo flux 3355 (ORH1)
Flux application, seconds	Dip, 3-5
Solder	63/37 tin/lead alloy solder from Kester®
Solder test receptacle	Bath
Solder temperature, °C	240
Height above solder surface at start of test, mm	10
Pre-heat, seconds	20
Immersion angle, degrees	40
Immersion/Extraction speed, mm./sec.	5
Immersion depth, mm	0.5
Test duration, seconds	5

Table 2-1: Wetting Balance Parameters

The wettable perimeter and cross-sectional area were determined for the pads. This information along with the immersion distance was used to calculate the volume and maximum theoretical wetting force based upon the formula shown below. The final units are normalized based upon the wettable perimeter and are reported in terms of µN/mm.

$$F_{max.\ theor.} = t \times P \times \cos(\alpha) - (d \times V \times g)$$

Where:

$F_{max.\ theor.}$ is the maximum theoretical wetting force (µN/mm)
t is the surface tension of the solder (0.4joules/m^2)
P is the wettable perimeter (mm)
d is the density of 63/37 eutectic tin/lead solder at 235/245ºC (8110 kg/m^3)
V is the immersed volume (mm^3)
g is the gravitational constant (9.81 m/s^2)
α is the wetting angle assumed to be 0 degrees for perfect wetting

Acceptable solderability can be established through evaluation of wetting balance curve properties: wetting time, wetting force and general shape of the curve (Figure 2-1). J-STD-003B provides suggested evaluation criteria based upon these properties (Table 2-2).

The results of the testing indicated three out of four test trial pads passed both Set A and Set B evaluation criteria with strong wetting forces generated (Table 2-3 and Figure 2-2). The last trial was performed using a highly active water soluble flux.

Parameter	Description	Set A	Set B
T_0	Time to buoyancy corrected zero (cross-over time)	$\leq$ 1 second	$\leq$ 2 seconds
F_2	Wetting force at two seconds from the start of test	**$\geq$ 50% of maximum theoretical wetting force at or before two seconds	Positive value at or before two seconds
F_5	Wetting force at five seconds from the start of test	At or above the value of F_2	At or above the value of F_2

Table 2-2: J-STD-003B 4.3.1 Test F Wetting Balance Testing

Note: These suggested criteria have been established as a two tier evaluation format with Set A being more stringent. Components meeting Set A suggested criteria are applicable to a larger soldering process window than components meeting Set B suggested criteria. It should be recognized that components meeting Set B suggested criteria may be completely acceptable to a larger process window but the user must determine which criteria set best integrates into their process.

In addition to the criteria here, J-STD-003B requires that “the area of the test sample with fresh solder adhesion shall be greater than the area that was immersed in the solder bath (i.e. the printed board shall exhibit positive solder wetting beyond its immersion depth)”.

** $F_{(50\%\ max)}$ is 188 µN/mm for the pad areas.

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Ask the EMPF Helpline!

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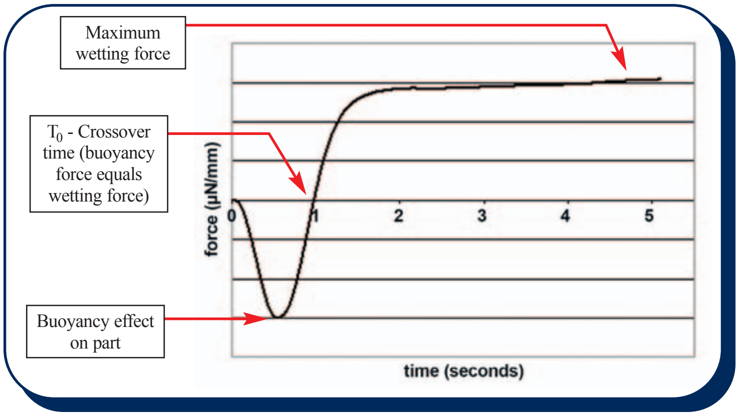
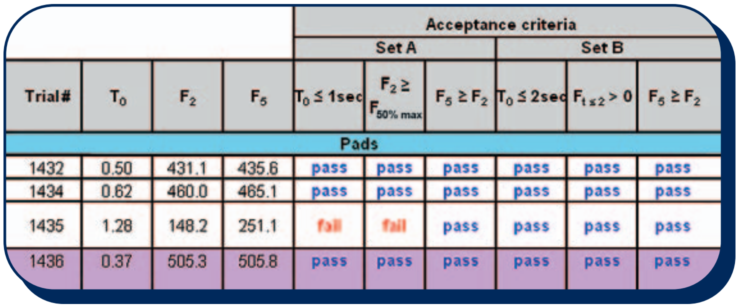


Figure 2-1: Typical Wetting Balance Curve

The panels of the PCBs displayed acceptable visual wetting. Numerical wetting balance results indicated not all the pads PCBs met the more stringent Set A criteria with one of three pads tested displaying slow and weak wetting forces when tested with the standard RMA flux, Table 2-3.



				Acceptance criteria					
				Set A			Set B		
Trial#	T_0	F_2	F_5	$T_0 \leq 1$sec	$F_2 \geq F_{50\% \max}$	$F_5 \geq F_2$	$T_0 \leq 2$sec	$F_{t \leq 2} > 0$	$F_5 \geq F_2$
Pads									
1432	0.50	431.1	435.6	pass	pass	pass	pass	pass	pass
1434	0.62	460.0	465.1	pass	pass	pass	pass	pass	pass
1435	1.28	148.2	251.1	fail	fail	pass	pass	pass	pass
1436	0.37	505.3	505.8	pass	pass	pass	pass	pass	pass

Table 2-3: Summary of Wetting Balance Results

Note: RMA flux was used in trials 1432, 1434, and 1435 while aggressive water soluble flux was used in trial 1436.

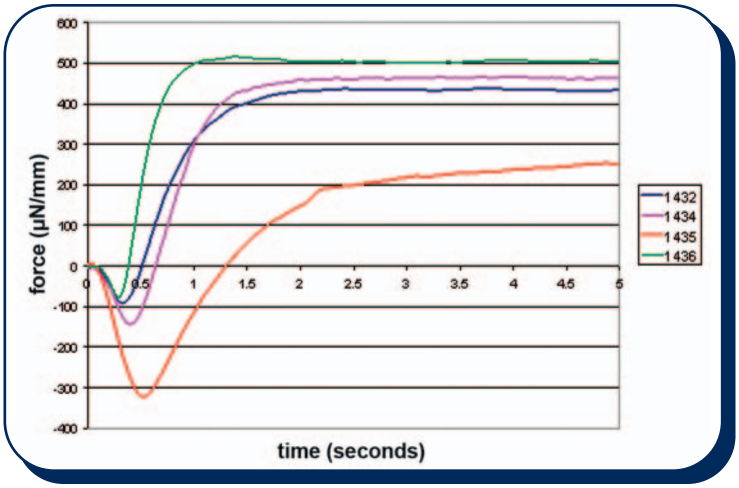


Figure 2-2: Wetting Balance Curves for PCB Pads

A difference in wetting between pads tested with the standard RMA (J-STD-004 activity: ROL1) and a very active water soluble flux (OA, J-STD-004 activity: ORH1) suggest the presence of some oxidation or hard to reduce species that could hinder wetting.

Wetting can be affected by many factors; flux type and activity, reflow conditions and how materials are stored (conditions and duration). The most likely failure mode in this case was a very short shelf life as a result of improper conditions or packaging. Further testing to include steam aging prior to solderability is recommended to determine the actual shelf life of the PCB.

Chris Deeble | Materials Engineer

Upcoming Courses

October 16-17 | *Lead Free Manufacturing*

- Gain an understanding of technical issues surrounding the lead-free soldering process.
- Learn to manufacture lead-free hardware using production quality equipment in the on-site demo lab.
- Bring samples of your hardware to evaluate responses to lead-free solders.

October 21-23 | *Chip Scale Manufacturing*

- Hands-on training utilizing advanced packaging equipment in the on-site demo lab.
- Identify and perform critical process steps when manufacturing ball grid arrays (BGAs), micro-BGAs, flip chips and chip scale packages.
- Identify and implement process control methods and practices when manufacturing assemblies with advanced packages.

Contact the Registrar for details:

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e-mail **registrar@empf.org**

Flip Chip Assembly

(continued from page 1)

signal path. Additionally, the power to ground inductance is reduced. By using flip chip interconnection, power can be brought directly into the core of the die, rather than having to be routed to the edges. This greatly decreases the noise of the core power, improving performance of the silicon. This is a key factor in high speed communication and switching devices and gives good I/O connection flexibility. A higher signal density is available with flip chip assembly. The entire surface of the die can be used for interconnect, rather than just the edges. Since a flipped chip can connect over the surface of the die, it can support vastly larger numbers of interconnects for a given die size. For a die where size is determined by the edge space required for bond pad ("pad limited") the size of the die can be reduced, saving silicon cost. In some cases, the total package size can be reduced using flip chip. This can be achieved by either reducing the die to package edge requirements, since no extra space is required for wires, or in utilizing higher density substrate technology, which allows for reduced package pitch. Flip chip assembly is a mechanically rugged interconnection method when completed with an adhesive underfill. This method also has the lowest cost interconnection for high volume automated production.

Figure 1-3: Double Stud Bump Attached with Conductive Epoxy

There are three stages in making flip chip assemblies: bumping the die or wafer, attaching the bumped die to the board or substrate, and in most cases, filling the remaining space under the die with an electrically non-conductive material. The conductive bump, the attachment materials, and the processes used differentiate the various kinds of flip chip assemblies. The most common bumping and attaching methods include solder bump, plated bump, stud bump, and adhesive bump. The bump serves several functions in the flip chip assembly. Electrically, the bump provides the conductive path from chip to substrate. The bump also provides a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump provides part of the mechanical mounting of the die to the substrate. Finally, the bump provides a spacer, preventing electrical contact between the chip and substrate conductors, and acting as a short lead to relieve mechanical strain between board and substrate.

The cost, performance, and space constraints of the application determine which method is the most suitable. A current EMPF project is focused on the development of a silicon germanium (SiGe) System on a Chip (SoC), assembled in a Flip Chip on Board (FCoB) configuration. For SiGe applications, stud bump bonding is considered to be one of the most robust packaging options given the process restrictions. The balance of this article reviews some of the more common bump attachment methods.

Solder Bump Flip Chip

The solder bumping process first requires that an under bump metallization (UBM) be applied to the aluminum chip bond pads, typically by sputtering or plating to remove the insulating oxide layer and to define the solderable area. Solder is deposited (Figure 1-2) on the UBM by needle-depositing or screen printing solder paste, evaporation, or electroplating. After solder bumping, the wafer is cut into bumped die. The bumped dies are placed on the substrate pads, and the assembly is heated to make a solder connection.

Stud Bump Flip Chip

The gold stud bump flip chip process, bumps die by a modified standard wire bonding technique. This technique makes a gold ball for wire bonding by melting the end of a gold wire to form a sphere. The gold ball is attached to the chip bond pad as the first part of a wire bond. To form gold bumps instead of wire bonds, modified wire bonders break off the wire after attaching the ball to the chip bond pad. The gold stud bump remaining on the bond pad provides a permanent connection through the aluminum oxide to the underlying metal. Gold stud bump flip chips may be attached to the substrate bond pads with conductive adhesive (Figure 1-3) or by thermosonic gold-to-gold connection.

Plated Bump Flip Chip

Plated bump flip chip uses wet chemical processes to remove the insulating oxide layer and plate conductive metal bumps onto the wafer's aluminum bond pads. In general, plated nickel-gold bumps are formed on the semiconductor wafer by electroless nickel plating of the aluminum bond pads of the chips. After plating the desired thickness of nickel, an immersion gold layer is added for protection, and the wafer is cut into bumped die. Alternatively, silver bumps are electroplated on a sputter seeded semiconductor wafer (Figure 1-4). Attachment generally is by solder or adhesive, which may be applied to the bumps or the substrate bond pads by various techniques.

Adhesive or Polymer Bump Flip Chip

The polymer bump process is a patented, stencil printing technology in which isotropically conductive, silver filled polymers are printed through metal stencils to form polymer bumps on a zincate-nickel gold, electroless plated UBM that covers the aluminum bond pads of the semiconductor die. The polymers are either thermoset which cures with heat, or thermoplastic which softens with heat. These silver-filled polymers are formulated for high precision stencil

continued on page 9

Advanced High Power, High Density Connectors

Electrical current carrying capacity is a primary concern of the design of the interconnect medium for any electronic system. This is as true for a power supply as for a radar or battlespace communications system. The performance of the interconnection carrying the required electrical current will be affected by the resistive heating of the components of the connectors and the cables. The generated resistive heating will cause a rise in temperature of the connector and cable which may eventually melt the connector or damage the system components.

Two technologies for limiting the temperatures generated by resistive electrical heating, and therefore maximizing the electrical current handling capability of the interconnect, are currently being explored by the EMPF. These technologies reduce the heat generated in a standard connector by multiplying the number of contact points between each connector pin and its socket.

For example, the standard existing connector socket has two or three leaf spring contacts that touch the connector pin in upon insertion of the pin into the socket. These are the standard bifurcated or trifurcated contact methods used in the common existing connectors (see Figure 3-1).

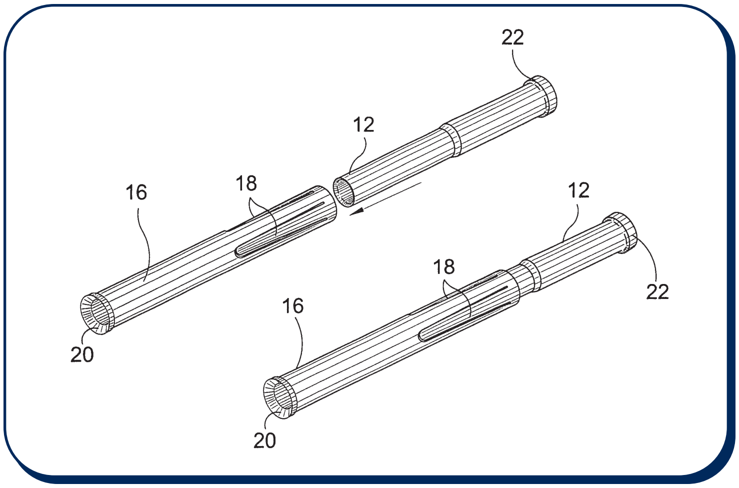

Figure 3-1: Typical arrangement of socket (20) and pin (22) in which dual leaf spring features (18) contact the pin at two places (12) after pin insertion into the socket.

In contrast, the new high current pin and socket technologies utilize tens or hundreds of contacts, rather than the standard two or three, to minimize the contact resistance of the pin in the socket and therefore minimize the resistive heating at a given current level. This lower heating rate allows for a larger current carrying capability in a standard pin size.

Figure 3-2 shows both of the two high current interconnect technologies being explored by the EMPF. Results so far are very encouraging. Resistance values using the new interconnect technologies in the sockets with standard interconnect pins show several times lower electrical resistance values than do the standard pin and socket contacts. When preliminary tests of socket contacts outfitted with the new technologies have been conducted, significant increases in current carrying capacity for a given size standard pin contact have been realized with only the standard temperature rise.

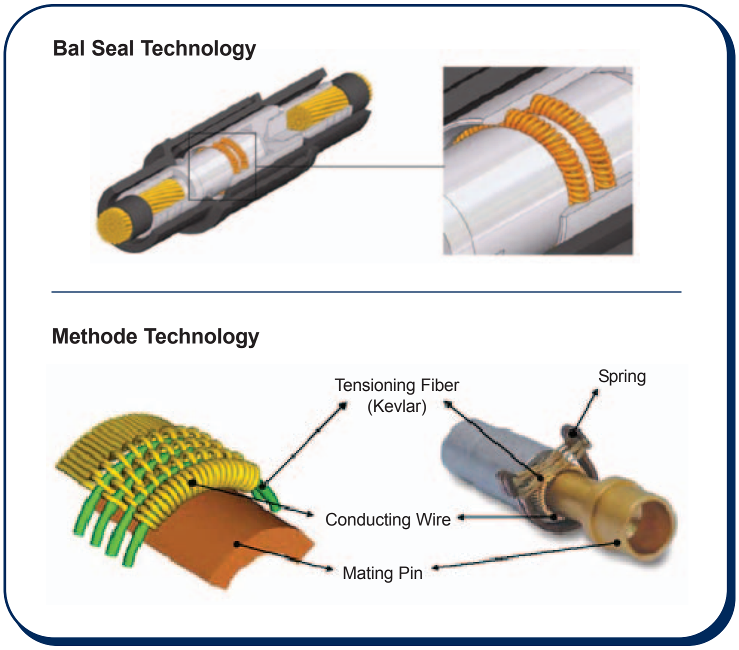

Figure 3-2: Left view shows Bal Seal technology being used to build high current connectors. Note the multiple toroidal shaped gold colored springs that multiply the number of contact points between the pin and the socket, compared to the two points in Figure 3-1. Right view shows mated pin and socket using the Methode Electronics approach having woven Kevlar fiber (green) and gold plated copper wire (gold) to accomplish similar effect. Both new contact technologies are under study by the EMPF.

Benefits of the new contact technologies will be that smaller and lighter form factor connectors will be usable for much higher currents. This allows the power distribution, that is critical for the new Navy ship designs, to be much more compact and lighter than was required using the existing style of bifurcated or trifurcated electrical contacts.

The role of the EMPF in this development is to facilitate the incorporation of this promising, commercially inspired development into critical Navy applications using military grade circular, rectangular, and "z-axis" (busbar to busbar) connectors for aboard-ship electronics. Applications to other services requirements may also be considered as the technology matures.

Fred Verdi | Senior Manufacturing Engineer

Manufacturer's Corner: Manncorp Surface Mount Technology (SMT) Line at the EMPF

As with any production line, performance is only as good as the sum of its parts. The EMPF has not just one machine from Manncorp, but an entire Manncorp line showing the full capability of a lower cost, but not lower performance SMT system. The line includes the Manncorp 1400 Automatic Stencil Printer, the MC-391V2V Dual-Head Pick and Place, a 3-Stage Conveyor, and the CR5000 Lead-Free Reflow Oven. For example, the stencil printer provides precision printing for fine pitch surface mount devices (SMDs) to 12mils, identical to the fine pitch specification of the pick and place that it interfaces. If this were not the case, the printer would not be capable of printing the pads for the complete range of components that the MC-391 is capable of mounting.

Automatic Stencil Printer with Programmable Controls

The stencil printer features a dual squeegee and dual stroke control system for the most efficient use of solder paste. All control parameters, print speed, stroke length, and squeegee pressure are fully programmable. In addition, the MC1400 can automatically align the stencil to the board with a high degree of accuracy. The printer is equipped with a flexible mounting table for quick setup and changeover of single and double-sided printed circuit boards (PCBs). Because all movements, PCB position, mounting table, and the squeegee head rely on precision linear guides, high levels of accuracy and repeatability are achieved.

Dual-Head Pick and Place with 160 Feeder Capacity

Designed for medium- to high-volume assemblers, the dual-head pick and place provides high-precision placement of the full range of SMDs, from the smallest 0201 devices through chip scaled packages (CSPs), ball grid arrays (BGAs), flip-chips, and ultra-fine-pitch (0.3mm lead pitch) quad flat packs (QFPs). Even odd-form components can be placed at rates of approximately 5500 components per hour (cph). The MC-391 features Cognex vision processing and head-mounted vision cameras for non-contact, "vision-on-the-fly" alignment of all components up to 16mm x 14mm. A bottom vision camera is used for large components up to 38mm x 38mm and devices with alignment features on their bottom side. Unlike systems that utilize laser centering methods, the Cognex vision processor, combined with a fine-resolution, linear-encoded X-Y drive mechanism, allow the MC-391 to deliver a remarkable ±.05mm placement accuracy. Not only can this system mount a wide range of parts, it also can surround the work area with up to 160 smart tape feeders, fulfilling enormous production flexibility requirements for high-mix assemblies.

One-, Two- or Three-Stage Surface Mount Equipment Manufacturer's Association (SMEMA) Inspection Conveyor

Linking the pick and place to the reflow stage is Manncorp's inline SMEMA-compatible conveyor, which is available as a one, two or three-stage transport for inspection, buffer, or pass-through. Each stage includes a programmable logic controller (PLC) 25W motor with adjustable speed control and can be used for board widths from 50mm to 400mm. Available conveyor lengths are 500mm, 1m or 1.5m.

Figure 4-1: Manncorp Pick and Place

Small-Footprint Lead-Free Reflow Oven

The CR-5000F is well suitable for medium to high volume lead-free reflow. Its small footprint of just 10ft. long, is 20-30% shorter than comparable systems, yet has five full zones of hot-air convection heating, each with independent upper and lower temperature controls. In addition, it includes a combination adjustable 550mm edge-pin/stainless steel mesh belt conveyor, three thermocouple inputs, and a computer controller with a user-friendly Windows-based operating system for precision temperature profiling. Another important feature is its timed automatic startup and shutdown modes for power management and energy conservation.

The Manncorp line is representative of high innovation at a low acquisition cost. For more information related to this article, or to schedule a demonstration at the EMPF, contact Ken Friedman, 610-362-1200 x279 or via email at kfriedman@aciusa.org.

Ken Friedman | EAB Coordinator

Tech Tips: Reflow Experiment

An experiment was recently performed in the EMPF Demonstration Factory for a customer that was interested in comparing the wetting of lead-free solders with varying temperature profiles and atmospheric conditions. In order to deliver an objective measurement of solder wetting (in addition to subjective inspection analysis), a simple wetting indicator pattern was added to the solder stencil in an area on the test vehicle that had exposed and unused copper.

This pattern comprised two rows of 22 printed solder deposits. Each individual deposit is 0.64mm x 1.27mm (0.025" x 0.050"). The deposits are paired in sets of two with decreasing gaps among each pair. The gap between each pair is constant. Figure 5-1 shows the dimensions of the printed deposits. Two rows are included in the pattern to give two replications of the measurement on each test vehicle.

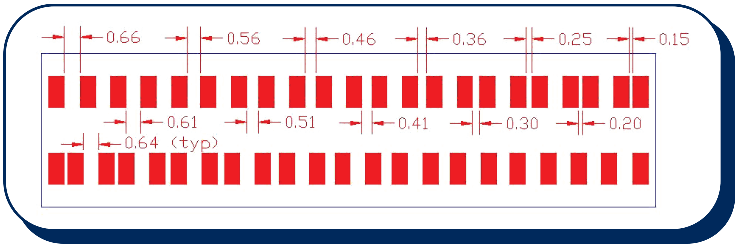

Figure 5-1: Wetting Test Pattern (dimensions in mm)

This pattern allows for two different measurements to be taken from the test vehicles after processing has been completed. The first evaluation is a count of the number of wetting pattern pairs that shorted together during reflow. As each pair of deposits is spaced further apart than the last, the number of pairs that bridge can be used to compare solder wetting under different conditions – an increasing number of bridged patterns indicates increasing wetting. Figure 5-2 shows an example of a wetting pattern after reflow, with four (4) shorted patterns.

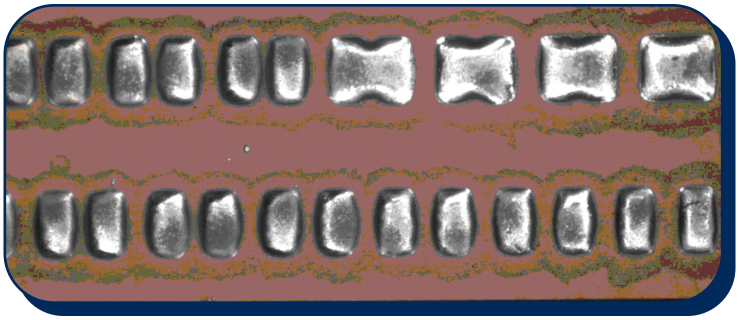

Figure 5-2: Post-Assembly Wetting Pattern

The second evaluation is a measurement of the gap between the paste deposit pair that is spaced furthest apart. This gap will decrease during reflow as the paste wets to the underlying copper and thus a smaller gap is an indication of greater solder wetting. Figure 5-3 shows an example of a paste deposit gap measurement.

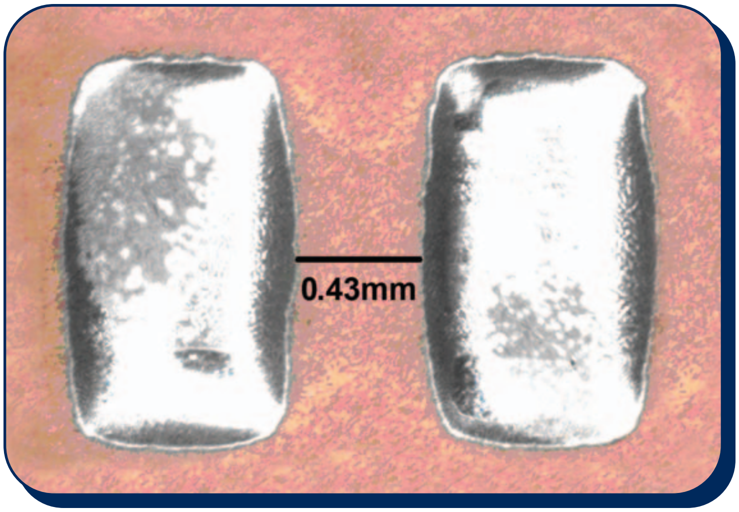

Figure 5-3: Wetting Pattern Gap Measurement

It is important to note that the printed circuit board (PCB) test vehicle was finished with OSP (Organic Solder Preservative) over bare copper and the gaps were designed with that in mind. Other surface finishes would require gaps of different sizes due to the expected wetting and spread of solder on the particular surface finish. If all of the deposits bridge, the count of bridged deposit pairs is no longer valid as a measurement and there will be no gap to measure between the last pair. For example, an ENIG (Electroless Nickel/Immersion Gold) finish, allows solders to wet and spread to a much higher degree than bare copper and would require much larger gaps in order to produce useable measurements. The solder alloy can also affect that proper spacing of this type of pattern; tin-lead solders are generally expected to wet and spread to a greater degree than their lead-free counterparts.

However, when this type of pattern is properly designed for a specific combination of materials and processes, it can be a very useful tool for process engineers that are testing the general wetting properties under varying processing environments. This evaluation method can be used on both purpose-built test vehicles as well as incorporated into an unused area of a production assembly for an easy indicator of the degree of wetting occurring between the solder and the PCB surface.

Jason Fullerton | Sr. Product & Applications Engineer

cut here and save!

Failure Analysis

Failure analysis (FA) is a term that product and quality mangers don't often wish to articulate when considering the expense and potential complexity associated with the investigatory process. Unfortunately, it is a necessity more often than not, and part of the discovery process to isolate the root cause of electronic assembly failures. Properly utilized, FA can be a tool to confirm and identify the mechanism that instigates the causes of electrical failures, such as solder joint crack propagation, dendritic growth, ionic residue, and other sources of contamination that either impede or redirect current flow. The FA lab at the EMPF has documented many such modes of failure where the origin of the problem was traced directly to a faulty manufacturing process, or a material deficiency. In some cases the designs proved to be contributors to assembly failures by exceeding the limits of the manufacturing process to produce reasonable yields.

Failure analysis can be utilized for a number of different reasons:

- **Direct Cause** – an example of this may be a cracked die or component (Figure 6-1) where the obvious cause of failure has been isolated and identified.

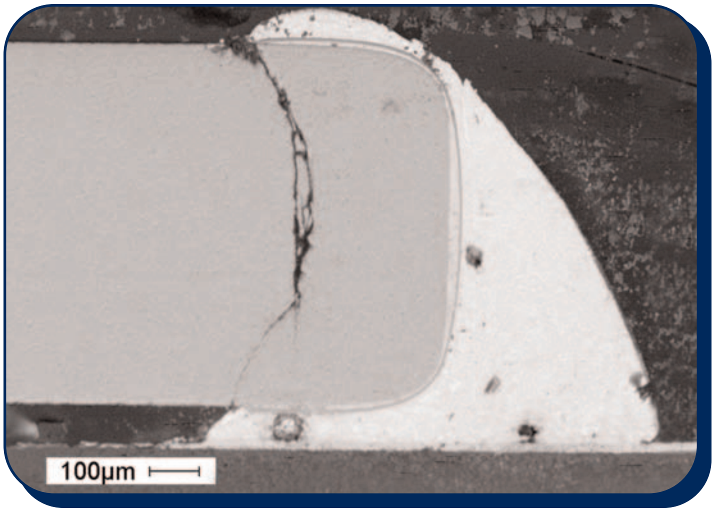

Figure 6-1: Optical Micrograph of a Cracked Component

Another such example of direct cause can be the verification of incorrect metallurgy using X-Ray Fluorescence (XRF) analysis of a component, such as a ball grid array (BGA), resulting in cold solder joints.

- **Indirect Cause** – The cleanliness of a printed circuit board (PCB) is an example where the ionic concentration is greater than the allowable IPC specification (Table 6-1), but the actual area of failure has not been established.
- **Process Indicators** – One recent example seen at the EMPF indicated that a potential for de-wetting was beginning to occur as the BGA solder balls began to recede from the pad area, even though the BGAs retained a collapsed appearance. This indicated excessive time spent in the liquidus stage.

Sample Code	Ionic Cleanliness
142	17.17 μg/in^2
155	24.81 μg/in^2
157	23.31 μg/in^2
187	31.40 μg/in^2

Table 6-1: Cleanliness Analysis of Several PWBs Using Ionograph Testing

- **Design Flaws** – An example of this would be a "via in pad" board design for BGA placement, where the micro-via exhibited insufficient copper deposition due to process limitations. As a result, imbedded air pockets were lodged directly beneath the BGA ball, where insufficient solder wetting in the micro-via entrapped the air during reflow.

Failure Detection Tools

Analytical methods for detecting failure can be segregated into two categories:

Destructive Methods – Where the sample for analysis will undergo physical or chemical changes rendering it inoperative for production use. This can be further divided into modes of detection:

- **Qualitative** – usually identifies the nature of the failure and can incorporate such methods as:
  - ***Optical or Visual Assessments*** – the use of stereomicroscopes for assessing cross sectional samples. Can be a quantitative method as well as a qualitative method.
  - ***Spectroscopy*** – can include scanning electron microscopy (SEM) analysis for identification of intermetallic boundary layers in solder joints or dendrites on the surface between two adjacent conductors.
- **Quantitative** – will ascertain the amount of the contaminant or source of failure, and in many cases identify its specific nature. Some examples are:
  - ***Inductively Coupled Plasma (ICP) Spectroscopy*** – can identify and determine the specific quantities of a given element within the sample.
  - ***SEM/Energy Dispersive Spectroscopy (EDS)*** – can quantify the thickness of particular intermetallic layers, and in some cases identify the oxidation states.
  - ***Wetting Balance*** – uses the inherent nature of surface tension against various solders and pad finishes to calculate a force of retraction as a measure of wettability.

Non-Destructive Methods – Can allow for re-use of the sample into production since the functionality of the assembly is retained. This needs to be a discretionary decision since the potential does exist for inadvertent damage through the course of analysis. Some examples of non-destructive testing are:

continued on page 9

Failure Analysis

(continued from page 8)

- **Fourier Transfer Infrared (FTIR)** – a spectroscopic method of detecting organic contamination on the surface of a substrate or assembly.
- **Ionograph** – an electrochemical method of detecting ions and measuring the total amount extracted from an assembly. Values are given as a relative quantity of NaCl.
- **XRF** – another spectroscopic method of determining alloy constituents. This is a useful tool for screening component finish and PCB metallic thickness without destructive cross-sections.
- **Ion Chromatography (IC)** – will quantify and identify specific ions in assemblies. Usually used as a process qualifier for flux and cleaning systems, where the results can be compared against the IPC specifications for board cleanliness.
- **X-Ray** – a critical diagnostic tool for contract manufacturers who assemble BGAs as a means of detecting shorts, opens and incomplete collapse of the solder balls during thermal reflow.
- **Automated Optical Inspection (AOI)** – an instrument used as a process tool for inspection and an indication of good paste deposition, component placement, and optical detection of surface anomalies on assemblies.

The EMPF training center offers courses in failure analysis that avail the students the opportunity to experience the use of many of these analytical tools. More importantly, the course is geared to assist the students in identifying the root causes of potential failures in bare boards, populated assemblies, and components, while utilizing that knowledge to select the best method of verification, and more critically, the recommended corrective actions to fix the problem. For more information on FA training, please contact the Registrar at 610-362-1295 or email registrar@empf.org.

Carmine Meola | Manager, Factory Services & Training

Flip Chip Assembly

(continued from page 4)

printing through laser etched or electroformed metal stencils. Once the bumped wafers are diced, the chips are inverted and bonded to the substrate. Final processing involves a heat cure for the thermoset bumps while the thermoplastic bump connections are made in a few seconds as heat and pressure are used to melt the thermoplastic.

Figure 1-4: Silver Plated Bumps

Flip Chip Underfill

As described above, one function of the bump is to provide a space between the chip and the board. In the final stage of assembly, this under-chip space is usually filled with a non-conductive "underfill" adhesive joining the entire surface of the chip to the substrate.

The underfill protects the bumps from moisture or other environmental hazards, and provides additional mechanical strength to the assembly. However, its most important purpose is to compensate for any thermal expansion difference between the chip and the substrate. Underfill mechanically "locks together" chip and substrate so that differences in thermal expansion do not break or damage the electrical connection of the bumps.

Underfill may be needle-dispensed or jet-dispensed along the edges of each chip. It is drawn into the under-chip space by capillary action and heat-cured to form a permanent bond.

Conclusion

The methods covered in this article are only a few of the wide range of techniques used as part of the flip chip process. The development of new techniques is proceeding continually. Flip chip assembly has been shown to have significant advantages over other microelectronic packaging methods. Several varieties of flip chip assembly, including solder bump, plated bump, gold stud bump, and adhesive bump are suitable for a wide range of applications.

Michael Barger | Senior Materials Engineer

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