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In this Issue

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Automated Testing with Boundary Scan

Boundary scan is a method for testing interconnects on printed circuit boards (PCBs) or sub-blocks inside an integrated circuit. It has rapidly become the technology of choice for building reliable high technology electronic products with a high degree of testability.

Due to the low-cost and integrated circuit (IC) level access capabilities of boundary scan, its use has expanded beyond traditional board test applications into product design and service.

What is Boundary Scan?

Boundary scan, as defined by the IEEE Std.-1149.1 standard developed by the Joint Test Action Group (JTAG), is an integrated method for testing interconnects on PCBs that are implemented at the IC level. The inability to test highly complex and dense printed circuit boards using traditional in-circuit testers and bed of nail fixtures was already evident in the mid 1980s. Due to physical space constraints and loss of physical access to fine pitch components and BGA (ball grid array) devices, fixturing cost increased dramatically while fixture reliability decreased at the same time.

Testing with Boundary Scan

The boundary scan architecture provides a means to test interconnects and clusters of logic, memories, etc. without using physical test probes. It adds one or more so called "test cells" connected to each pin of the device that can selectively override the functionality of that pin. These cells can be programmed via the JTAG scan chain to drive a signal onto a pin and across an individual trace on the board. The cell at the destination of the board trace can then be programmed to read the value at the pin, verifying the board trace properly connects the two pins. If the trace is shorted to another signal or if the trace has been cut, the correct signal value will not show up at the destination pin, and the board will be known to have a fault.

When performing boundary scan inside integrated circuits, cells are added between logical design blocks in order to be able to control them in the same manner as if they were physically independent circuits. For normal operation, the added boundary scan latch cells are set so that they have no effect on the circuit, and are therefore effectively invisible. However, when the circuit is set into a test mode, the latches enable a data stream to be passed from one latch to the next. Once the complete data word has been passed into the circuit under test, it can be latched into place. Since the cells can be used to force data into the board, they can set up test conditions. The relevant states can then be fed back into the test system by clocking the data word back so that it can be analyzed.

The principles of interconnect test using boundary scan are illustrated in Figure 1-1 depicting two boundary scan compliant devices, U1 and U2, which are connected with four nets. U1 includes four outputs that are driving the four inputs of U2 with various values. In this case, we assume that the circuit includes two faults: a short between Nets 2 and 3, and an open on Net 4. We will also assume that a short between two nets behaves as a wired-AND and an open is sensed as logic 1. To detect and isolate the above defects, the tester is shifting the patterns shown in Figure 1-1 into the U1 boundary scan register and applying these patterns to the inputs of U2. The inputs values of U2 boundary scan register are shifted out and compared to the expected results. In this case, the results (marked in red) on Nets 2, 3, and 4 do not match the expected values and, therefore, the tester detects the faults on Nets 2, 3, and 4.

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Ask the EMPF Helpline!

REACH Directive

Recently, an EMPF customer called to discuss the REACH Directive for parts being shipped to EU countries. The customer was concerned if they had to register with the EU since the parts were not directly marketed in the EU countries, but they have downstream customers who use their product in EU countries.

In June 2007, the European Union (EU) System on Registration, Evaluation, Authorization and Restrictions of Chemicals (REACH) entered into force. This new legislation substantially rewrites the current EU chemicals policy and introduces new legal obligations for the industry.

Not only chemical producers, but also downstream users of chemicals and producers of finished products are heavily impacted. Companies importing products to the EU market will have to comply with the same strict requirements as the EU companies.

Registration or authorization is a precondition to access the EU market. Ability to provide REACH compliant products will be decisive for choosing a supplier. You may gain a competitive advantage if you start preparing for compliance now.

REACH shifts the burden to industry, such that all actors in the supply chain are obliged to ensure the safety of the chemical substances they handle. The registration process requires that manufacturers and importers generate data for some 30,000 chemical substances produced or imported into the EU above one ton per year. This data should be filed in a registration dossier, which should be submitted to the European Chemicals Agency (ECHA).

For substances of very high concern, authorization will be necessary. These substances will be prioritized and, over time, included in Annex XIV. Once they are included, industry will have to submit applications to the Commission for authorization on continued use of these substances. In addition, EU authorities may impose restrictions on the manufacture, use, or placing on the market of substances causing an unacceptable risk to human health or the environment. Safety Data Sheets must be provided to downstream users by manufacturers and importers to inform them about the potential risks of the concerning substance.

The European Chemicals Agency is in charge of the day-to-day management of REACH.

Substances exempt from REACH

Some substances are exempted from REACH: radioactive substances, wastes, substances under customs supervision, and substances necessary for the interests of defense.

Chemical substances used to manufacture other chemical substances that are never separated from the mixture of other chemicals inside a closed system, are fully exempt from REACH (as non-isolated intermediates). Intermediates that are separated during the production process (as isolated intermediates) must be registered, but with simplified information requirements commensurate with their lower risk.

Substances exempt from Registration

Some substances are exempted from Registration. Substances occurring in nature, such as minerals, ores and ore concentrates, cement clinker, natural gas, liquefied petroleum gas, natural gas condensate, process gases and components thereof, crude oil, coal, and coke are not required to be registered as long as they are not chemically modified. In addition, a number of basic substances for which the hazards and risks are well known are also exempted: hydrogen, oxygen, several noble gases (argon, helium, neon, xenon), and nitrogen.

There are also exemptions from large parts of REACH for substances in food, medicinal products, and plant protection because those are regulated in specific legislation.

Polymers are, for the time being, also exempted from registration and evaluation. However, monomers must be registered.

Nanomaterials are included in the scope of REACH and should be registered and authorized.

How does REACH affect your company?

- Your company may be affected not only as a producer, importer of chemicals, but also as an importer of finished products to the EU market and downstream user of chemicals.
- Each individual case should be carefully assessed. You may be the importer for one substance and a downstream user for another.
- Assessing impact is a company specific issue; your situation is not the same as your competitor.
- No data, no market! Registration or authorization is a precondition to sell on the EU market.
- Ability to provide REACH compliant products will be decisive for choosing a supplier.

What information should be submitted?

The registration dossier should include:

Technical dossier

- Physicochemical, toxicological, ecotoxicological properties of substances
- Intended uses, human and environmental exposure
- Classification and labeling
- Proposed risk management measures, testing

Chemical safety report

- If >10 ton/year: human health, environment, exposure hazard assessment, risk characterization

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Advanced High Power, High Density Electrical Connectors

The EMPF recently cooperated with a large defense original equipment manufacturer (OEM) company on a Navy ManTech project for characterization of two new interconnection technologies that were developed by and have been introduced into commercial electronics. The purpose of the EMPF investigation was to evaluate the potential adoption of either or both of these commercial technologies into Navy electronic systems. These two current-enhanced interconnection technologies are based on the multiplication of electrical contact points in the pin-and-socket contact pair that lower the contact resistance of each such pair and thereby lowers the ohmic heating of each mated pair. The result is the enhanced ability of each of these enhanced lower resistance contact pairs in a given connector to conduct a higher electrical current than possible with conventional three or four point contact arrangement for a given temperature rise in the contact.

The first of these is the "Tribotek technology," shown in Figure 3-1, whereby gold plated copper wire and Kevlar aramid fiber are woven together. The resultant fabric lines the electrical socket contact such that each "knuckle" of the weave provides one electrical contact to the inserted pin. The Kevlar fiber is placed under tension by an added mechanical spring, which supplies the normal force for each contact.

The second of these is the "Bal Seal technology," shown in Figure 3-2. Toroidal springs (made by Bal Seal, Inc.) are inserted into the socket contacts, thereby providing one pin contact for each coil of the spring.

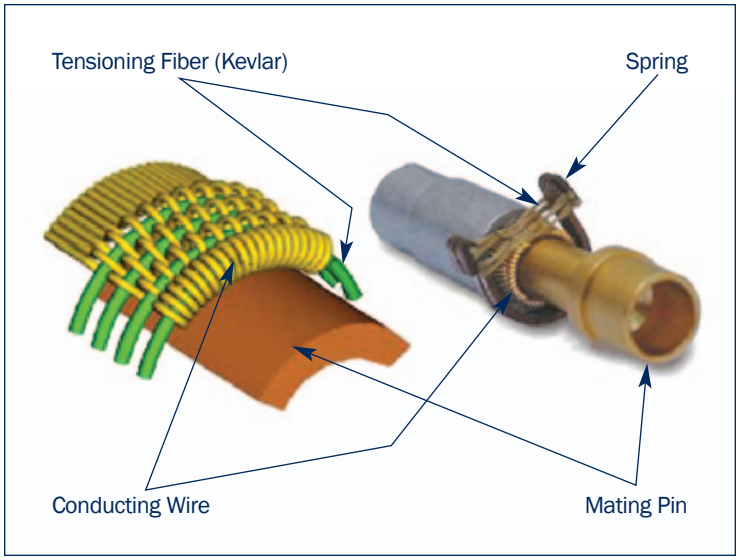

Figure 3-1: Methode Electronics (formerly Tribotek) method of utilizing woven gold plated copper wire and Kevlar fiber "fabric" with the Kevlar under spring tension to multiply the number of contacts to a conventional mated pin contact.

Several springs can then be utilized in each socket so that there are hundreds of contacts at each pin-socket pair. Just like in the Tribotek case, the multiple contacts at each mated pin-socket pair drastically reduces the total electrical resistance of the pin to the socket. This drastically reduces the resistive heating of the contact and the connector as a whole will be capable of carrying vastly more electrical current than the conventional connector having two or three contact pin-socket mated pairs.

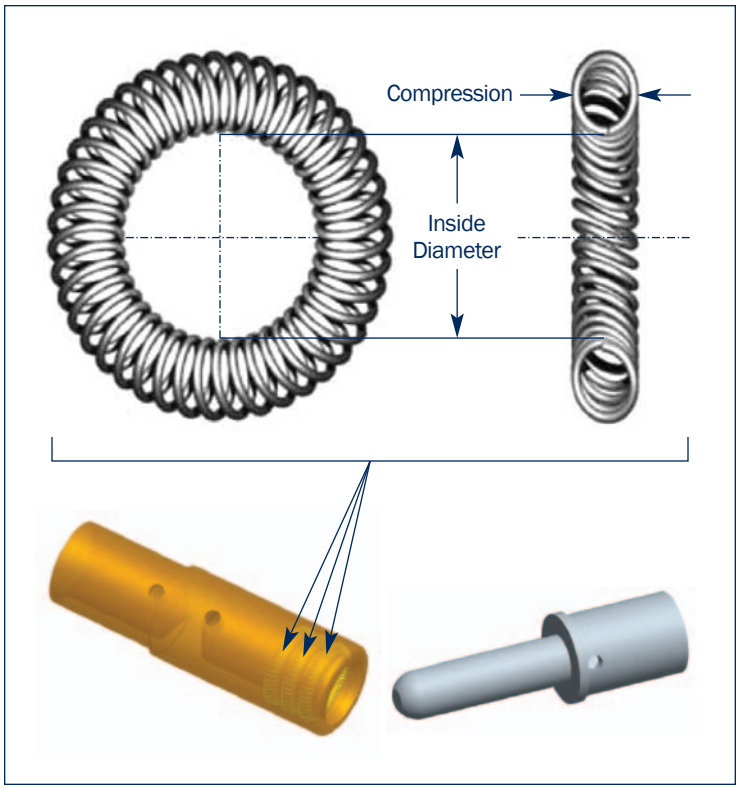

Figure 3-2: Bal Seal technology in which several toroidal shaped springs are inserted into individual sockets for the standard pin contacts. Each coil of each spring gives a contact point to the pin and socket mated pair. The mated pair then exhibits much lower contact resistance and therefore much lower heating for a given current flow than the conventional (two or three contact point) mated pair.

Fred Verdi | Senior Manufacturing Engineer

Tech Tips: COTS Challenges in a Military Environment

In order to rapidly insert the latest technology and maintain our technological lead, commercial-off-the-shelf (COTS) components are increasingly incorporated into military applications. Not only does this significantly reduce the design cycle time to rapidly introduce equipment into the battlefield, it addresses the shrinking DoD market share and the declining supplier base for "Mil-Spec" components.

However, some COTS products may not hold up to harsh military environments and use. Many applications require COTS component modifications to meet the military environmental (MIL-STD-810), power (MIL-STD-704), and EMI (MIL-STD-461) standards.

Testing can determine a method in which COTS parts can be utilized in harsh conditions. The following example (Figures 4-1 through 4-3) shows a modification which meets MIL-STD-810F Method 509.4 for Salt Fog Testing. Sample specimens were shielded by the "device under test" and subjected to salt fog. The images show the corrosive effects due to electromechanical reaction and accelerated stress corrosion or formation of acidic/alkaline solution following salt ionization in water.

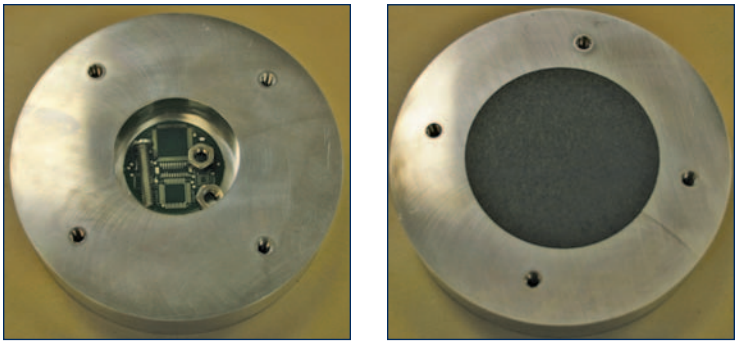

Figure 4-1: On the left, test specimens including a PCB, bolts and nuts. The image on the right shows the sealed shield.

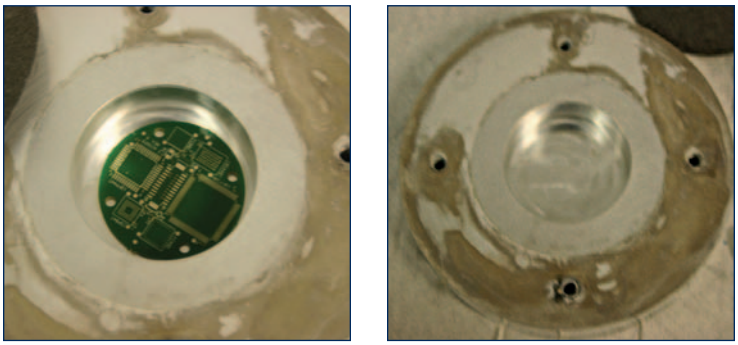

Figure 4-2: After being subjected to 48 hours of salt fog and dried outside the chamber for an additional 48 hours, these images show the effects of corrosion on the shield.

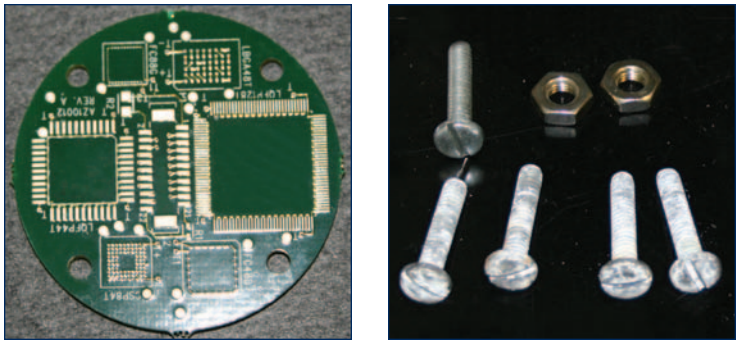

Figure 4-3: The test PCB shown at left, as well as the bolt and nuts in the top portion of the picture on the right, are free from corrosion. The bolts in the lower portion of the photo to the right show the effects of corrosion.

The following are some issues that a designer would have to consider when using COTS parts for the DoD, Navy, and Army.

- Pure tin plating should be avoided on COTS parts. It can cause the growth of tin whiskers. Refer to the Government Electronics and Information Association (GEIA) standards for guidelines on the use of lead free materials in military electronics modules.
- COTS connectors should be replaced with military qualified connectors to meet environmental and vibration requirements. In cases where COTS connectors can not be replaced due to special circumstances, a hard wire connection or a locking mechanism should be added to prevent loosening in a harsh environment. Applying shock absorbers or wire rope isolators to the design would also help with shock and vibration.
- Integrated circuits (ICs) that fall outside the temperature range for military operations should be replaced. Typically, commercial parts operate in a temperature range from 0-70°C while the military requires a -40°C to +85°C operational range. If the commercial ICs can not be replaced, a cooling or heating system must be used to ensure the ICs operate within the full military temperature range.
- Filters may be required to ensure COTS components pass radiated and susceptibility testing. A Pi filter or others such as a C filter, LC filter, ferrite beads, or inductor may be needed for power and signal lines. To save space, some manufacturers implement these filters within a custom connector, but these can be costly.
- Openings for all enclosures must be minimized to prevent radio frequency signals from entering the internal circuitry.
- Shielding on external cables is needed to reduce radio frequency coupling onto signal lines.

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Manufacturer's Corner: Kyzen Corporation

There are two key issues facing electronic cleaning processes today as assemblies, and the modern solder materials we use to assemble them, continue to evolve.

First, modern assemblies involve a wide range of component sizes that often share one thing in common – they are placed at very low, near zero standoff heights. This presents a real challenge for cleaning materials to remove all residues from such tight spaces.

Kyzen Corporation, a cleaning chemistry partner to the EMPF, is an expert in providing cleaning solutions to both military and commercial customers. Several years ago, they developed a low standoff test card to study the effects of different cleaning agents and mechanical energy configuration to achieve what they call z-axis cleaning. As component geometries decrease, the challenges for successful removal of flux and other contamination caught under the z-axis increases. After thousands of low standoff cards and several technology generations, cleaning these difficult z-axis areas is simply routine. Whether the use of these chemistries are introduced in batch or in an inline process, the improved cleanliness results in higher quality, better first pass yields, and lower operating costs.

The second key issue is that as manufacturers work with changing components and materials, the cleaning processes parameters have gradually changed to keep pace. To address these changes, process temperatures often increase and exposure time to the cleaning materials may increase as well. This is where modern cleaning agent design, including a robust inhibition package to protect the various materials on an assembly, is critical. In the mid 90s, Kyzen developed a proprietary test card to evaluate surface cleanliness, as well as surface finish, following a cleaning process. Their proven success – after almost two decades of dedication to board and system cleaning technology – makes Kyzen a valuable partner to the EMPF and the industry as a whole.

Of course, not every board is a new design or new production. A few years ago in the aftermath of Hurricane Katrina, the EMPF was tasked to recover some important assemblies that had been in storage in the greater New Orleans area. The goal was to clean and remove any contamination risk due to the ill effects of the storm. Using the Kyzen chemistry in an inline process, the EMPF was able to achieve that goal in a single pass. This, and countless other successes, show the value and necessity of cleaning chemistry manufacturers like Kyzen.

Figure 5-1: Kyzen features a large variety of cleaning chemistries.

To learn more about the various cleaning chemistries of Kyzen or to schedule a live demonstration, please contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.

Ken Friedman | EAB Coordinator

IPC J-STD-001D Requirements for Soldered Electrical and Electronic Assemblies

J-STD-001D is a process document that establishes a set of criteria for the manufacturing of electronic assemblies to a degree of reliability dependent upon the end use of the product. The criteria encompass a broad spectrum of products from general purpose electronics (designated as Class 1), to dedicated service electronics (designated Class 2), and to high performance electronics (designated Class 3). To ensure consistent levels of quality during the manufacture of a product, the document focuses on a process control methodology being incorporated into the manufacturing process.

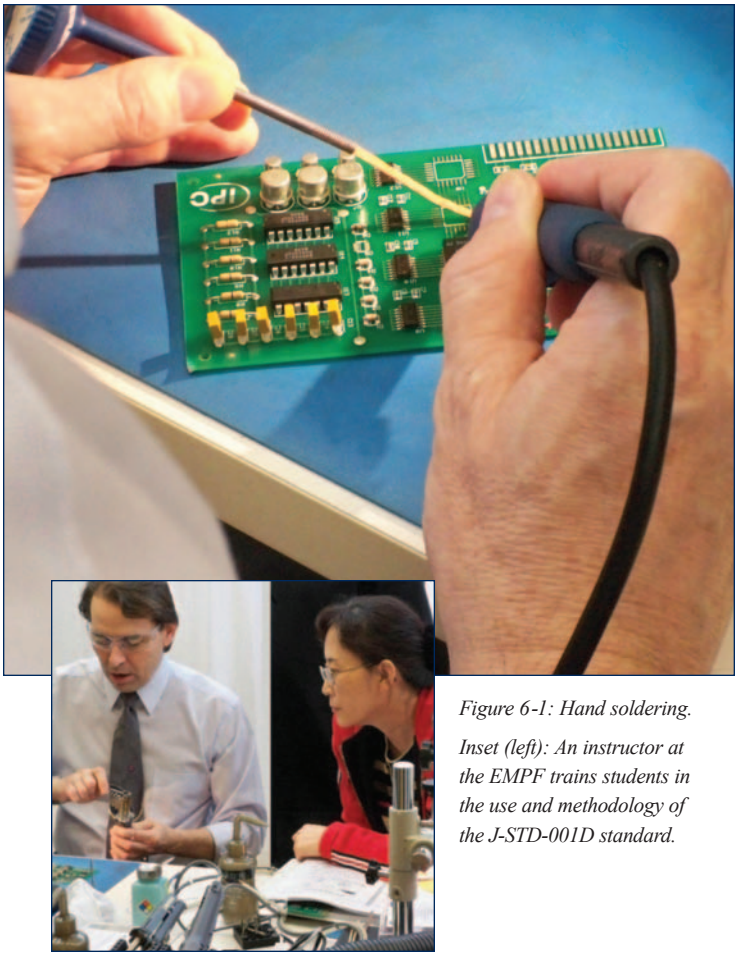

Figure 6-1: Hand soldering.

Inset (left): An instructor at the EMPF trains students in the use and methodology of the J-STD-001D standard.

The EMPF offers training in the use of this standard and its associated methodology in the J-STD-001D Certified IPC Specialist (CIS) course (Figure 6-1 inset). This course consists of five modules that can be taught over a one to five day duration (depending upon the number of modules chosen). The first module is mandatory and all subsequent modules are optional and dependent upon the successful completion of the first.

- Module One: covers general requirements, materials, components, cleanliness, assembly, and soldering process criteria. Successful completion is dependent upon passing an open book exam, as well as, a closed book exam with a combined average of 70% or better and no single score less than 60%.
- Module Two: (optional) covers terminals and wire connections and includes (but is not limited to) specifications regarding wire preparation, wire wrap, soldering and inspection of stranded wire to various terminal connections.
- Module Three: (optional) covers installation, soldering, and inspection of through-hole connections (both supported and unsupported).
- Module Four: (optional) covers mounting, soldering, and inspection requirements for surface mount components.
- Module Five: (optional) covers inspection criteria.

All the optional modules require that the student pass an open book exam with a score of 70% or better.

Students will learn the differences between the three classes of product, how to navigate the standard, how to interpret the requirements of the standard and become familiar with the terminology used. Workmanship skills assessment is used with modules two through four and inspection skills are developed through a practical exercise in module five. The student must perform wire and component preparation, and then hand solder (Figure 6-1) a variety of terminations. The soldered connections have to meet Class 3 requirements of the J-STD-001D. It is also required that half of the soldered connections be accomplished using lead-free solder.

Upon successful completion, the student will receive a certificate valid for two years from the date of issue in the areas where proficiency is demonstrated. The certification is a portable credential which is issued to the individual. Candidates for training in J-STD-001D may include (but are not limited to): assemblers, technicians, engineers, inspectors, or anyone involved in the manufacturing process who will not be training others (a separate course is taught for instructors).

Employees who attend this training program will be better equipped to apply an established regimen of criteria known for producing quality electrical and electronic assemblies within a manufacturing environment. For further information, please contact the EMPF registrar at 610.362.1295 or registrar@empf.org.

Ross Dillman | Technician/Instructor

Automated Testing with Boundary Scan

(continued from page 1)

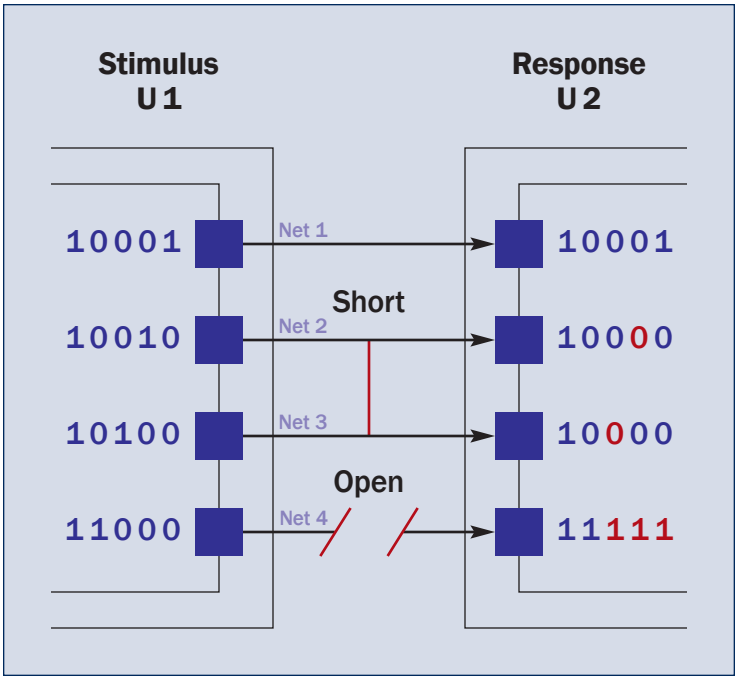

Figure 1-1: Interconnect Test Example

By adopting this technique, it is possible for a test system to gain test access to a board. As most of today's boards are very densely populated with components and tracks, it is very difficult for test systems to access the relevant areas of the board to enable them to test the board. Boundary scan makes this possible.

Debugging with Boundary Scan

While it is obvious that boundary-scan based testing can be used in the production phase of a product, new developments and applications of the IEEE-1149.1 standard have enabled the use of boundary scan in many other product life cycle phases. Specifically, boundary scan technology is now applied to product design, prototype debugging and field service.

A large proportion of high end embedded systems have a JTAG port. ARM [Advanced RISC (reduced instruction set computer) Machine] processors come with JTAG support, as do most FPGAs (field-programmable gate arrays). Modern 8-bit and 16-bit microcontroller chips, such as Atmel AVR and TI MSP430 chips, rely on JTAG to support in-circuit debugging and firmware reprogramming (except on the very smallest chips, which don't have enough pins to spare and thus rely on proprietary single-wire programming interfaces).

The PCI (Peripheral Component Interconnect) bus connector standard contains optional JTAG signals on pins 1-5; PCI-Express contains JTAG signals on pins 5-9. A special JTAG card can be used to re-flash corrupted BIOS (Basic Input/Output System). In addition, almost all complex programmable logic device (CPLD) and FPGA manufacturers, such as Altera, Lattice and Xilinx, have incorporated boundary scan logic into their components, including additional circuitry that uses the boundary scan four-wire JTAG interface to program their devices in-system.

Boundary Scan Applications at the EMPF

The EMPF has successfully incorporated boundary scan, or JTAG into its numerous designs for U.S. Army and NavAir projects. The use of onboard JTAG ports in the designs involving Xilinx CPLDs and FPGAs allows design engineers at the EMPF to have the flexibility to program the parts and change their logic on-the-fly without powering down the board. Additionally, by utilizing Xilinx ChipScope, an embedded software based logic analyzer and virtual input and output controller through JTAG, the EMPF engineers have great convenience in examining, analyzing and manipulating the internal logic of their FPGA designs.

Summary

Boundary scan is a widely practiced test methodology that is reducing costs, speeding development, and improving product quality for electronics manufacturers around the world. By relying on an industry standard (IEEE 1149.1), it is relatively quick, easy, and inexpensive to deploy a highly effective test procedure. It saves design time and adds new value added capabilities to the design, which contributes to the overall effect of significantly reduced product development and support costs.

For more information about boundary scan or any other services offered at the EMPF, contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.

References:

http://standards.ieee.org/reading/ieee/std_public/description/testtech/1149.1-1990_desc.html

http://www.jtag.com/

http://www.corelis.com/products/Boundary-Scan_Tutorial.htm

http://www.xilinx.com/support/documentation/topicfpgafeaturedesign_bscanjtag.htm

Yinhao Wu | Senior Design Engineer

Ask the EMPF Helpline!

(continued from page 2)

Timeline for registration

The deadline for registration is the same for substances on their own, in preparations, and in articles. They depend on:

- The volume of the substance produced or imported per year
- Substances classified below should be registered by 2010
  - CMRs (Carcinogens, Mutagens and substances toxic to Reproduction) >1ton/year
  - vPvBs (very Persistent and very Bioaccumulative substance)
  - R50-53 >100ton/year
    - R-Phrases (short for Risk Phrases) are defined in Annex III of European Union Directive 67/548/EEC: Nature of special risks attributed to dangerous substances and preparations.

      R50: Very toxic to aquatic organisms

      R51: Toxic to aquatic organisms

      R52: Harmful to aquatic organisms

      R53: May cause long-term adverse effects in the aquatic environment

2007	June 1	REACH program began.
2008	June 1	European Chemical Agency becomes fully operational.
	June - December	Pre-registration for phase-in substance started:*
2010	November	Registration deadline for vPvBs or CMRs >1 ton/year or R50-53 >100 tons.
2013	June	Registration deadline for R50-53 or substances in quantities >100 tons.
2018	June	Registration deadline for substances in quantities of one ton and more.

**Any new substances will need a registration dossier submitted before they are placed on the market. Voluntary registration prior to deadlines is possible.*

If the substances you are producing or importing are classified as CMRs, PBTs, or vPvBs and are included in Annex XIV, you must ask for an authorization for your specific use. The request for authorization should be sent to the Commission.

Authorization dossier should include:

- Chemical safety report
- Analysis of the alternatives considering their risks and the technical and economic feasibility of substitution
- Research and development activities by the applicant
- Substitution plan including a timetable for proposed actions by the applicant

Authorization dossier may include:

- Socio-economic analysis
- Justification for not considering risks to human health and the environment arising either from emissions or discharges
- The European Commission grants authorization assisted by the Agency and a Committee

Authorization of use is granted if:

- Risk to health and environment is controlled, including discharges, emissions, and losses
- Socio-economic benefits outweigh risk and no suitable substitutes available

Authorization is time limited and subject to review. Exemptions of use are granted if EU legislation provides for requirements and management measures related to heath and environmental protection, and risk is controlled.

Reporting

Under REACH, certain information should be communicated to your suppliers, customers, and public authorities.

Reporting to suppliers

- Your company has the right to make use known to supplier of substances
- You have the obligation to identify exposure scenarios and measures to control risks

Reporting to customers

- Safety Data Sheets are to be submitted to your customer
- You must inform your customers of the presence of Hazardous Substances contained in a concentration > 0.1% by weight, even if the total annual volume is less than 1 ton/year

Reporting to authorities

- The European Chemicals Agency
- The Commission
- Member States Authorities

Your company has the obligation to keep and update information.

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Ask the EMPF Helpline!

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For more information on REACH Directives, or other classes available from the EMPF, including IPC certifications, please contact the registrar at 610.362.1295 or via email at registrar@empf.org. Course descriptions can be found on the web at www.aciusa.org/courses.

Anand Bhavankar | Senior R&D Engineer

Tech Tips: COTS Challenges in a Military Environment

(continued from page 4)

The benefits from using COTS components are worth the adaptations required. COTS parts allow applications to stay current through spiraling refinements, faster fielding, and accelerated implementation. By adapting to COTS insertion, we can reduce the typical defense system development cycle and provide numerous technology refresh and insertion points throughout the product lifecycle including sustainment.

The EMPF offers an array of testing and analytical services to be certain that your COTS parts can perform in harsh environments and extreme conditions. Please contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.

Thuan Dinh | Design Engineer

Free Workshop: PACE Worldwide and Vision Engineering

Wednesday, July 15, 2009; 10:00 am to 2:00 pm | 1 International Plaza, Suite 600, Philadelphia, PA 19113

Complimentary lunch is provided.

Shrinking PCB and component footprints, heavy ground planes, and lead free solders are just a few of the challenges in today's PCB world. **PACE Worldwide** has designed their products to meet these demands and we would like to share this with you. This presentation will show you how PACE products were designed to efficiently, safely and properly meet these challenges that will continue to impact our marketplace!

Microscopes, or optical inspection equipment, are used in many market segments and have a number of different applications. Other than the obvious magnification of objects that cannot readily be viewed by the naked eye, optical inspection equipment is an invaluable tool to users. **Vision Engineering's** presentation will discuss the ergonomics of stereo microscopes, the advantages of dynascopic technology, and increased production possible through their use.

John Romanowicz is the National Sales Manager for PACE and has over 11 years in the electronics assembly, rework and repair markets. Spending the last 4.5 years with PACE and the previous 6.5 years as a PACE distributor, John has extensive product knowledge and real life application experience. He is a Penn State graduate, with a BS in Business Logistics.

As National Sales Manager, **David Marks** is responsible for the growth of the Vision Engineering product line. He has served Vision Engineering for 13 years in this capacity and is responsible for North American sales and distributor relations. David holds a BS in Chemical Engineering from the University of Massachusetts and an MBA from Boston University.

RSVP via: *phone* **610.362.1200, ext. 609** | *e-mail* **registrar@aciusa.org** | *online* **www.aciusa.org/workshop**

ACI Technologies, Inc.

National Electronics Manufacturing Technology Center of Excellence

Class Schedule for the Calendar Year 2009

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CIT Certification
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July 6-10
August 10-14
September 14-16
October 12-16
November 2-6
December 14-18

IPC J-STD-001
CIT Recertification
January 14-15
March 25-26
April 29-30
June 17-18
August 26-27
September 23-24
October 28-29

IPC A-610
CIT Certification
February 23-26
March 16-19
June 8-11
July 6-9
August 17-20
October 19-22
December 7-10

IPC A-610
CIT Recertification
January 12-13
March 23-24
April 27-28
June 15-16
July 27-28
August 24-25
September 21-22
October 26-27
November 30 - December 1

IPC A-600
CIT Certification
January 20-22
April 6-8
July 20-22
August 31 - September 2
November 16-18

IPC 7711/7721
CIT Certification
March 2-6
June 1-5
August 3-7
November 9-13

IPC 7711/7721
CIT Recertification
February 23-24
May 4-5
July 13-14
September 28-29

High Reliability Addendum

IPC J-STD-001 DS
CIT Certification
January 16
May 1
August 28
October 30
December 4

Skills

Chip Scale Manufacturing
March 2-4
May 13-15
August 3-5
December 2-4

BGA Manufacturing, Inspection, Rework
January 5-6
April 20-21
July 13-14
September 14-15
December 7-8

Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing
March 9-10
May 11-12
July 27-28
September 16-17
November 30 - December 1

Design for Manufacture
January 12-13
April 27-28
July 20-21
September 21-22

Failure Analysis and Reliability Testing
February 9-11
April 6-8
June 29 - July 1
August 31 - September 2
November 16-18

IPC® Training Center

All courses and dates subject to change without notice.