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Advanced Packaging of SMT Assemblies for Greater Cost Reduction

Legacy electronics assemblies, such as through-hole (Figure 1-1) and connectorized component packages, are robust and prevalent throughout industry. However, each of these assembly methods have reached their limits in terms of weight, volume, reliability, and most importantly cost. With cost reduction of assemblies now the primary focus area throughout the electronics industry, there is more of a need than ever to implement the latest advancements in surface mount technology (SMT) into electronics assembly designs. Although SMT has been utilized in the electronics industry for many years, implementation of the technology is still in the ever-evolving process of reducing component footprint size, component spacing, and component I/O pitch. Implementation of the most up-to-date SMT processes provides optimal weight, volume, and cost savings, for any type of assembly.

The use of SMT components in electronics assembly designs significantly minimizes real estate on a printed circuit board (PCB). SMT components are significantly smaller than their standard through-hole, or leaded, component counterparts. They can be one-quarter to even one-tenth of the size and weight of a leaded component. Since SMT components are attached using small solder joints,

they must be small and lightweight. Smaller component size means smaller component footprint, and less occupied PCB real estate. This results in much greater circuit densities. Figure 1-2 shows an example of an assembly using SMT. The resistors and capacitors occupy considerably less real estate than those shown in Figure 1-1.

SMT components also allow for denser routing within the internal PCB layers. In the case of through-hole PCBs, any circuitry on internal layers must be routed around the through-holes, adding complexity to the design. Internal circuitry of a SMT PCB doesn't have the through-hole restrictions, so traces can be routed with higher density. Likewise, a lack of through-holes allows for the capability of mounting more components on the backside of the PCB. Increasing the circuit density of the PCB results in a significant size reduction of the assembly, as great as four times smaller, with lower material costs. Additionally, SMT components can cost around one-half to one-quarter to that of its leaded counterpart. The savings are even greater when compared to connectorized packaged components, which also require connectors and cabling as their interconnects. This is especially compelling data for assemblies that contain many individual components.

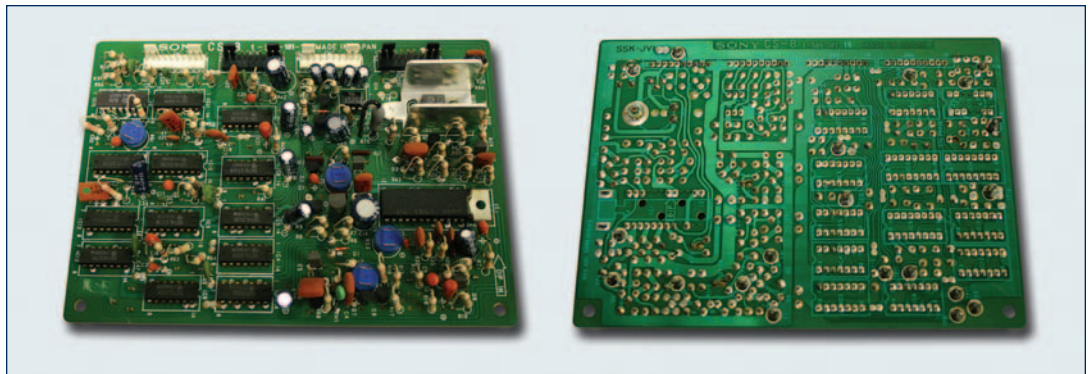


Figure 1-1: Traditional Through-Hole Assembly

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Ask the EMPF Helpline!

Failure Analysis Lab Call

Recently, a customer contacted the EMPF helpline to conduct solderability testing per J-STD-002C Test S (4.2.5) on several ball grid array (BGA) components for analysis.

Using the appropriate stencil thickness for the BGA lead pitch, and the temperature/time reflow parameters for the IR/convection reflow oven, testing simulated actual surface mount component performance in a reflow process. At the conclusion of testing, an inspection revealed failures which required the use of several analytical techniques to determine the source of the problem.

To pass optical inspection at 10x magnification, all leads must have a continuous, 95 percent defect-free solder coating in the critical areas. In addition, the BGA leads must be wetted in a consistent and unified manner, with no indication of surface oxidation anomalies. Optical microscopy, shown in Figure 2-1, revealed the existence of black residue around the periphery of one solder ball, and a smaller solder ball affixed directly to the main solder ball body. The presence of this defect and the residue were indicative of a possible contamination issue which required additional analysis.

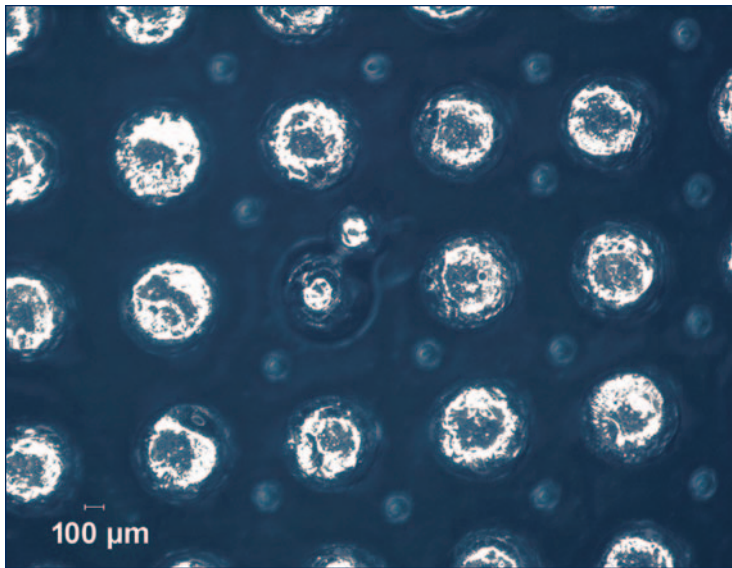


Figure 2-1: Optical micrograph of BGA defect showing small solder ball attached to main solder ball and black residue around periphery.

A Scanning Electron Microscope (SEM) was used to examine the solder ball arrays under enhanced magnification. By using backscattered electrons (BSE), regions with elements having a higher atomic number appear brighter than regions with lower atomic number elements. BSE analysis of the failed component revealed contrasting bright and dark regions on the ball, indicative of different elements present on the surface (Figure 2-2). As a control, components that had passed the solderability testing criteria were also examined. These ball arrays displayed uniformly dark colored regions, indicating a homogeneous chemical composition.

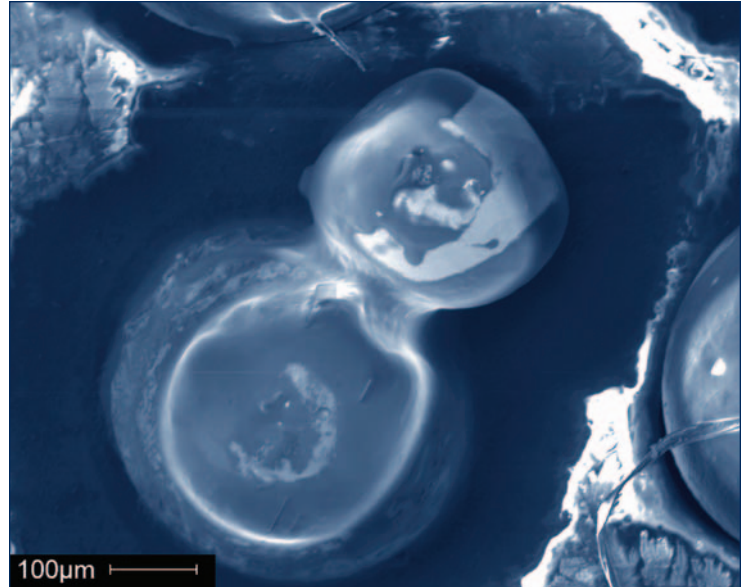


Figure 2-2: Backscattered electron SEM image of the solder ball defect clearly shows regions of different chemical composition.

To characterize the elemental compositions present, energy dispersive x-ray spectroscopy (EDS or EDAX) analysis was required. EDS is a technique using the electron beam in the SEM to determine the identity and the relative quantities the elemental constituents. The EDS analysis of the darker areas of the control component determined that both carbon and oxygen were present (Figure 2-3), an indication of an organic contaminant. The contrasting brighter region displayed the expected presence of tin and lead on the solder ball. Additional analysis of the dark regions also indicated the presence of sodium, calcium, fluorine, magnesium, silicon, aluminum, chlorine, iron, and potassium. After cleaning several of the components to remove the residue, the tin-lead microstructures became readily apparent; further demonstrating that the dark regions may be indicative of a cleanliness problem.

To identify the organic contaminants, Fourier Transform Infrared (FT-IR) spectroscopic analysis was performed. Through adsorption of infrared radiation at specific frequencies, chemical functional groups in a sample can be determined. FT-IR can rapidly produce an infrared spectrum of a sample by using interference techniques and mathematical analysis. By comparing the unknown spectrum to a database of known chemical spectra, identification of chemical compounds can be determined. In this case, the FT-IR spectrum of the sample had peaks similar to a surfactant used in a variety of cleaning products.

continued on page 8

Fixturing for Selective Soldering

Once upon a time, all printed circuit board (PCB) assemblies were designed with the same basic construction. The “primary side” was the installation side for through-hole components and contained surface mount technology (SMT) components while the “secondary side” had exposed pins for through-hole components and might have some SMT components. The process engineer was faced with a very basic assessment when determining the correct assembly method. Most assemblies were processed in the same way. The secondary side had glue dots applied, SMT components installed, and the glue was cured (if SMT components were present). Then, the primary side had solder paste applied, SMT components installed, and the solder was reflowed. This was followed with through-hole installation and wave soldering. The biggest concern for process engineers dealing with the through-hole components was controlling solder shorts and ensuring design engineering understood how to optimize the design for wave soldering.

Unfortunately, the “good old days” of straight-forward mixed-technology design is mostly a thing of the past. Today, electronic assemblies are more complicated and have smaller and smaller form factors. This forces both SMT and through-hole components to take residence on both sides of an assembly. Many designs are highly integrated, with the vast majority of parts taking SMT form. However, there are some parts that don’t lend themselves to an SMT package, such as beepers, switches, and user access connectors. Multi-image panels are utilized for many designs in order to maximize the efficiency of the PCB construction and assembly. This can create a situation where it is impossible to control co-planarity of the entire panel due to its overall width. All of these factors are driving the assembly industry to adopting “selective soldering” processes.

Selective soldering refers to the direct application of solder to specific areas of a PCB to form through-hole solder joints, rather than the “all or nothing” approach used in wave soldering. There are a variety of processes that fall under the heading of selective soldering. These

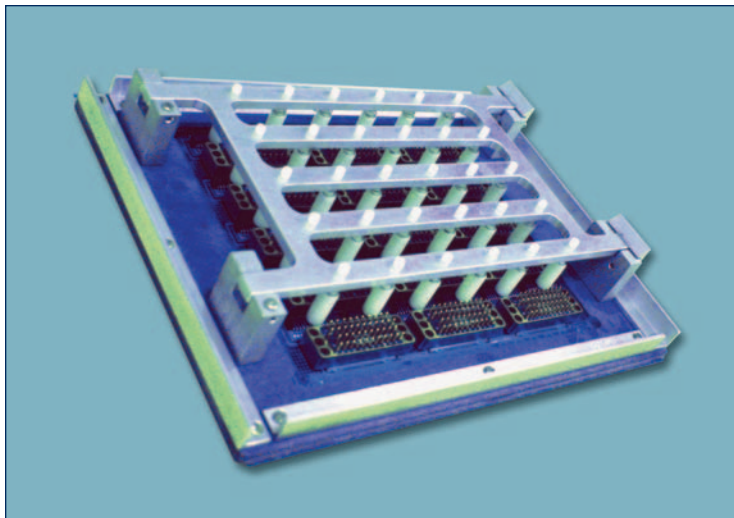


Figure 3-1: Masking pallet firmly holds the board in place from top side.

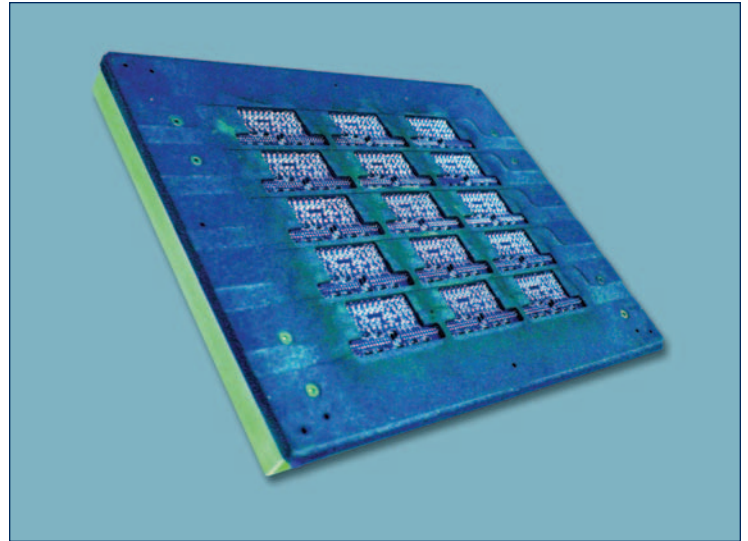


Figure 3-2: Bottom side of board is masked to only allow exposed pins to see the solder wave.

include robots that mimic hand soldering processes (a programmable solder iron and solder wire feeder), robots that use lasers and solder wire to form solder joints, programmable machines that precisely solder by moving a mini-wave solder pot or assembly to specific locations, and masking pallets that expose only specific locations of the board to a standard solder wave.

Palletized selective soldering is an excellent way to introduce more complicated product designs that stray from the standard mixed technology design, with little investment in time and money. In most cases, the wave solder equipment is already part of the existing assembly process. The process knowledge may already exist with the personnel, equipment maintenance procedures, and raw material supply already present. Masking pallets typically cost less than \$1000 each and can be sourced from a number of commercial suppliers, or designed and fabricated in-house. Even with a low percentage of assemblies that require selective solder, wave solder equipment can still be utilized for standard designs. Processing pallets over a solder wave require only minor adjustments that can be changed in a matter of minutes.

Masking pallets can generally only accommodate a single assembly per pallet design, so care must be taken to ensure a relatively stable design before investing heavily. Depending on the size of the wave solder machine, typically, no more than ten pallets are required for a fully developed application. Pallets can force designs to use larger keep outs for non-wave parts as the solder is indiscriminately applied to the entire exposed area. The pallet must be completely seated to the board to prevent solder leakage into areas that should be shielded from the wave. This requires a sufficient clear area around the exposed portion of the assembly to allow sealing with the pallet.

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Tech Tips: Battery Selection

Battery selection should be considered early during the design phase of affordable electronic systems. The important choice of an appropriate battery can reduce system acquisition costs and keep logistics support costs down for the life of the system.

Battery Selection Considerations

Operational voltage: At what voltage will the system operate? Batteries are rated for a nominal voltage, which is the average voltage the battery produces from full charge to end of discharge. Design your system to operate properly over the full voltage range of the battery to maximize the energy capacity for your system.

Typical run time: How long does the system need to run before replacing or recharging the battery, or shutting down the system? High power requirements, high operational voltage, and long runtimes mean larger batteries.

If small, lightweight batteries are required – such as for soldier carried communications systems – consider power management in your system design. Try to minimize power consumption when the system is on standby or running routine functions.

Operating environment: Will the system be required to run outside in extreme cold (winter in Alaska) or extreme heat (summer in the Middle East)? If so, select a battery that can operate at extreme temperatures.

Single use (primary) battery or rechargeable (secondary) battery (Table 4-1): Consumer grade, single use batteries such as AA and D alkaline cells are inexpensive. The logistics cost of supplying warfighters at long distances from a supply depot, may significantly add to the cost of a “cheap” consumer grade primary battery and therefore increase the lifetime cost of the system. When the system is used at the end of a long supply chain, a rechargeable battery may initially cost a little more, but re-supply costs will be reduced. Consider a system design that allows either rechargeable or single use batteries to be switched in the field.

Need	Rechargeable	Non-Rechargeable
Cycling	X	
Long Life	X	
Low Cost		X
Low Weight		X
Low Maintenance		X

Table 4-1: Comparison of Rechargeable (Secondary) Batteries and Single-Use (Primary) Batteries¹

Battery compartment size: Once the battery has been selected, dedicate enough space in the system housing for the battery. Do not block or disable battery safety devices, such as safety pressure release vents or battery safety electronics. When possible, keep batteries away from heat concentrations in the housing. Overheating rechargeable batteries could negatively impact their cycle life or cause a thermal runaway condition. When considered late in the design process, sometimes only a custom battery can provide the power needed while still fitting in the available housing space. Custom batteries drive up both the acquisition and lifetime costs of a system. Unless a special application requires a custom battery that a proven electro-chemistry cannot satisfy, avoid cutting edge battery developments because of their lack of standardization and unproven performance.

Finally, when possible, select a standard size commercial battery or a standard military battery in common use. Standard batteries are easy for the operator to obtain and the manufacturers automatically improve their capacities with the latest electro-chemistry and manufacturing technology improvements without additional costs to the system designer.

Electro-Chemistry	Typical Application
Lead acid	Wheel chairs, emergency lighting, UPS, automobiles
Nickel-Cadmium (NiCd)	Two-way radios, biomedical equipment, video cameras, power tools
Nickel-Metal Hydride (NIMH)	Cell phones, laptop computers, electric and hybrid vehicles
Lithium Ion (Li-Ion)	Computers, cell phones
Lithium Ion Polymer (Li-Ion polymer)	Cell phones, computers
Reusable Alkaline	Toys, entertainment devices, flashlights

Table 4-2: Some Typical Applications for Standard Rechargeable Batteries¹

¹ Buchmann, Isidor. *Batteries in a Portable World: A Handbook on Rechargeable Batteries for Non-Engineers*. Cadex Electronics, Inc. May 2001.



Rebecca Morris | Product and Applications Engineer

Manufacturer's Corner: KIC

In today's complex manufacturing environments, a great deal of thought is given to the lean concepts of day-to-day production. Although lean manufacturing techniques are reducing process costs, growing electricity prices are increasing manufacturing costs overall.

Developing the most accurate reflow thermal profiles is a critical component of long term cost savings and production accuracy. Using a thermal profiler is the first step in this process. The thermal profiler measures the time and temperature as the product travels through the reflow oven. The data acquired typically includes statistics such as peak temperature, soak, time above liquidus, and more. This profile is crucial for understanding the "success" of the thermal process relative to the factors that limit the process (i.e., the process window).

Studies have been conducted at numerous electronics manufacturing facilities to observe the effect of power use on varying reflow oven settings. The KIC profilers were key to these investigations. It was theorized that by reducing the heat and increasing the dwell time in each zone of the oven, considerable energy can be saved. This may seem counter-intuitive to the standard profile of using higher reflow temperatures for shorter times; however, the average reflow oven has many alternative recipes that can produce a correct profile. In fact, for any given application, a number of these recipes are capable of processing the product within specification. But the manual setup and investigation of many profiles is very slow and expensive. Software tools are now available to automate process optimization using modern simulation algorithms. Even optimizing



Table 5-1: The KIC Explorer Thermal Profiler

The Explorer is a new generation of thermal profiler from KIC (Figure 5-1). It features a very compact design which will easily move through the restrictive process dimensions encountered in today's thermal applications. It incorporates state-of-the-art surface mount technology (SMT) components and the high-temperature rated components that are necessary to endure the harsh conditions of real-world factory use. KIC's thermal profilers measure all relevant data of the process. By combining this data into a matrix, a process window is defined to assure product reliability. The closer to the center of this window, the more robust the process profile, and the lower the Process Window Index (PWI). This unique and vital statistic measures how well the actual product profile matches the established process window. The PWI not only helps ensure correct wetting and cooling, but will help reduce long-term energy costs.

on low power consumption can now be performed. The KIC tools can consider millions of available recipes and select the appropriate oven setup that yields the lowest energy use, all within seconds.

The profiling expertise of the KIC Explore is a valuable tool, not only to find the perfect thermal recipe, but also as a means to cut wasted energy and production costs.

For more information related to this article, or to schedule a demonstration of the KIC thermal profiler located at the EMPF, contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.



Ken Friedman | EAB Coordinator

Electronics Manufacturing Boot Camp

One of the most comprehensive courses offered at the EMPF Training Center is the Electronics Manufacturing Boot Camp. This two week course is designed to provide information on all aspects of electronics manufacturing for personnel who may not be up to date with the current state of the industry.

Component identification is the first presentation. This lecture provides students with the information necessary to identify and understand the different types of parts used in soldered electronic assemblies. They are also introduced to the considerations necessary when choosing or working with various types of components. Real examples of a variety of components are used during the lecture, and students work with a number of different components during the hands-on portions of the two week course.

The presentation begins by defining nomenclature such as the difference between active components and passive components, the difference between discrete and integrated components, the concept of polarity and the ways polarity can be indicated on parts and printed circuit boards (PCBs), and the concept of lead pitch distances.

Leaded components are introduced by showing the various types of gull-wing and J-leaded components, both integrated and discrete. The various package body types and sizes of small outline integrated circuits (SOICs) and small outline transistors (SOTs) are shown, so the students can understand their differences.

Area array components are presented as the last SMT component type. This discussion covers both ball grid array (BGA) packages (including plastic BGAs and ceramic BGAs), column grid arrays, tape bonded grid arrays, and micro BGAs. Also presented are direct chip attach packages, including flip chip, chip on board, and chip on flex components.

The lecture is completed with presentations on understanding part value markings and packaging types. Both numerical value markings and color band markings are included in the marking discussion. The various types of delivery media (tape and reel, matrix tray, tube) are compared and contrasted.

After attending this lecture, students have a greater familiarity with the variety of parts used in electronics manufacturing. Students also have a greater comfort level with the acronyms used to identify components,

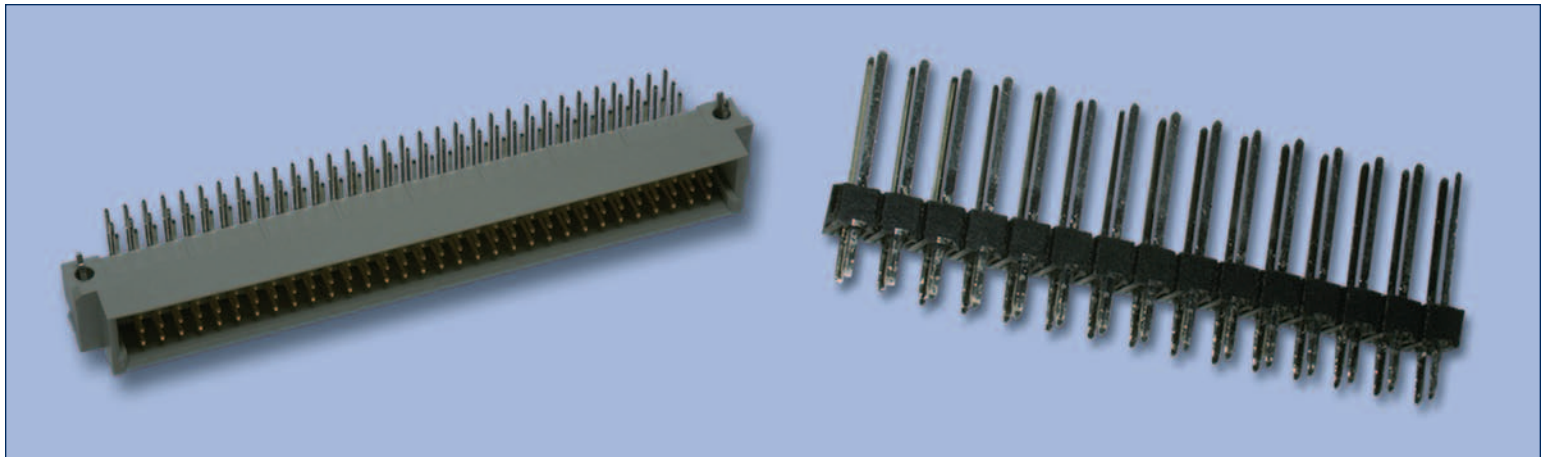


Figure 6-1: Two examples of connectors are shown here. These components are placed on a PWB so that wires, cables and other outside connections can be made to the board via the connector. The pin count and shape of the component varies according to the number of contacts to PWB and style of mating connector.

Next, the students are introduced to through-hole components. Simple axial and radial leaded components are introduced and compared. Single in-line, dual in-line packages, pin grid array, and connectors are also discussed. The advantages and disadvantages of the different types of through-hole components are presented and the preferred types are identified.

Surface mount technology (SMT) parts are also introduced. The three types of interconnects present on SMT parts (terminations, leads, solder bumps) are demonstrated. Rectangular chip components and cylindrical metal electrode face (MELF) components are compared, and the size code system used to describe rectangular chip components is presented. Also included in the discussion of termination type components, are castellated and quad flat no-lead components.

which allows them to become more involved in discussions with manufacturing personnel back at their place of employment.

For additional information on the Boot Camp course, please contact the Registrar at 610.362.1289 or via email at registrar@empf.org. A complete roster and descriptions of all of the courses offered at the EMPF can be found at www.aciusa.org/courses.



Jason Fullerton | Senior Product & Applications Engineer

Advanced Packaging of SMT Assemblies for Greater Cost Reduction

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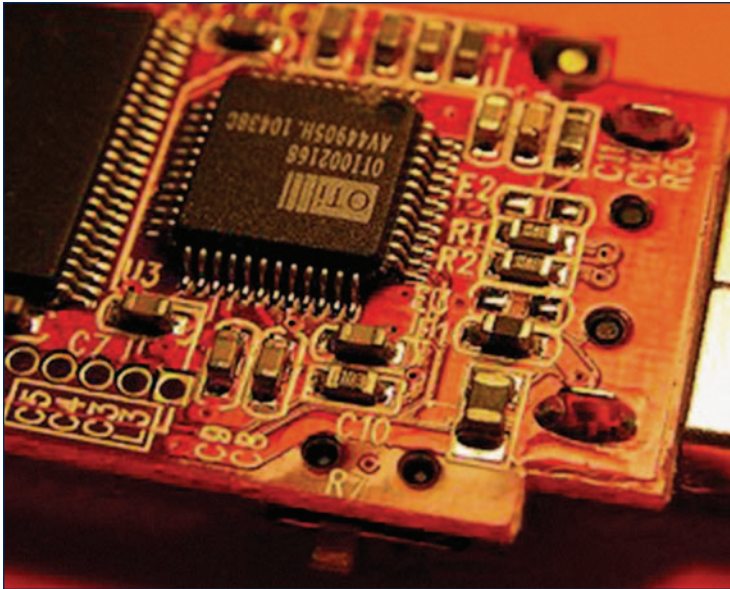


Figure 1-2: SMT Assembly

Surface mounting of components lends itself to a high degree of automation. Traditional leaded component assemblies require a great deal of touch labor. Automation of PCB assemblies limits touch labor to automation set-up. Automation reduces labor costs and greatly increases production rates. These improvements could result in a cost savings of 25 percent or better. For SMT components with very small case sizes, a certain level of manufacturing process development may be necessary to assure parts placement accuracy. Additionally, a top level, functional manufacturing process flow may also need to be established in order to detail the fabrication steps that accommodate a number of SMT package styles.

The leads and cables in leaded component and connectorized package assemblies contribute a certain amount of inductance, potentially degrading the performance of the assembly. Since SMT components are virtually lead-less, the amount of inductance added at the solder joint is considered negligible, and therefore contains far less parasitic losses and

Flip-Chip on Board (FCoB)

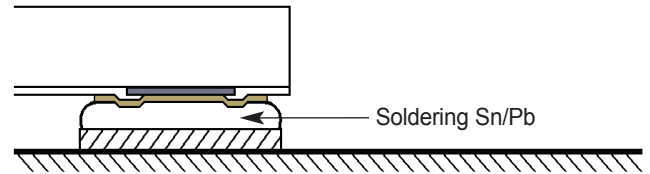


Figure 1-3: Flip-Chip on Board (FCoB) Technology

potentially less consumed power. This would provide savings at the higher system level. The lack of leads or cables in an SMT assembly also provides much better reliability. Since SMT components are attached by a single solder joint, rather than multiple leads or wires, and have much smaller mass than their counterparts, they provide much better shock and vibration resistance. Thus SMT assemblies exhibit higher yields than their leaded assembly counterparts, and are far less likely to require repair in the future. Likewise, greater yields directly contribute to cost savings.

Advanced packaging using SMT can provide even greater cost, weight, and size savings. System-on-Chip (SoC), Flip-Chip-on-Board (FCoB), System-in-Package (SiP), and System-on-Package (SoP) are examples of SMT advanced packaging methods, each designed to help provide such savings. SoC refers to integrating many components of an electronic system into a single integrated circuit or chip. The SoC may contain digital, analog, mixed-signal, and RF functions, all on a single device. Flip-chip technology (Figure 1-3) takes SoC to the next level by eliminating the integrated circuit (IC) package and bonding the bare die directly to the PCB. Flip-chip eliminates the need for wirebonds, further reducing the device's footprint size.

As the complexity of circuit functionality continues to grow, so does the number of elements within the circuit. This presents great challenges in attempting to incorporate the added functionality onto a single SoC.

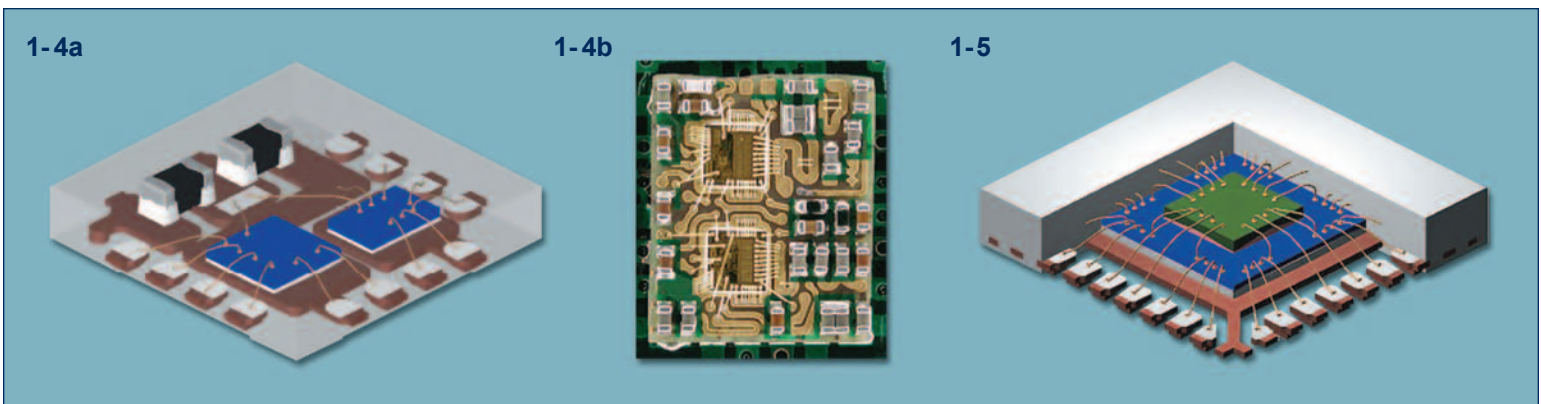


Figure 1-4a, 1-4b and 1-5: System-in-Package (SiP) Technology cross sections and examples.

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Advanced Packaging of SMT Assemblies for Greater Cost Reduction

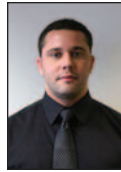
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Implementation of SiP helps surpass certain limitations of SoC capabilities, by allowing for integration of many functions into a single package. SiP (Figure 1-4) integrates one or more SoCs, or other ICs, along with discrete components, using lateral and even vertical integration technologies. The ICs within a SiP can also be stacked, as another means of adding functionality of a circuit, while minimizing the footprint of the package. The stacking of die, or chip stacking (Figure 1-5), deviates from the traditional two-dimensional means of attachment, and involves utilization of the third, or “z” dimension.

SoPs take SiPs a step further, by incorporating multiple dissimilar components and materials, such as silicon, gallium arsenide (GaAs) and silicon germanium (SiGe), as well as passives, into a single package. SoPs can utilize systems-on-chips (SoC) for IC integration, along with

SiP, multi-chip module (MCM) and 3D chip stacking techniques for highly-integrated package integration.

Advanced packaging using SMT provides design flexibility in achieving manufacturing design goals. The EMPF has proven success in design and manufacturing of SMT assemblies. More information can be found by visiting the EMPF website, www.empf.org, or by calling the EMPF technical staff at 610.362.1320.



Nick Fardella | Packaging Engineer

Ask the EMPF Helpline!

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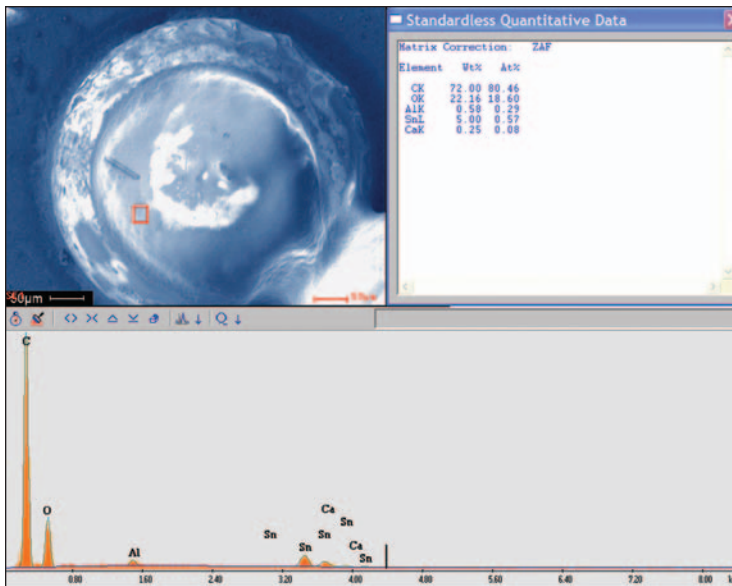


Figure 2-3: Energy Dispersive Spectroscopy analysis of the dark areas of the control component (indicated by the red box) indicating quantities of both carbon and oxygen.

Through analysis involving solderability testing, optical microscopy, SEM/EDS, and FT-IR, it was determined that the BGA components had solderability problems due to contamination. The presence of salts and organic contaminants is a reliability issue which may lead to component failure, performance problems, and an abbreviated life span. Changes in the cleaning process, such as using different cleaning materials or improved rinsing, were recommended.

The EMPF offers a variety of analytical instrumentation and techniques for failure analysis. Ion chromatography, solderability testing, optical microscopy, ROSE testing, FT-IR, and SEM/EDS capabilities are all available to investigate possible contamination issues and determine their root causes. For more information, please contact the EAB Coordinator, Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.



Ron Sauro | Chemist

Fixturing for Selective Soldering

(continued from page 3)

The reasons for requiring a selective solder pallet can be varied. In some instances, a pallet may be required due to SMT components on the secondary side that can not be wave soldered or that are installed using a standard double-side reflow process that would be pushed off by the solder wave (due to the lack of glue). This is especially true for designs that have a high percentage of components in SMT form, with a very small amount of parts that are available only as through-hole. In other designs, a multi-image panel may bow when supported only by the wave solder finger conveyor due to the width of the panel and the mass of the parts. If the individual designs don't allow for the panel to be broken into smaller strips (either due to irregular edge designs or lack of edge clearance for finger conveyors), a pallet can be used for support and/or masking. Finally, the use of masking pallets can allow through-hole components to be installed on both sides of an assembly by using one pallet for each side, and wave soldering the assembly twice.

Processing a masking pallet assembly over a solder wave requires some adjustments to the standard conditions. Most importantly, the pre-heat temperatures will require adjustment as the pallet adds significant thermal mass to the assembly. Care must be taken to ensure that flux is activated

and the assembly does not suffer from thermal shock, just as is true for a standard wave solder application. Wave height settings will require modification, as well. In the case of a standard assembly, the maximum wave height is the height that does not flood the topside of the board. With a pallet, the wave is required to flow into a pocket so it must be set higher. The pallet's extra thickness allows the wave height to be higher without flooding the assembly.

Many options exist for manufacturers that find themselves forced to create designs that violate the old ways of processing assemblies. Selective solder pallets allow a manufacturer to capitalize on existing equipment and process knowledge, while increasing product complexity and capabilities. For more information on selective soldering with pallets, please contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.



Jason Fullerton | Senior Product & Applications Engineer

Upcoming Workshop

Twisted Wire Interconnect

An Alternative to Traditional Multilayer PCB Construction *Presented by Medallion Technologies*

Twisted Wire Interconnects (TWI) are used to replace complex and costly multilayer boards with a series of simple, low cost double-sided boards. The double-sided boards can be populated on **both** sides and then joined with TWIs to form a robust, solderless and compact assembly with free convection channels to assist in thermal management. In addition, the interconnect provides a layout-friendly means of PCB-to-PCB connection, in many cases eliminating the need for routing-restrictive, expensive, high-density connectors.

About Tom Borkes. Tom has over 35 years of technical and managerial assignment experience in electronic product design and assembly. He also teaches within the engineering departments at the City College of New York and Valencia Community College in Florida. A graduate of Hofstra University with a B.S. in Mechanical Engineering, he has worked on technical projects as diverse as the micro-electronic packaging of hybrid circuits and the macro-engineering of a 13 meter diameter parabolic RF antenna.

He is currently working with Medallion Technologies on the next generation in high density, low cost circuit board assembly called "Twisted Wire Interconnects."

DATE: Wednesday, October 21st, 2009

TIME: 10:00 a.m.; complimentary lunch will be served

RSVP: by Monday, October 19th 2009 via phone at 610.362.1200 ext. 609, email at registrar@aciusa.org or online at www.aciusa.org/workshop

Space is limited so please RSVP as soon as possible.

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IPC J-STD-001 CIT Certification

January 5-9
February 9-13
March 9-13
April 13-17
May 18-22
June 22-26
July 6-10
August 10-14
September 14-16
October 12-16
November 2-6
December 14-18

IPC J-STD-001 CIT Recertification

January 14-15
March 25-26
April 29-30
June 17-18
August 26-27
September 23-24
October 28-29

IPC A-610 CIT Certification

February 23-26
March 16-19
June 8-11
July 6-9
August 17-20
October 19-22
December 7-10

IPC A-610 CIT Recertification

January 12-13
March 23-24
April 27-28
June 15-16
July 27-28
August 24-25
September 21-22
October 26-27
November 30 -
December 1

IPC A-600 CIT Certification

January 20-22
April 6-8
July 20-22
August 31 - September 2
November 16-18

IPC 7711/7721 CIT Certification

March 2-6
June 1-5
August 3-7
November 9-13

IPC 7711/7721 CIT Recertification

February 23-24
May 4-5
July 13-14
September 28-29

High Reliability Addendum

IPC J-STD-001 DS CIT Certification

January 16
May 1
August 28
October 30
December 4

Skills

Chip Scale Manufacturing

March 2-4
May 13-15
August 3-5
December 2-4

BGA Manufacturing, Inspection, Rework

January 5-6
April 20-21
July 13-14
September 14-15
December 7-8

Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing

March 9-10
May 11-12
July 27-28
September 16-17
November 30 -
December 1

Design for Manufacture

January 12-13
April 27-28
July 20-21
September 21-22

Failure Analysis and Reliability Testing

February 9-11
April 6-8
June 29 - July 1
August 31 - September 2
November 16-18

