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RF Semiconductor Devices

By maturing and implementing semiconductor device technology, Navy ManTech anticipates a reduction in size, weight and cost of its naval advanced electronic assemblies.

Semiconductors are a unique class of materials because they are, by definition, sometimes insulating and sometimes conducting, and practical conditions exist where the material can act in either manner. A key characteristic of a semiconductor material is its crystal structure which relates to its ability to form bonds with itself and other materials. Another key characteristic is its energy band gap which can be described as the minimum amount of energy required to allow charge transport in a semiconductor. In comparison, materials characterized as metals do not have band gaps because they always transport charge.

Semiconductor materials are highlighted in the portion of the periodic table shown in Figure 1-1. Elements are arranged by both mass and number of electrons in the outermost energy level. In this region a "rule of eight" holds as a common principle dictating the atomic bond nature and bond strength of the element as eight electrons are needed to fill the outermost shell. Semiconductors consist of a crystal lattice of one or more elements and are referred to as binary, ternary, or quaternary compound semiconductors (depending on the number of elements in the basic structure). Silicon has proven to be the ideal elemental semiconductor for electronics since it has four electrons in its outer orbital that form perfect covalent bonds (using all eight electrons) with neighboring Si atoms in a crystal lattice. For radio frequency (RF) applications, the common compound semiconductor materials include GaAs, GaN, SiGe, and InP.

Figure 1-1: Semiconductors highlighted on a portion of the periodic table of elements.[1]

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Ask the EMPF Helpline!

Adaptation of Specifications

A customer called the EMPF Helpline with a question regarding which standards apply to thermo-compression attachment of flip-chip components.

An EMPF customer contacted the Helpline expressing difficulty in locating a specification for reliability testing of flip chip components using thermocompression attachment. The customer was looking to perform thermal reliability and vibration testing on their assemblies, and needed an applicable specification in order to define the test parameters and pass/fail criteria. Although there are specifications available for seemingly every other attachment method, none exists as of yet for such a unique method as thermocompression attachment.

Flip chip bonding is the most desirable direct chip attachment approach for minimizing electronic assembly size as well as improving device performance. A completed flip chip assembly is much smaller than a traditional chip-and-wire based assembly. The chips sit directly on the printed circuit board (PCB) or substrate, reducing the device footprint. The processing of a flip chip component is similar to conventional integrated circuit (IC) fabrication, with a few additional steps. Near the end of the manufacturing process, the attachment pads are metalized to make them more receptive to solder. A small dot, or bump, of gold is then deposited on each metalized die bond pad. Finally, the chips are cut from the wafer as normal, and the die is directly connected to a PCB or substrate. This bumping and attach process is also preferred over the traditional chip-and-wire bond, as its short bond path exhibits much lower inductance, reducing parasitics and allowing higher speed signals.

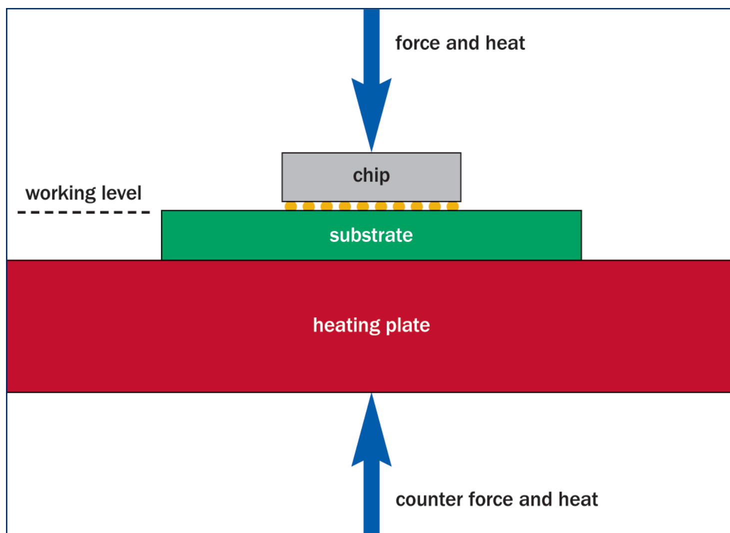


Figure 2-1: Thermo-compression attachment method.

The thermocompression attachment method is a means of attaching a bumped flip chip IC to its PCB or substrate. It is much more robust than attaching the IC bumps to the substrate pads using a conductive epoxy. In thermocompression bonding, temperatures in the range of 300ºC to 400ºC are required to bond the bump to the substrate pad. This heat is applied either by a heated capillary or by mounting the substrate to a heated stage. Figure 2-1 graphically represents this process. Heat, time, and pressure (force) are the major determining factors in the formation of a thermocompression bond. A robust thermocompression bond typically results in a flattened ball appearance.

Reliability testing determines whether an attachment technology meets specified performance requirements by testing to more severe conditions than those that would be used for normal screening of an assembly. In this instance, the customer was interested in performing thermal reliability testing on their flip chip assemblies. Thermal reliability testing involves rapidly cycling between temperatures that are far above and below what the assembly would actually see in the field. This accelerated exposure can provide the equivalent of several years of assembly operation in the field in only a few days inside a thermal chamber.

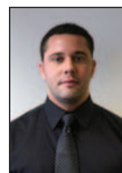
Currently there is no standard available for flip chip thermocompression attachment reliability. Of the many standards available for reference, the JESD22-A104-D and IPC-9701 standards were written for reliability of solder joints of surface mount components and appear to be the most applicable for thermocompression attachment. By referencing these two standards, and also taking into account limitations of the thermal chambers available to the customer, the following criteria were recommended for evaluating the thermal reliability of the customer's flip chip thermocompression attached assemblies.

Based on JESD22-A104 (test condition G) and IPC-9701 (test condition TC3) the following criteria were applied:

- Maximum temperature: +125ºC +15/-0ºC
- Minimum temperature: -40ºC +0/-10ºC
- Preferred soak (dwell) time: 10 minutes
- Ramp rate: less than 15ºC/minute
- Test duration: 1,000 cycles or 50% cumulative failures, whichever occurs first
- Testing to 63% cumulative failures is preferred to characterize the failure distribution.

The customer performed thermal cycling to the above conditions and felt confident in the reliability results obtained.

For more information on JESD or IPC training or certification, please contact the registrar at 610.362.1295, via email at registrar@empf.org, or find course descriptions on the web at www.aciusa.org/courses. For any other information regarding flip chip attach or thermocompression bonding, please contact the EMPF Helpline at 610.362.1320.



Nick Fardella | Packaging Engineer

aci

NAVY MANTECH

The EMPF Power Packaging Laboratory

Microelectronics is the manufacture of systems built from extremely small electronic components. In today's electronic world, devices must be portable, equipped with wireless technology and are driven by size, weight, power, and cost (SWaP-C). These system level drivers are crucial to all current and future electronic applications from personal computers and cellular telephones to military-fielded hardware, biomedical instrumentation, and space-flight hardware.

The EMPF will continue to broaden its capabilities to meet, and exceed the expectations of our customer base. The power packaging laboratory is one example of this, with its ability to handle the latest materials and assembly techniques used in microelectronics packages. The combination of best in class packaging equipment, thermal simulation, thermal measurement capability, and device level diagnostics are the foundations upon which future systems for power, RF, and advanced packaging technology will quickly advance. Designers can rapidly assess and mitigate the risks inherent in their designs of new electronic packages while engineers can take advantage of the full potential of the emerging advanced power electronics technologies.

Figure 3-1: POP components.

Reduced product size and weight can be realized through a decrease in the number of individual components and internal interconnects. Multilayer printed circuit boards (PCBs) with plated micro vias and embedded passives are designed to reduce the number of components. In addition to reducing size and weight, product reliability will increase due to fewer components while costs are reduced.

Innovative circuit packaging is a key technology in reducing size and space requirements. Chip scale package (CSP), package on package (POP), and fine pitch ball grid array (FBGA) all have supported high-density wiring technology and are widely used in the market. Miniaturization forced the use of new approaches in die packaging in order to achieve the smallest possible solutions.

With the reduction in chip size and increase in functionality, chips are now being converted from a wire bondable configuration to a flip chip application. The stacking of chips has been very common in the computer industry as well as in hand held devices. Stacking flash memory and static random access memory (SRAM) over an application specific integrated circuit (ASIC), with or without the use of an interposer, is widely used to reduce the size, weight and cost.

The power packaging lab has the capability for stacking package on package as well as die stacking. Using a die bonder, die can be placed at an accuracy of ±12.5 microns with a precision of three sigma. Stacking of die can be accomplished with FBGA reflowed using solder or by having metal to metal contact between the BGA and pads using epoxies. Using the 14 x 14 FBGA components in Figure 3-1, a POP was successfully assembled as shown schematically in Figure 3-2.

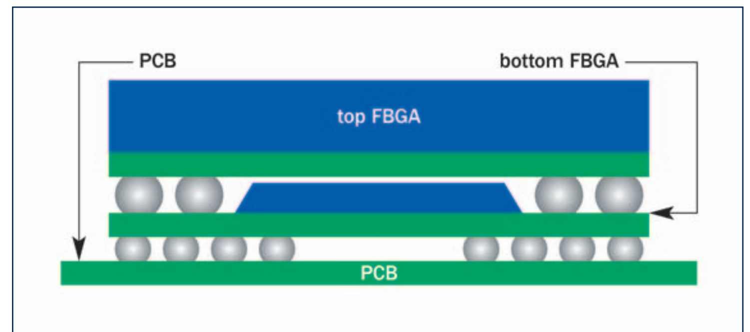


Figure 3-2: Schematic of POP assembly using FBGA.

For more information regarding the power packaging lab capabilities, please contact the EMPF Helpline at 610.362.1320 or visit the EMPF website at www.empf.org.

Anand Bhavankar | Senior R&D Engineer

Tech Tips: Sensor Drop Testing for Gun Launch

Shock is defined as a sudden change that affects the location, velocity, acceleration, or forces in a structure. A blast or shock wave due to a near-miss explosion can obviously cause sudden deflection and high strain rates in electronic components and wiring boards, but it is by no means the only type of shock loading which engineers must concern themselves with. Shock and high g loading may occur during assembly, transport, or handling of electronic packages. In some cases, the transport environment is much more severe than the actual use environment.

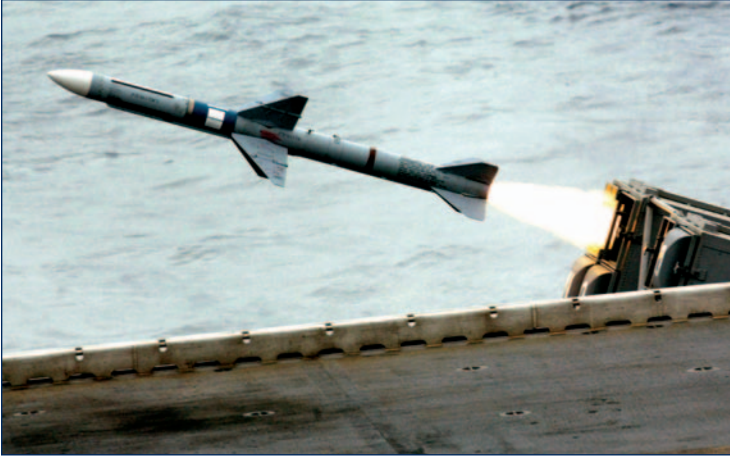


Figure 4-1: A drop shock tester can be used as a pre-screening method for projectile designs to help ensure reliability during launch.

A free-fall drop is often used to simulate the shock environment in transport, but can also be used as a pre-screen test for actual gun launch applications (Figure 4-1) where sensors or microelectro mechanical (MEM) devices need to withstand forces exceeding 20,000 g. However, the use of conventional shock test equipment will not simulate the environmental conditions associated with gun launched projectiles. Compared to gun shock pulses, the drop shock test has a much shorter shock duration. The effective transient duration times between air gun and drop tester is illustrated in the shock response spectra in Figure 4-2. The shock response spectrum (SRS) shows that the drop test achieved a maximum force of 21,086 g for 0.09 milliseconds. In contrast, the inset chart indicates that the gun launch shock is maintained over a much longer duration (by a factor of ten). However, the use of the drop tester as a pre-screen for gun launch projectiles utilizing sensors and MEM devices is not without merit.

A recent project at the EMPF involved testing the reliability of a sensor to be utilized in a projectile application that required survivability after a 20,000 g force. To pass the rigors of high acceleration, the proper combination of sensor redesign and the addition of shock absorbing materials had to be used to redistribute the forces away from the sensitive solder connections which were prone to cracking upon gun launch. A pre-screening of the various sensor designs and material sets was initiated using the drop tester as a low cost indicator of which sensor and material combinations could be excluded from the more expensive gun launch testing (which can exceed $2,000 per shot). The utilization of the shock

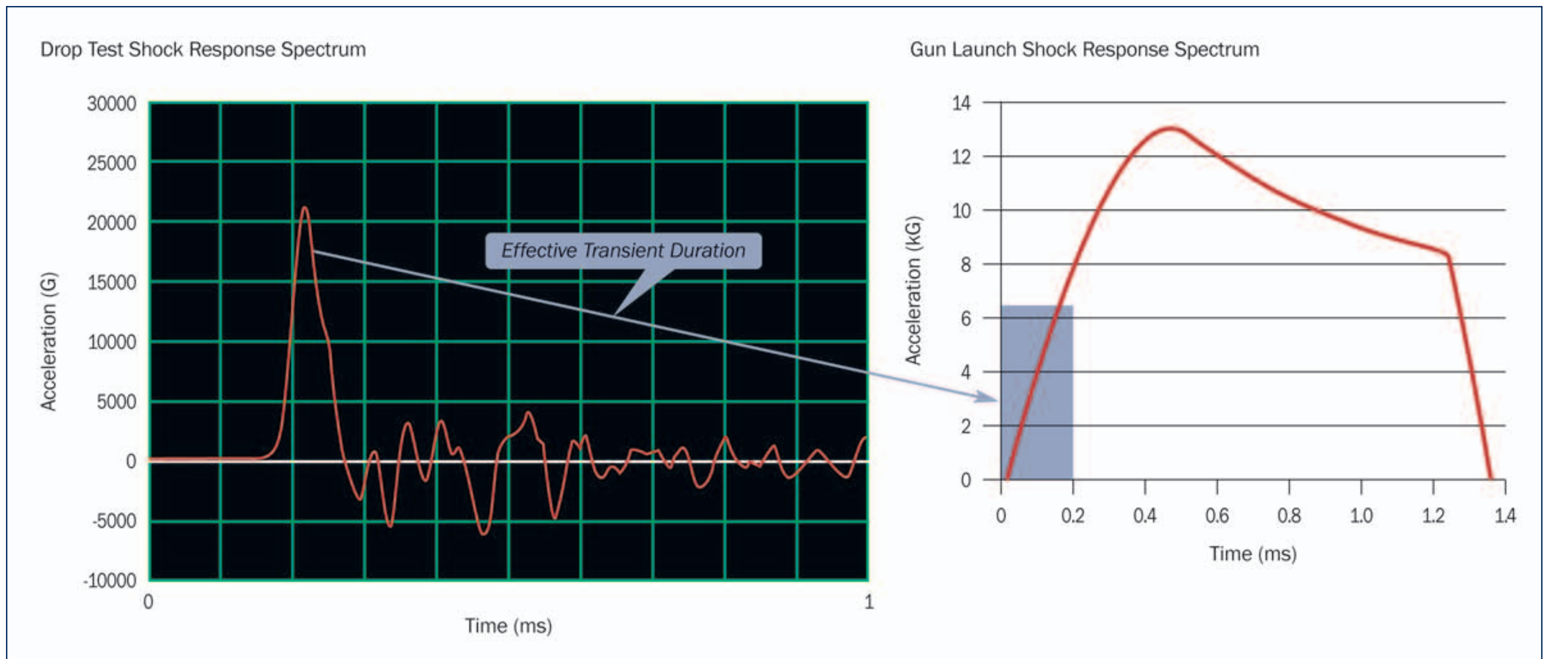


Figure 4-2: Shock response spectra comparisons - drop tester versus gun launch.

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Manufacturer's Corner: Dage

A Dage digital X-ray system (Figure 5-1) can provide high quality inspection capability when no other method is practical or able to provide the necessary direct observation. When the critical points of inspection are the central balls of a ball grid array (BGA), the integrity of a solder joint, or a trace deep in a circuit board, modern high magnification and real-time X-ray inspection is often the only reliable method available to assure a clear assessment of the issue (Figure 5-2).

An understanding of several key X-ray characteristics is needed before interpreting the images. These characteristics are feature recognition, live image capability, resolution, tube power, and penetrating power.

Feature recognition is a human skill, but the images presented to the operator are the accumulation of all the technical capabilities of an X-ray machine. It is essential that the specific image is clear and unambiguous. The X-ray image is presented on the monitor with a full 16 bits of grayscale resolution. The value of this subtle shading is clear. For example, a solder joint failure may manifest itself as a thin line on the X-ray image. Recognizing that the fine line on a solder joint is a fracture is an operator skill, but the ability to see the fine line is due to the 100 nanometer feature recognition capability of the equipment and the grayscale resolution on the monitor.

Live image capability is the ability to see real-time X-ray images. As the X-ray camera moves along the object being examined, the image captured is presented at 30 frames per second (fps) to the machine operator. This is a very useful feature when the specific position of the problem has not been identified and the suspect area must be searched.

The high performance of the Dage machine is achieved with an innovatively designed sealed transmissive X-ray tube. This technology can provide up to 10 watts of power, adjustable in precise increments, to retain the sub-micron feature recognition that is critical for resolving small features and defects. The high power also provides greater visual penetration necessary for dense materials like a multilayer circuit board or the packaging material of a BGA.

5-1

5-2

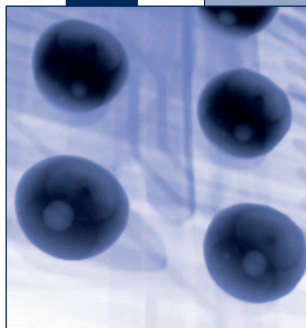

Figure 5-1: The Dage XD7600NT digital X-ray inspection system.

Figure 5-2: BGA X-ray image clearly shows voiding within the solder balls.

Well designed and intuitive software control allows the operator to achieve the correct blend of X-ray penetrating power with the highest possible resolution. The intuitive nature of the software lowers the operator learning time and the chances of errors. As a typical example, the height of an object being inspected can be programmed into the machine and a "no fly zone" created. This will prohibit the X-ray head from colliding with the sample.

Circuit boards are usually flat and can be easily inspected in a parallel fashion above the surface of the board. But when the top view is not enough, the Dage inspection system is capable of providing up to 70 degrees of oblique views or 140 degrees of total view with no loss of resolution. These oblique or side angle inspections are preferred when examining under a component.

To summarize, the Dage X-ray system can provide the high quality images necessary for manufacturing process inspection. The performance of entire systems can depend on the integrity of a solder joint, the position of a BGA, or the trace inside a circuit board. All these issues and more can be resolved by inspection with a Dage X-ray machine. For more information or a demonstration of this machine, please contact Mike Prestoy at mprestoy@aciusa.org.

Mike Prestoy | Senior Applications Engineer

BGA Application Training

Ball grid array (BGA) packaged components have many design advantages when compared to equivalent components with external leads, such as higher I/O density, lesser termination inductance, and the ability to design reliefs into the substrate to improve thermal performance. While these advantages are significant for design activities, there are some unique challenges encountered when assembling and soldering BGA packages to printed circuit boards (PCBs). The EMPF offers a course on BGA Manufacturing, Inspection, and Rework that addresses the challenges that exist in the BGA assembly process.

The course begins with information on the various types of BGA packages and their advantages and disadvantages. The most common type is the plastic BGA (PBGA), which is constructed by molding over a substrate with a die attached and wirebonded (Figures 6-1 and 6-2). The substrate is typically a glass epoxy material and may be exposed or completely contained within the plastic molded body of the PBGA. These parts are typically lower in cost than other package types. Since the coefficient of thermal expansion (CTE) is similar to PCB materials, lower stresses occur between the BGA and the PCB during temperature changes. PBGAs can be sensitive to moisture exposure and package fracturing during reflow if not stored and handled properly.

Ceramic BGAs (CBGAs), an alternative to PBGAs, can be hermetically sealed and thus are not sensitive to moisture. Since the CTE of a CBGA is significantly lower than epoxy glass PCB base materials, stresses on the soldered connection can result during temperature changes. A CBGA also has a significantly higher thermal mass than an equivalent PBGA which makes reflow oven profiles more difficult to develop.

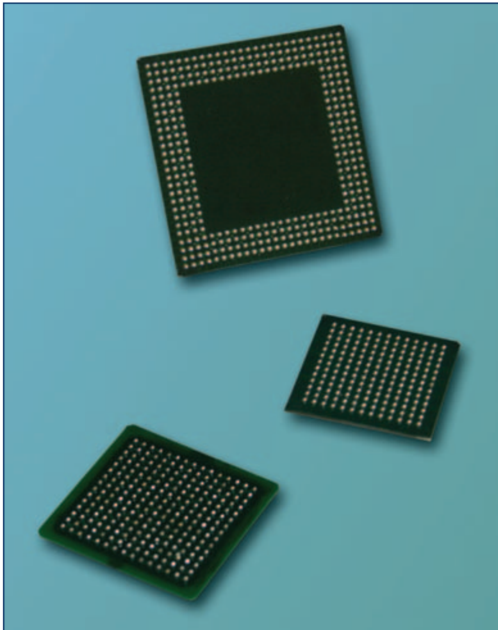

Figure 6-1: Plastic BGAs.

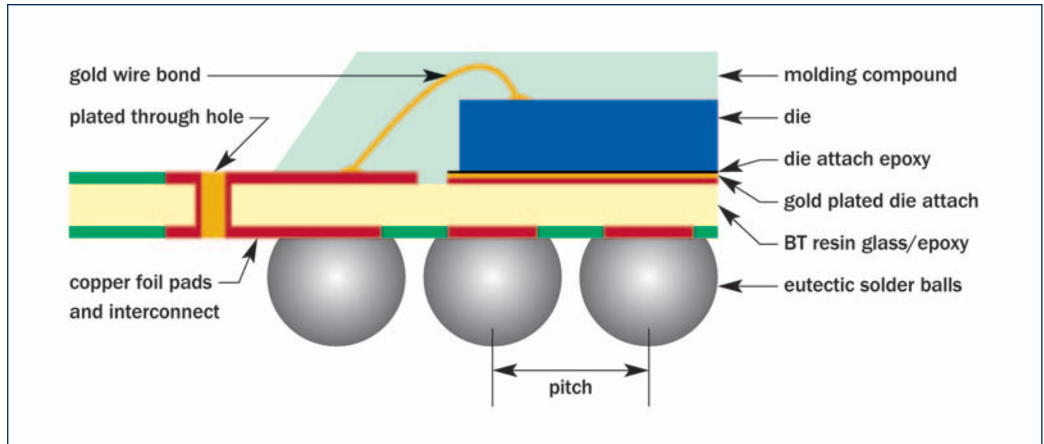

Figure 6-2: Plastic BGA construction.

Assembly concerns are the next topic presented during the course. This section exposes the student to some of the difficulties that can be present during BGA assembly processes. Storage and handling of BGAs, PCBs, and the solder paste used to install them is discussed with a focus on humidity exposure and defects that can occur as a result of improper storage. The use of solder mask defined (SMD) lands and the advantages of non-solder mask defined (NSMD) lands in the design of the PCB is discussed. The effects of CTE mismatch on reliability are also presented.

The manufacturing process to install and solder BGAs is discussed. Control of the solder paste application process is stressed as a means to ensure a quality solder joint. The effects of improper paste volume and alignment of the stencil to the PCB are demonstrated and actions that can be taken to prevent or eliminate these issues are discussed. Strategies for alignment of BGAs to the PCB, such as mechanical alignment fixtures and vision alignment systems, are compared and contrasted. The self-centering effect of BGAs during solder reflow is demonstrated via a short movie during the lecture presentation.

Rework of BGA components through the use of hot air and infrared radiation equipment is discussed. A focus on obtaining the correct reflow temperatures is stressed. Reballing techniques, such as the use of paper preforms or loose balls and fixtures, are presented with a focus on the advantages and disadvantages of each method. The proper way to prepare a PCB site during BGA removal and replacement is presented (Figure 6-3) with a focus on preventing damage to the PCB surface.

The various methods of inspection of soldered BGAs are the final topic of focus during the course. The use of endoscopic camera systems is presented. The capabilities and limitations of inspection endoscopes are highlighted through the use of images taken using such a system. The use of X-ray to inspect the workmanship of a soldered BGA is presented, highlighting the advantages and limitations of the various types of X-ray systems.

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RF Semiconductor Devices

(continued from page 1)

The electric potential bandgap of a semiconductor adjusts with the potential of the adjoining material at the semiconductor junction. This interaction is the basis of "bandgap engineering" which is the common term for semiconductor device engineering. As device fabrication quality has improved, this physical junction phenomenon has been used to foster real advantages in device applications based on joined combinations of various semiconductors, metals, and insulating materials.

Bandgap engineering is employed in the development of all semiconductor transistor devices including the well established field effect transistor (FET) and bipolar junction transistor (BJT). These use a semiconductor interface as a controlled "gate" to regulate the path of electrical charge transport. FETs use a voltage controlled gate while BJTs use a current controlled gate. A popular related device to the FET is the metal oxide semiconductor FET, or MOSFET. The MOSFET (Figure 1-2) is similar in design to the FET, but improves output performance with a metal-oxide insulating film that alters the interface at which the charge current travels. The ability of silicon to oxidize and form a stable oxide layer makes this device very popular for Si-based devices.

High electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) are particularly well suited for the amplification of large microwave signals with better efficiency for low noise applications. They have been used most often in the recent development of monolithic microwave integrated circuits (MMICs) for microwave and millimeter-wave transistors. These devices use heterojunctions of different semiconductor materials for their operation unlike conventional transistors which use junctions of the same material with different dopants (added impurities).

HEMT devices (Figure 1-3) are unique for their enhanced carrier mobility induced by the formation of a two-dimensional region of trapped charges at the junction interface. While the more delicate device geometry results in higher cost devices, the electrical property improvements have been of increasing interest for high performance device applications. With recent improvements in epitaxial fabrication methods, these devices have become an increasingly popular alternative for high performance devices.

Modern RF systems for military applications commonly use semiconductor devices to support communications, surveillance, and electronic warfare functions. These devices include amplifiers, mixers, multipliers, dividers, phase-shifters, devices for frequency generation, and highly integrated multifunction parts. While the design of these devices may be similar in theory as silicon based devices for electronics applications, critical RF factors such as the operation frequency, bandwidth, and noise isolation tend to favor devices made with compound semiconductor materials for higher frequencies. A common rule of thumb depicted in Figure 1-4 is that silicon based devices are well suited for common RF applications up to the 1-2 GHz range, while at higher frequencies the bandgap advantages of compound semiconductor devices become worth the cost increase related to fabrication.

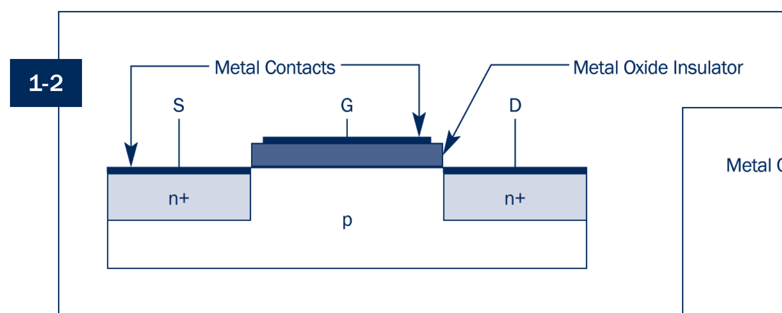

Figure 1-2: MOSFET general device geometry.[1]

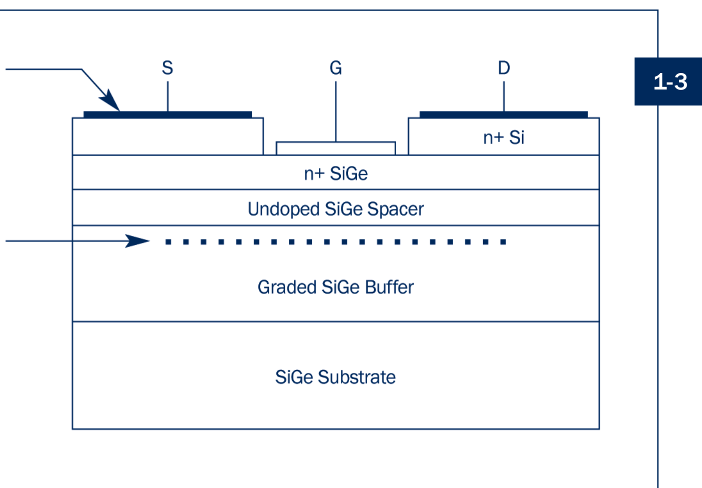

Figure 1-3: HEMT general device geometry.[1]

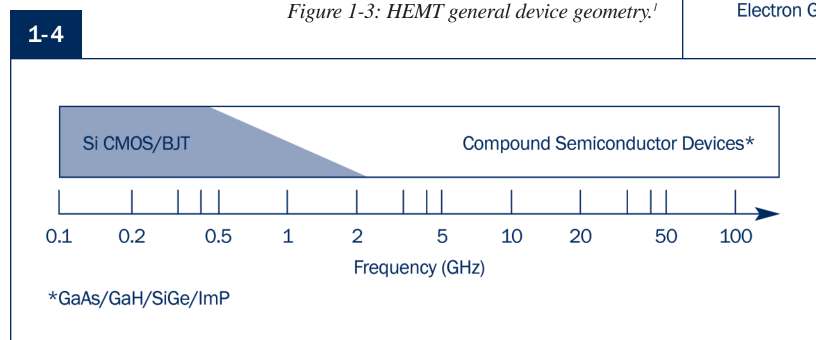

Figure 1-4: Device technology versus application frequency.[2]

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RF Semiconductor Devices

(continued from page 7)

ManTech programs, by definition, support the technology transfer and deployment activities which integrate the present state of the art technology with modern warship and warfighter development. Many current programs involve the integration of high power and high frequency compound semiconductor based devices to increase the range and efficiency of existing RF systems. The R&D engineering team at the EMPF is comprised of experienced professionals with backgrounds in all aspects of semiconductor and RF technology. This experience is leveraged to evaluate new technology effectiveness, efficiency, reliability, and cost concerns with the overall goal of maintaining the U.S. Navy's superior status on the global stage.

References

[1] Losee, Ferril A. *RF Systems, Components, and Circuits Handbook*. Boston: Artech House, 2005. Print.

[2] Maiti, C. K., and G. A. Armstrong. *Applications of Silicon-germanium Heterostructure Devices*. Bristol [u.a.: Institute of Physics Publ., 2001. Print.

Dan Perez | R&D Engineer

Tech Tips: Sensor Drop Testing for Gun Launch

(continued from page 4)

tester can provide an economical method of eliminating sure failures and narrowing the viable test candidates.

The EMPF uses a Model 23 Lansmont Shock Test System with a dual mass shock amplifier and high g shock accelerometer (Figure 4-3). The accelerometer is located on the fixture that holds the test boards. An electric hoist raises the shock table until it reaches the programmed drop height; in this case 70 inches, which was easily preset by the operator using the Touch Test Shock II Controls. A seismic base provides a precision impact surface and also isolates high shock loads from the floor and surrounding areas. The shock table drops from the set drop height and impacts the base programmer, generating the desired shock pulse. The resulting SRS is recorded by a data acquisition system for each drop.

Figure 4-3: EMPF high g shock tester.

The use of a carefully planned test allowed the EMPF to quickly and cost effectively screen a variety of sensors and packaging. Combined with the expertise in electronics, materials, and sensor design, survivable circuitry can be developed to sustain high g forces. The nature of the electronic manufacturing and research done at the EMPF has necessitated our expertise in the material requirements and design of sensors, MEMs, and other devices which demand performance at high g forces. For more information on shock or vibration testing of sensors and other electronic devices, please contact the EMPF Helpline at 610.362.1320, via email at helpline@empf.org or visit the website at www.empf.org.

Carmine Meola | R&D Projects Lead

BGA Application Training

(continued from page 6)

The students are also given the opportunity to reinforce the lecture materials through the use of the EMPF Demonstration Factory. Students are given the opportunity to assemble BGAs to PCBs using an automated solder screen printer, SMT placement equipment, and reflow oven. These assemblies are then inspected using both the endoscope and transmissive X-ray systems in the Demonstration Factory. Students remove and replace a BGA on their PCB using hot air rework systems. The students can then inspect the replaced components to demonstrate the differences in quality between a BGA assembled using a fully automated process and one using a rework process. The instructor also demonstrates a variety of defects that can be identified during inspection and measures that can be taken to prevent those defects from occurring in the first place.

For more information about the BGA Manufacturing, Inspection, and Rework course — or to develop a customized BGA course that can provide training at your facility, on your equipment — contact the EMPF Registrar by calling 610.362.1295 or via email at registrar@empf.org. Information and schedules can also be obtained at the EMPF website: www.empf.org.

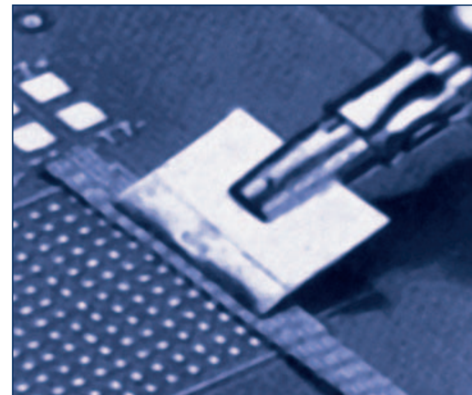

Figure 6-3: BGA site preparation.

Jason Fullerton | Sr. Product and Applications Engineer

IPC Revision E Training Available Now!

The new Revision E for both **IPC J-STD-001** and **IPC A-610** covers five years of critical upgrades, changes and clarifications. Both revisions were released in April 2010 and are covered in the training at ACI Technologies.

With the last update of the **J-STD-001** performed in February 2005, there are five years of significant changes to the standard.

Some of these changes are:

- Clarification on acceptable damage for stranded wire
- Requirements for heat shrinkable soldering devices
- Specifications for BGA underfill requirements
- Expanded treatment of rework acceptability

The **IPC A-610** is the most referenced electronic build standard in the world. Like the J-STD-001, it has been revised to incorporate the critical requirements for the assembly of quality circuit boards. Revision E has 165 new or updated illustrations, bringing the total illustrations to more than 800.

Some of the critical additions are:

- Expanded coverage for hot tear and lead free fillet lifting
- New trends and requirements in array technologies
- Enhanced package on package criteria

IPC J-STD-001

CIT Recertification: October 5-6
DS CIT Certification: October 8
CIT Certification: October 18-22

This course provides an in-depth study and hands-on application of the national standard for soldering as well as all materials necessary to conduct operator training.

IPC A-610

CIT Certification: October 11-14
CIT Recertification: October 4-5

Achieve the highest quality and most cost-effective productivity by knowing how to correctly apply the IPC A-610 acceptability criteria.

Contact the Registrar for scheduling by phone at **610.362.1295**, via email at **registrar@empf.org** or visit us online at **www.aciusa.org/courses**.

ACI Technologies, Inc.

2010 Class Schedule

National Electronics Manufacturing Technology Center of Excellence

Electronics Manufacturing

Boot Camp A
March 1-5
May 3-7
September 13-17
November 1-5

Boot Camp B
March 8-12
May 10-14
September 20-24
November 8-12

CIS/Operator

IPC J-STD-001
Call for Availability

IPC A-610
Call for Availability

IPC 7711/7721
Call for Availability

IPC/WHMA-A-620A
CIS Certification
February 16-18
April 19-21
June 28-30
September 27-29
December 20-22

High Reliability Addendum

IPC J-STD-001 DS
CIT Certification
January 15
February 26
April 16
May 28
August 27
October 8

IPC CIT Challenge Test

January 29
February 19
April 23
June 18
July 16
August 20
October 15
November 19
December 17
Call for Additional Availabilities

IPC Certifications CIT/Instructor

IPC J-STD-001
CIT Certification
January 4-8
February 1-5
March 15-19
April 26-30
June 7-11
July 19-23
August 30 - September 3
October 18-22
December 6-10

IPC J-STD-001
CIT Recertification
January 13-14
February 24-25
April 14-15
May 26-27
July 14-15
August 25-26
October 6-7
November 17-18
December 15-16

IPC A-610
CIT Certification
January 4-7
February 8-11
April 19-22
June 14-17
August 16-19
October 11-14
December 6-9

IPC A-610
CIT Recertification
January 11-12
February 22-23
April 12-13
May 24-25
July 12-13
August 23-24
October 4-5
November 15-16
December 13-14

IPC A-600
CIT Certification
January 26-28
March 22-24
June 21-23
September 7-9
November 29 - December 1

IPC 7711/7721
CIT Certification
January 25-29
March 22-26
July 26-30
October 25-29

IPC 7711/7721
CIT Recertification
March 8-9
May 17-18
June 14-15
September 13-14

Skills

BGA Manufacturing, Inspection, Rework
January 19-20
April 5-6
June 28-29
October 11-12

Chip Scale Manufacturing
February 16-18
May 26-28
August 11-13
December 13-15

Continuing Professional Advancement in Electronics Manufacturing

Design for Manufacturability
February 8-9
May 24-25
August 9-10
November 22-23

Failure Analysis and Reliability Testing
March 15-17
May 17-19
September 27-29
November 15-17

Lead Free Manufacturing
February 22-23
June 7-8
October 4-5
December 20-21

Contact the Registrar for course information and pricing: *phone:* 610.362.1295 *email:* registrar@empf.org

Electronics manufacturing assistance is available via the EMPF Helpline: *phone:* 610.362.1320 *email:* helpline@empf.org

Custom courses and on-site training are available. ACI is conveniently located next to the Philadelphia International Airport.

All courses and dates subject to change without notice.

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