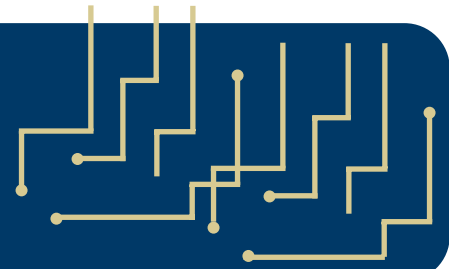


empfasis



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American Competitiveness Institute
One International Plaza
Suite 600

Philadelphia, PA 19113

(610) 362-1200 • FAX: (610) 362-1290

HELPLINE: (610) 362-1320

WEBSITE: www.empf.org

The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

EMPF Director

Michael D. Frederickson
mfrederickson@aciusa.org

EMPF Technical Director

Jerry McGowan
jmcgowan@aciusa.org

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Office of Naval Research
Director of Manufacturing Technology

Steve Linder

linderst@onr.navy.mil
(703) 696-8482

ONR Program Officer

John Olewnik
olewnij@onr.navy.mil
(215) 697-9526

Moisture Sensitive Devices (QFPs and BGAs)

The first surface mount devices available to electronic assemblers were ceramic packages. These packages were near hermetic and were not sensitive to moisture. The drive towards smaller and cheaper electronics has led to plastic-body packages, such as quad flat packs (QFPs) and ball grid arrays (BGAs). These packages are all sensitive to moisture to some degree. In fact, early plastic packages had poor resistance to moisture ingress. Recently, component manufacturers and material suppliers have improved the plastics and molding processes to increase the moisture resistance of the packages.

Moisture can infiltrate these packages and facilitate failures two different ways. First, moisture can collect at the interfaces within a package, then upon reflow, expand rapidly and explosively creating delaminations, possibly severing wire bonds or tab bonds.

ionic contaminants have minimized observations of these types of failures.

Standards have been developed to aid the manufacturer in determining sensitivity to moisture and setting guidelines on how to handle such packages, J-STD-033. This document is a joint publication of the IPC and the Joint Electronic Device Engineering Council (JEDEC)¹. This document was published in 1999 replacing the prior standards IPC-SM-786 and JEDEC-JESD22-A112. This document supplies information on how to pack, store, bake, etc. moisture sensitive devices. One of the most often used tables links the JEDEC moisture resistance level to floor life (see Table 1). Other information in the document relates how these exposure times may differ when the ambient conditions are different. Also, the recommended baking time based on the exposure conditions are also listed.

Level	Floor Life (out of bag) at < 30°C/60% RH
1	Unlimited at < 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.

Table 1. Moisture Classification Level and Floor Life¹

The second common failure mode associated with moisture in packages is corrosion of internal metallic structures (e.g. wire bonds). New plastics that have less mobile and low overall

Following these guidelines blindly can also impact your process. For example, in a high mix manufacturing environment a tray of BGA components (Level 5a) that may be used

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Metallographic Analysis of Solder Joints

With smaller packages, increased board density, and the introduction of lead-free solder alloys, metallographic analysis of solder joints has become increasingly useful in assessing both surface mount and through hole solder joints. Metallographic analysis includes inspection of the solder joints using any of a number of different analytical methods. The most useful of metallographic analysis methods is a cross-section. Cross-sections, or microsections as they are often termed, can reveal much more information about the quality and composition of a solder joint than surface analysis alone. Areas of investigation for metallographic analysis of cross-sections in electronics include:

- Cracks
- Voids
- Microstructure
- Plating Dimensions
- Plating Defects
- Solder Wetting
- Corrosion
- Elemental Composition
- Fatigue
- Solder
- Geometry

Sample Preparation

Sample preparation for metallographic analysis must be performed with extreme care. Many of the methods used to expose areas of interest may also produce deformation that could be misinterpreted or damage a sample. Sample preparation for cross-sections typically includes documentation, sectioning, grinding, polishing and etching.

Prior to sectioning the electronic assembly or circuit board, the area of interest should be marked and recorded. It is also helpful to draw a sketch, take a photograph, or use the original board drawings to number the area being sectioned. These numbers can be transferred to mold mounting cups and eventually to the metallographic mount itself for easy identification throughout the sectioning and examination process. If available, X-ray inspection of the sample area should be performed. The information obtained by X-ray inspection will help localize the area of interest while exposing possible problem areas. Once the area is well

documented, a sectioning route should be established and the board can be sectioned. Often it is the sectioning route that determines what type of initial cut can be performed. A band saw or router can be used on bare boards and sparsely populated boards where there is space to cut between components. Densely populated areas need to be cut by a precision table saw, preferably with a wafering blade. Following sectioning of the sample, specimens should be cleaned thoroughly to remove contamination and debris from all surfaces.

Sectioned samples can be cold mounted in an acrylic, polyester, or two-part epoxy. Edge retention, shrinkage, time of cure, and heat of cure varies with the type of mounting media used and should be noted when mounting media is selected. Difficulty in removing samples from the

mount can be overcome by applying the mold release to the sample cup prior to applying the mount material. Any air bubbles trapped in a two-part epoxy resin can be removed prior to cure by using a vacuum to impregnate the sample.

A number of successive grinding and polishing steps are performed on the cured mounts in order to expose the area of interest. These grinding and polishing steps are typically classified into one of three categories: planar grinding, the specimen integrity, and the final polishing. Planar grinding involves the use of coarse grit silicon carbide paper. The specimen integrity stage removes the deformation caused by the planar grinding stage. Both silicon carbide paper and napless polishing cloths are used in this stage. The high-nap cloth and alumina slurry used during the final polishing stage removes any scratches remaining from the specimen integrity stage.

Revealing many of the features of a solder joint often requires the solder joint to be etched. Prior to etching the joint, the samples should be examined in its pre-etched form. This helps distinguish separations and cracks prior to the etching process. After etching, cracks and separations may become large or difficult to distinguish from the other etched areas. Chemical etching is the preferred method for most electronic analysis laboratories. The etchant used will depend entirely upon the composition of the sample and the feature of most interest. There are a number of chemicals that can be used to reveal microstructure of a solder joint. Hydrogen peroxide-ammonium hydroxide solution works well for tin-lead samples, but investigators should consult a good metallographic reference if examination of other alloys is required.

Examination Techniques

The most popular techniques of examining cross-sections are optical and scanning electron microscopy (SEM). Optical microscopy can be used to examine features that are visible under low to medium magnification. These features include cracks, voids, solder geometry, and wetting. There are a number of optical microscopy examination modes from which a sample can be examined such as bright-field, dark-field, oblique, phase contrast, interference contrast, and polarized light illumination. A polarized light metallograph is extremely efficient at producing contrast between the different phases, layers, and materials present in a surface mount solder joint. These polarized metallographs have a normal or inverted sample stage and provide information that cannot readily be resolved using some of the other illumination techniques. The performance and usefulness of an optical investigation can be enhanced when the microscope is coupled with a camera and digital imaging system that allows for manipulation and measurement of digital images. Measurement of solder fillet geometry, as well as layer dimensions can be used as process and reliability indicators.

Scanning electron microscopy is used to examine features that require high magnification or good depth of field.

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Figure 1. SEM backscatter image of solder microstructure after mild heat treatment.

Metallographic Analysis of Solder Joints

(continued from p. 2)

Microstructure, plating, intermetallic growth, microcrack formation and separations are a few of the more common anomalies investigated using electron microscopy. When used in the elemental contrast producing backscatter electron mode, phase differences in tin-lead microstructure can be viewed quite easily. Most scanning electron microscopes require a thin conductive coating, such as gold or platinum, to be applied to resist the build up of electrons on the sample surface. This coating is usually thick enough to provide a conductive path but thin enough not to mask the features of the surface. Elemental dispersive spectroscopy (EDS) is often used in conjunction with SEM to identify the elements present in a sample. EDS uses characteristic X-rays to identify, image, and quantify elements and compounds with atomic numbers higher than seven.

Metallographic Evaluation

Properly prepared cross-sections of solder joints and their surrounding materials can provide a wealth of information about process and service conditions as well as the reliability of the solder joint. Key areas of investigation in a tin-lead joint are the dimensions of the interfacial intermetallic regions and the size and location of tin-rich and lead-rich regions. Tin-lead microstructure consists of Sn-rich and Pb-rich lamella grains. When using metallographic polarized light microscopes, the Pb-rich grains appear as dark regions while the Sn-rich grains appear significantly lighter in color. Using backscatter electron microscopy, where there is contrast between elements and compounds with different atomic numbers, Pb-rich regions appear as light areas, while the Sn-rich appear as dark areas. Upon reflow, tin-copper or tin-nickel intermetallic structures form between the solder, lead, and pad. If the solder joint is subjected to extended periods of time at high temperatures, the tin and copper or tin and nickel continue to interdiffuse and the intermetallic region begins to grow. At some point, the strength of the intermetallic is reduced by compositional changes caused by this growth. Dimensioning the intermetallic is a good way of determining whether or not the joint has been embrittled by exposure to heat. The tin-rich and lead-rich regions of the solder also experience

growth when exposed to high temperatures for some extended period of time. The growth of these regions can be accelerated by thermal or mechanical stress. Often, this stress will also orient the grains in a direction that helps to relieve this stress. An example of an oriented tin-lead grain structure is shown in Figure 1. This growth, movement, and orientation is termed grain coarsening. Grain coarsening weakens the joint and is a primary indicator of thermal or thermo-mechanical fatigue. Often cracks that form in tin-lead solder joints after thermal cycling occur in the lead-rich coarsened grains near the interfaces.

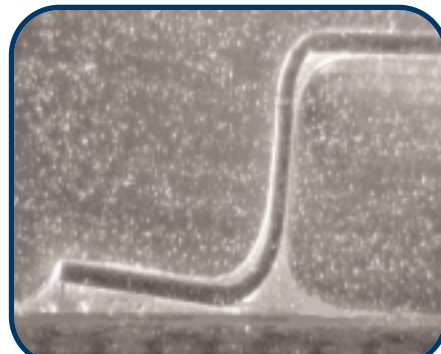


Figure 2. Optical picture of gull-wing solder joint. This micrograph is used to dimension the joint geometry.

Tin-based lead-free alloys exhibit vastly different bulk solder microstructure. Where tin-lead alloys exhibit distinguished Sn-rich and Pb-rich grains, the majority of tin-based lead-free alloys exhibit intermetallic structures within the tin-matrix. These intermetallic structures are composed of a ratio of tin and some other elemental constituent of the alloy (e.g. Ag₃Sn). Intermetallic structures comprise a small percentage of the area within the solder joint because of the relatively low percentage (3-5 wt%) of alloying elements. The intermetallic structures do not take on a lamellar form; rather, the morphology varies, exhibiting a round, lathlike, blocky, or needle-like structure. In lead-free joints, the coarsening effect has not been documented however, lead-free joints exhibit interfacial intermetallic growth similar to tin-lead and therefore can be used as a process and service indicator.

Cross-sections of solder joints are also performed to investigate wetting and

joint geometry. Many of the standards such as minimum fillet height, wetting angle, toe, knee, and heel coverage can be measured and compared to industry standards such as IPC-A-610 "Acceptability of Electronic Assemblies." An example of an optical micrograph used for IPC acceptability standards is shown in Figure 2. These standards are occasionally used as process indicators. Poor plating and voiding are two other often seen anomalies of solder joint cross-sections. Often, the adjustment of a reflow profile or component placement location can result from examination of a solder joint cross-section.

Summary

- Metallographic analysis is often used in conjunction with other analysis methods such as Fourier Transform Infrared Spectroscopy (FTIR), scanning acoustic microscopy (CSCAN), and ion chromatography (IC) to provide a complete history of the process conditions, service conditions, and reliability of surface mount and through-hole mount solder joints.
- Samples must be prepared carefully using the proper equipment and materials in order to produce an interpretable sample.
- Although there are many more examination techniques, the most popular and efficient techniques are polarized light microscopy and scanning electron microscopy with EDS.
- The microstructure of tin-lead and lead-free joints are different yet they both can provide some clues to the conditions and reliability of the solder joint.
- Solder wetting and joint geometry are two key areas that can be used to optimize the assembly manufacturing process.

Moisture Sensitive Devices (QFPs and BGAs)

(continued from p. 1)

over several production runs, goes through the baking cycle multiple times. Each time the component is baked, moisture is driven out, but oxidation of the tin/lead is occurring. The greater the oxidation on the solder the lower the solderability, therefore baking the components may result in unsolderable components. This effect typically would occur only after several baking cycles, and would not typically occur after only 1-2 bakes.

In order to alleviate this excessive baking, some assemblers have dry storage locations for moisture sensitive components to be kept until needed. It was assumed that this storage "stops the clock" with respect to moisture ingress.

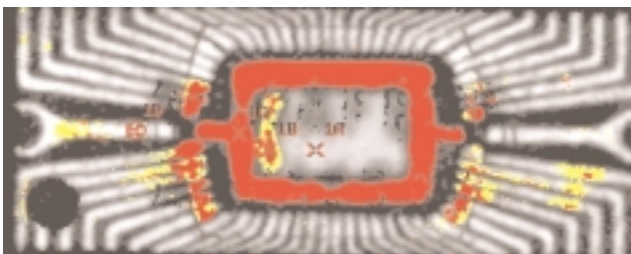
A recent paper by Shook and Goodelle² investigated the effect of dry storage after moisture exposure. One example from the paper illustrates a level 5 component (max 48 hours exposure) exceeded the critical moisture limit after 16 hours of exposure followed by 70 hours of "dry" storage. Dry storage will slow the process, and if left in a dry environment long enough the part will eventually dry out. The IPC/JEDEC standard specifies a minimum dry storage time of five times the exposure time in order to re-set clock back to zero¹.

The most common failure due to moisture in the packages is popcorning. This failure is so named since the effect is the same as what occurs during the popping of popcorn. These defects are not often visible to the naked eye, but can be the source of a number of internal damage to a plastic package, such as: wire bond breaks, die cracks, tab bond fracture and delaminations. The tool most often used to inspect for popcorning defects is scanning acoustic microscopy. This effect is dependent on both the amount of moisture in a package, rate of temp increase, and peak of temperature increase. The latter two factors come into play as people start to consider moving to lead-free assemblies. The higher reflow temperatures required will impact the moisture resistance levels of MSDs. Researchers at the EMPF were participants in an ad hoc committee looking into the effects of lead-free on component processing. This group presented a paper at IPCWorks 2000 in Miami³. The results of the MRT testing showed that some packages had a shift of as much as 4 levels (see table 1 on pg 1). Component manufactures are working on new packaging plastics that will be more resistant to

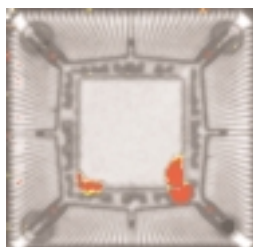
moisture ingress and be more robust with respect to high temperature processing and moisture ingress.

The drive for more functionality and cheaper components continues to add complexity to the manufacturing process.

Moisture sensitive components are one factor that adds to the complex nature of the manufacturing environment. Quality control and understanding the issues at hand are critical to minimizing this affect on your product.



Scanning Acoustic Microscope Images of delaminations in plastic packages (images courtesy of Sonix)



Common terms and definitions related to moisture sensitive devices:

Active Desiccant: Desiccant that is either new or has been baked according the manufacturer's recommendations in order to restore its effectiveness.

Desiccant: A moisture absorbing material. Used to maintain a low relative humidity in moisture barrier bags. Typically a silica-gel or other material packed in dustless pouches.

Floor Life: The allowable time period, after removal from a moisture barrier bag and before the soldering process that a moisture sensitive device should be exposed to ambient conditions not exceeding 30°C and 60% RH (according to J-STD-033).

Humidity Indicator Card (HIC): A card printed with a moisture sensitive material that changes color from blue to pink when the indicated relative humidity is exceeded. Cards typically have three circles with varying sensitivities (e.g. 8, 10, and 20 %RH or 5, 10, and 15 %RH). This is typically packed in the moisture barrier bag along with the desiccant.

Manufacturer's Exposure Time (MET): The maximum time that the component manufacturer allows between baking and sealing in the moisture barrier bag. This is also the maximum time allowed at the distributor to package components into smaller lots.

Moisture Barrier Bag (MBB): A bag designed to minimize the transmission of water vapor and used to pack moisture sensitive devices. Bags should be ESD safe, flexible, and puncture resistant (see MIL-B-81705 Type I requirements). Water vapor transmission rate should be < 0.002 g/100 in² in 24 hours at 40°C after flex testing per ASTM F 392-93 condition E.

Relative Humidity (RH): The ratio of the amount of water vapor in the air compared to the maximum amount of water vapor the air can hold, at that temperature, typically expressed as a percentage.

Shelf Life: The minimum time that a moisture sensitive device can be stored in an unopened MBB, provided that the enclosed HIC, does not indicate an elevated humidity level within the bag. Should be a minimum of twelve months when stored in a non-condensing environment < 400C / 90%RH.

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3. M. Kwoka and G. O'Brien, "Lead-Free Components FOCUS Group Evaluation - Status Report I," IPC Works, 2000.

Power Electronics Teaching Factory

Methods of Solder Interconnect for Power Electronic Packages

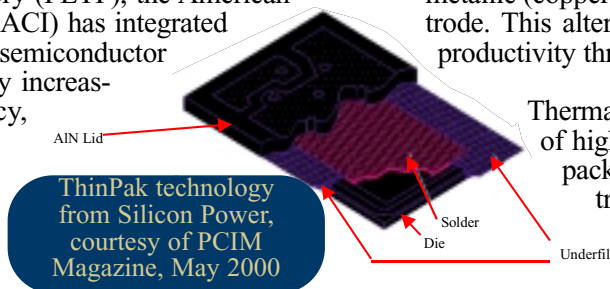
A major focus in the power electronics community today is to incorporate the advantages of modularization and standardization to reduce cost, size and design cycle time. Presently, there exist opportunities with semiconductor devices, materials, and related control technologies that will enable production of low cost "smart" power electronic modules with dramatically reduced size. These power modules must have increased power density capability, high reliability, and provide electric power control, conditioning, and very high speed switching in order to meet the technical definition of a "smart" power module. To satisfy the power density requirements of the higher power module, design modifications must take place with the semiconductor packaging to make it both smaller and more efficient. However, device operating efficiency is limited by the method of electrical interconnect to other components, baseplates and bus bars inside and outside the power module. With the cooperation of Silicon Power Corporation (SPCO) and the evolution of the ONR-sponsored Power Electronics Teaching Factory (PETF), the American Competitiveness Institute (ACI) has integrated a patented technology of semiconductor packaging that significantly increases device efficiency, enhances power density capabilities and uses the advantageous solder bonding technology.

Interconnect Technology

The integrated packaging technology, termed ThinPak by SPCO, is a semiconductor die (P-MCT, N-MCT or IGBT) soldered to an aluminum-nitride (AlN) lid with gold film deposition. Soldering thin copper strapped directly to the surface of the tin plated gold ceramic lid provides an interconnection technology to the power device cathode that eliminates the need for wire bonds and still ensures compliance under thermal cycling. This method reduces the inductance normally gained through the wire bond connections and improves the electrical performance of the device. A larger contact area is produced that greatly reduces current crowding, effectively distributes thermo-mechanical forces, and greatly reduces mechanical forces (40%) and thermal hot spots generated between wire bonds. The application of the AlN ThinPak packaging also contributes to improved thermal performance through reduced device operating temperatures. As a result, devices can be placed closer together to improve power density and reduce thermal stresses by decreasing thermal expansion strain. Using the ThinPak technology will allow the transfer of the high power semiconductors to the commercial industry for incorporation into appropriate power systems. The ThinPak will exist as a single, durable, efficient, independent power device suitable for high power, fast switching applications.

The wire bonded interconnects for power electronic devices provide the electrical path of current flow between devices inside and outside a module. However, with every bond there

is a magnitude of inductance to consider when analyzing device impedance. This becomes significantly apparent when attempts are made to increase the overall current flow through the device. Additional wire bonds or thicker bonding wire is required to compensate for the increased current flow. Consequently, the overall integrity of the package becomes compromised through increased impedance. The alternate interconnect method to reduce the aforementioned parasitics and device impedance employs the technology of direct bonding, currently used for ThinPak-based systems or power modules. Direct Bonding (DB) is not prevalent in the power electronics industry when considering device interconnects to both sides of a die. However, with the evolution of the ThinPak technology, DB is used to eliminate wire bonds and electrically connect both sides (electrodes) of the die. Whereas wire bonding involves the diffusion of two metals through an ultrasonic or thermocompression technique, direct bonding requires the application of solder to form the joint between a metallic (copper) conductor (or substrate) and the device electrode. This alternative method will lead to increased device productivity through improved manufacturing processes.



Thermal management is critical to the development of high-power electronic device and power module packages. The heat generated by these packages is transferred to the ambient environment through an attached heat spreader or thermal dissipater. Copper is the most common heat spreader material for power modules due

to its high thermal conductivity, easy mechanical handling, galvanic plating, and moderate pricing. Unfortunately, the CTE mismatch between copper and silicon presents a disadvantage that often leads to mechanical failures between the interface of the device substrate and copper heat spreader. Stress and mechanical strain in the interfacial layer (i.e. solder or conductive epoxy) aggravate cracks or voids under high power cycling, causing increased thermal resistance between the device substrate and copper heat spreader. For this reason, the interfacial layer becomes one of the primary sources for power package failure and a key area for optimization. Through process control and improved bonding techniques, thermal management and mechanical strength can be improved to increase the reliability of the interface connection. Another solution to minimizing the CTE mismatch would be using Aluminum Silicon Carbide (AlSiC) as the heat sink material, but high cost and attachment methods prove to be unfavorable in the power module industry. An epoxy system would be required for attachment of the AlSiC heat spreader to the module baseplate, but epoxy is not as thermally conductive as solder, so this would also be undesirable for the power industry.

Alternate interconnect technologies such as the Dimple Array from CPES at Virginia Tech, Power Overlay Technology from General Electric, the Bottom-less Flip Chip technique from Fairchild Semiconductor, and the Copper Strap technique

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Boot Camp: Where Theory and Practice Converge

In today's ever-changing electronic manufacturing environment, there is a great demand for qualified personnel who truly understand the complexities of modern manufacturing practices. There is no time to spend on "trial and error" process development. You must have process engineering personnel who can achieve the desired results in a timely and efficient manner. Unfortunately, as good as most academic engineering programs are, all have one common denominator. None provide actual "hands on" training using modern manufacturing equipment in a "real world" manufacturing environment.

The question remains: how do you expose inexperienced personnel to the real world without sacrificing valuable manufacturing time? The answer to this question can be found at the EMPF's Learning Center. The electronics manufacturing productivity facility (EMPF) recognized the lack of training options available to manufacturers who wanted to expose their engineering and operations staff to actual manufacturing scenarios. For this reason the EMPF has developed an intensive two week training seminar known as "Boot Camp."

The EMPF has a clearly defined mission. Operating as a Naval Center of Excellence under the leadership of the American Competitiveness Institute (ACI) and in conjunction with the Office of Naval Research, one goal of the EMPF's Learning Center is to provide thorough knowledge based training to engineering and operations personnel involved in the complex world of electronics manufacturing. The EMPF achieves this mission by partnerships with academia, equipment and materials manufacturers and private industry forming an exceptionally strong alliance to find solutions to the problems associated with today's electronic manufacturing requirements.

Boot Camp is two weeks of intensive electronics manufacturing training geared specifically towards those individuals in your organization who will make the decisions on how your electronics manufacturing processes will be deployed. The specific topics covered throughout the two-week period will have great impact on the success of your manufacturing processes. Areas of interest covered include material selection, reliability, acceptability standards, statistical process control tools, design of experiments and all aspects of the manufacturing process relating to electronics. The attendees will know the fundamental theory and application of processes such as stencil printing, adhesive dispensing, automated optical inspection, automated component placement, thermal profiling, reflow processing, wave soldering, aqueous and solvent cleaning and cleanliness verification. Not only will the attendees have a thorough understanding of the science of the process involved, they will also have the opportunity to perform the processes using our state-of-the-market manufacturing equipment. The ability for the attendees to use the manufacturing equipment provides a unique advantage in seeing first-hand the effects of process parameter changes to the success of the process. What happens if squeegee pressure is too high? What effect does insufficient heat in the thermal profile have on solder connections? These questions not only can be discussed, but can also

be visualized by the "hands-on" applications throughout the two weeks session.

Although the volume of material presented to the attendees is great, the course is structured accordingly to provide continuity between theory and application. Technical experts familiar with a particular discipline present each module of the material. The course material is first presented in lecture form in the classroom environment. This allows a structured presentation of the material as well as the opportunity for class discussion and interaction. Immediately following the lecture presentation, the attendees will proceed to the manufacturing floor of the EMPF where they can apply the theory into practice. This is truly where the EMPF Boot Camp has a distinct advantage over other training regimens. The ability to immediately turn theory into practice is a powerful learning advantage. Just talking about developing a thermal profile and actually developing a working profile are very different experiences. Interaction and discussion amongst the attendees combined with the technical expertise from our staff and the ability to

regulate and analyze process parameters and results combine into a powerful and insightful learning experience. In addition, the attendees will be provided with all course material required including study and reference materials for the topics discussed. These reference materials are invaluable not only during the training sessions but throughout the attendees working career as well.

If you believe the Boot Camp may be a valuable training aide to your engineering staff, providing valuable "hands-on, real

world" manufacturing experience, please contact the EMPF Learning Center. The two-week sessions are scheduled quarterly throughout the year and held at the ACI campus in Philadelphia. The EMPF Demonstration Factory is equipped with the latest manufacturing equipment provided through our partnerships with the leading equipment manufacturers in the industry. Manufacturers such as Electrovert, BTU, Cookson, Samsung America, Technical Devices, and many other leading equipment manufacturers help to make the EMPF the premier manufacturing training facility.

Further evidence of the value of the training provided by the EMPF can be found on TECHNET, an internet based technical forum for the electronics manufacturing industry. A recent Technet inquiry asked about training options available to electronic manufacturers. An unsolicited response was submitted by one manufacturer who stated, "There is really no substitute for the hands-on training provided by the EMPF. Their approach is professional, informative and provides real world experience that is not available with computer based training options."

If you would like to experience the challenge of the EMPF Boot Camp, please contact our registrar at 610-362-1295 for further information regarding scheduling of classes and registration.

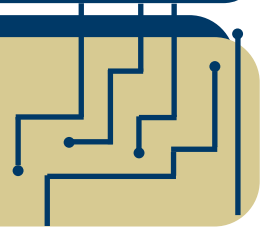
"There is really no substitute for the hands-on training provided by the EMPF. Their approach is professional, informative and provides real world experience that is not available with computer-based training options."



Electronics Manufacturing
Productivity Facility

TECH TIPS...

Flip Chip Underfill Processing
part II



Cut here and save!!

Last month's *empfi* featured part I of "Flip Chip Underfill Processing." This month, Tech Tips features part II of this article with information on types of underfills, dispensing patterns, dispensing accuracy, choosing the right needle, curing the underfill, and increasing flip chip processing throughput.

Types of Underfills

There are many types of underfills used in industry today. The four most commonly used underfills are snap cure, low profile, high performance, and reworkable.

Snap Cure: Snap cure underfills are typically used in a production environment because of their fast flow rate and quick cure time schedule. This type of underfill is also high in reliability and can fill a gap as small as three mils. The only disadvantage to using the snap cure is that it may not be as reliable as the high performance underfills depending on the end use of the flip chip.

Low Profile: This type of underfill is much like the snap cure except that it is better suited for flip chips that have smaller gaps to be filled.

High Performance: High performance underfills are typically used in a prototype environment because of their slower flow rate and longer cure time schedule. The advantage of using this type of underfill is its high reliability factor. It can absorb much more of the coefficient of thermal expansion (CTE) than that of the snap cure and low profile types of underfill, allowing experimentation to take place on the flip chip where the CTE mismatch is unknown.

Reworkable: Similar to that of the snap cure and low profile underfills, the reworkable underfill has a fast flow rate and a quick cure time schedule, but at higher temperatures. The advantage to using this type of underfill is that it is reworkable where the other underfills are not. The disadvantage is that it may be more expensive to use in terms of cost of the underfill material and the actual rework labor involved.

Dispensing Patterns

There are three commonly used types of dispensing patterns: single side, L-shaped, and modified U-pattern.

Single Side: The single side pattern dispenses underfill along one side of a flip chip. If the fillet size (size of the angle between the top of the chip and surface of the board) is not important, the entire amount of adhesive can be dispensed along the longest edge of the die in one

shot. If a smaller fillet is desired, then a multiple straight-line pass with a smaller needle is used to limit the fillet size. This pattern also provides the slowest flow out which allows the least amount of trapped air. However, the single side pattern makes it difficult to control the fillet size along the three opposite sides of the flip chip.

L-Pattern: The L-pattern allows more fluid to be dispensed in a single pass without expanding the fillet size. This pattern also enhances the speed of underfill because more sides of the die are used to initiate the fluid flow while providing better fillet control on the adjacent sides compared to that of the single side pattern. However, the L-pattern may create air pockets (voids) under the die if one flow front becomes ragged and meets the second flow front in a way that would trap an air bubble.

Modified U-pattern: The modified U-pattern optimizes fluid flow under the die making it the quickest dispensing pattern with the most consistent control of fillet size around the perimeter of the flip chip. However, similar to the L-pattern, the chance of air pockets becoming trapped is increased.

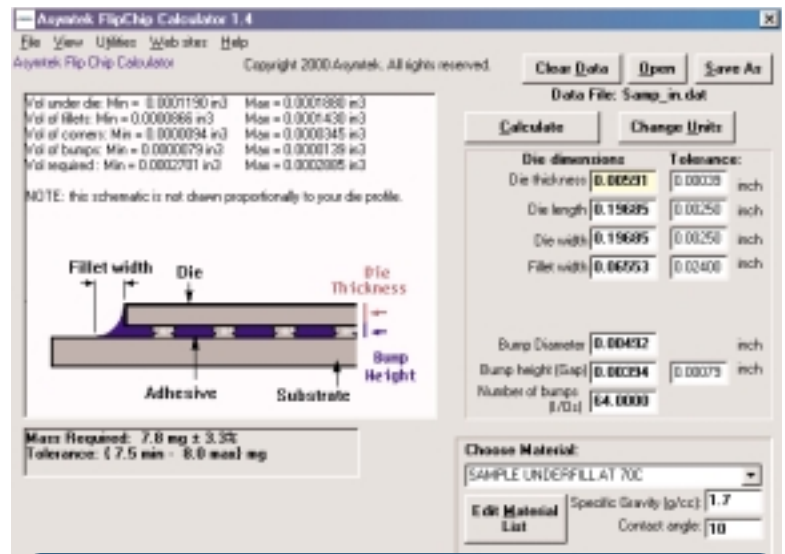


Figure 1: software is available that will automatically calculate the amount of material required based on the size and desired fillet width of the flip chip. Copyright 2000 Asymtek Flip Chip Calculator v1.4

Dispensing Accuracy

To get reliable parts from the underfill process, the right amount of underfill material must be dispensed in the right pattern in a well-timed sequence. The amount of material dispensed is geometrically computed by adding

continued on p.8

Flip Chip Underfill Processing

(Continued from p. 7)

the volume under the chip to the volume of the fillet, then subtracting the volume of the interconnect bumps as shown using the following formula:

$$V = VC - VB + VF$$

VC - Volume under the die = die length x die width x underfill gap

VB - Volume of the interconnect bumps = area of cross section of bumps x underfill gap x number of bumps

VF - Volume in the fillet = [fillet height x fillet width x 2 (die length + die width)] + p/3 (fillet width) 2x (fillet height)

Underfill Dispensing Tolerances: The tolerance on the amount of material dispensed depends on the physical tolerances of the die and fillet. The minimum amount of underfill dispensed to ensure that the part has been underfilled properly occurs when the dispense gap is at its maximum and the fillet width is at its minimum. The maximum amount of underfill material that can be dispensed occurs when the gap is at its minimum tolerance and the fillet is at its maximum width (see Table 1 below). As the die size increases, so does the volume under the die (faster than the volume in the fillet). This makes the fillet the reservoir that compensates for variation of volume under the die.

The following conclusions can be made about dispensing tolerances:

- The fillet is the reservoir that absorbs the changes in the dispense gap from part to part.
- Larger dies have tighter tolerances by percentage because the volume under the chip is relatively larger than the fillet.
- The more accurate the dispensing tolerance can be held, the tighter the fillet tolerance can be held.

Choosing the right needle

Due to the importance of accuracy and volume, the type of needle being used is a critical factor. There are a variety of needle shapes and sizes that are either

plastic or metal and have straight, bent, and tapered tips. The size of the needle is identified in wire gages 14-30. To determine what type of needle to use, you need to know what kind of material you are dispensing and how much, in terms of volume, you need to dispense. For example, in dot dispensing the size of your dot should be the same diameter as your needle tip. This also applies to underfilling, but in terms of lines.

Curing the Underfill

Curing the underfill has classically been performed in some type of convective and/or radiant oven situated in-line after the fluid dispenser. However, microwave curing ovens have been implemented in the line because of the improvement in reduced fillet residue that is sometimes left behind. The curing schedule for the underfill depends on the type (snap cure, reworkable, low profile, or high performance) and what the particular manufacturer recommends.

Increasing Flip Chip Processing Throughput

The following is a list of suggestions that can help increase throughput and may reduce process defects during flip chip underfilling:

- Heat the packages prior to the dispensing step.
- Add a post-dispense station to complete the fillet around the perimeter of the chip and/or to dispense more fluid under the die if required. This will prevent a bottleneck where the original underfilling step took place.
- Use a dispenser that has automated set-up procedures and can automatically calibrate the amount of volume required to underfill the flip chip.
- Use a dispenser with automatic fiducial recognition software.
- Choose a pump or valve with a fast flow rate to help reduce dispensing time.
- Use easy to clean pumps or valves, preferably ones that can be cleaned off-line to reduce down time.
- Having more than one pump or valve ready to change will also keep your line from shutting down. Use multiple dispensers to do more than one flip chip in a single pass.
- Manipulate the SPC (Statistical Process Control) data from your dispenser so the quality of your product can be monitored while maintaining a consistent throughput.

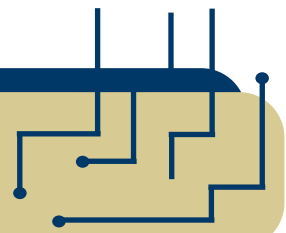
Table 1. Dispensing Tolerance Examples

Example #	Die Size (mm)	Max Gap (mm)	Min Gap (mm)	Fillet Height	Min Fillet Width (mm)	Max Fillet Width (mm)	*Shape Factor	Dispense Tolerances %
1	15	0.09	0.07	1	2.5	1.5	1	15.8
2	15	0.09	0.07	1	2.5	1.5	0.3	1.8
3	25	0.09	0.07	1	2.5	1.5	1	9.9
4	25	0.09	0.07	1	2.5	1.5	0.3	-5.8

* The shape factor is dependent on the type of underfill fluid and its wetting characteristics. This is usually a function of the contact angle which is provided by the underfill manufacturer.

Manufacturer's Corner

Glenbrook Technologies Analyzer Software



The January 2000 edition of the *emp-fasis* featured an article on the Jewel Box 70 X-ray system from Glenbrook Technologies. Glenbrook has continued its support of the EMPF with a system upgrade for analyzing ball grid array (BGA) and Micro-BGA components. The BGA analyzer software provides image processing capabilities and BGA integrity evaluation. The Glenbrook X-ray system is a valuable tool for customers in the analytical laboratory and in process prove out. The BGA analyzer software also aids students in understanding and interpreting X-ray images.

Locating and Identifying Potential Defects in Solder Balls

Locating solder defects requires highly skilled and trained personnel. Depending on the defect location, component type, ground planes and board geometry, the X-ray image and clarity can be hindered. Glenbrook developed a way to assist customers in identifying these defects. The analyzer software enhances the image allowing the ball(s) defects to be highlighted. This option is important for the EMPF's training center and the analytical laboratory. This software option will improve the EMPF's capability to identify and recognize defective solder joints.

Measuring Solder Ball Size, Shape and Orientation

Having consistent ball size, shape and orientation is ideal when evaluating BGA solder joints. The analyzer soft-

ware will "map out" the ball grids patterns and compare each solder joint. Having all the balls symmetric and uniform indicates the process is working correctly. Irregular shaped balls are good indications of poor wetting, excess, or insufficient solder. The software will apply an overlay to the image on the screen and give a graphic illustration of what the solder joint looks like, which is effective when determining ball size and consistency. This data is important in process development and provides a good visual aid for easy identification.

User Defined Pass or Fail Criteria

X-ray users will be able to benefit from the software by setting up a pass or fail criteria developed from process prove out. Users are able to select a pass or fail criteria dependent on ball size, shape, and orientation. This will help make the inspection process quicker and easier and also help reduce the error of questionable solder joints. Operators will be able to see instantly if the printed circuit board (PCB) they are inspecting is acceptable or not.

View Measurements

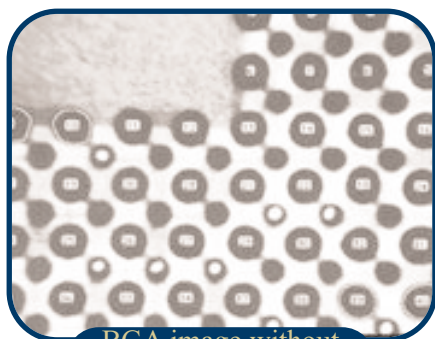
Part of the analytical benefits of the software is the raw measurement data that is displayed in a 3-D graphical mode or in a spreadsheet style. This information helps in identifying failure modes. Having information that will provide a pattern is useful for repeatability. The raw data can be compared to assemblies built today, yesterday, last month, and so on, thus creating a

history and a process indicator. The EMPF can keep customer records on particular assemblies and can be compared or used for future failure modes.

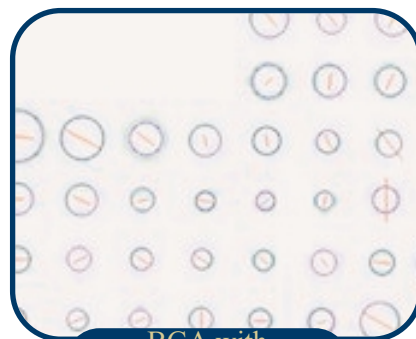
Full Image and Sectional Analysis

Full image and sectional analysis helps to define the area failure mode. For example: a full image with balls in the center of the package that are smaller than the balls on the perimeter of the package may indicate poor wetting or not enough heat to reflow the solder balls in the center. Taking that a step further, one can capture sections of a BGA, potential problem areas, and compare them to other assemblies to see if the problems are consistent from one assembly to another. Simple random sampling allows for tighter process control measures.

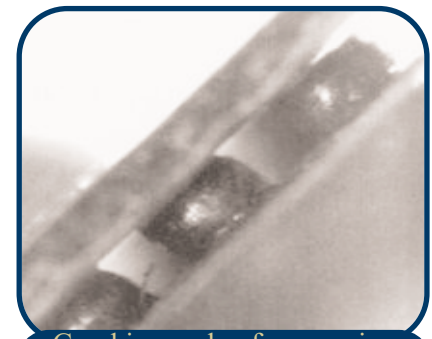
As technology, assemblies, and components rapidly change, the need for BGA inspection services are rapidly growing. Having useful tools such as the BGA analyzer helps to maintain the competitive edge needed to provide solutions to our customers. This software not only enhances our capabilities but helps to provide in-depth analysis of customers products and will provide even more useful data in proving out processes and failure modes. Customers can have the satisfaction of knowing that the EMPF has used the necessary tools and the latest state of the art equipment industry to evaluate their assembly.



BGA image without analyzer software



BGA with analyzer software

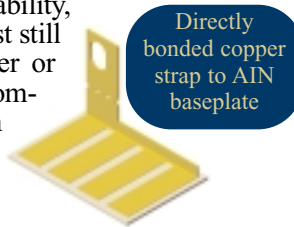


Graphic overlay for mapping ball size and symmetry

Power Electronics Teaching Factory

(continued from p. 5)

from International Rectifier have been brought about due to the demanding requirements of higher power density, higher power conversion efficiency and better reliability on today's power modules. Three-dimensional interconnect techniques such as these are at the forefront of research for simultaneous breakthroughs in performance, reliability, cost and manufacturing, but they must still endure the reliability issues of solder or epoxy bonding systems. This is a commonality that will improve through the current research and development under the PETF.



Improved Methods of Interconnect

With the implementation of the PETF, the EMPF has the ability to investigate improved methods of solder interconnect for power semiconductor devices and packages. Through the evolution of the ThinPak technology and the planned development

for a manufacturing process, EMPF engineers have established procedures for solder bonding between metallic substrates and power device packages. Taking the next step into power module manufacturing, EMPF has become educated on the various types of bonding techniques used for satisfying specific power packaging issues. Thermal coefficient of expansion (CTE), mechanical strength, fusing current, and module density all exhibit parameters that depend on the bonding technique employed within the power module.

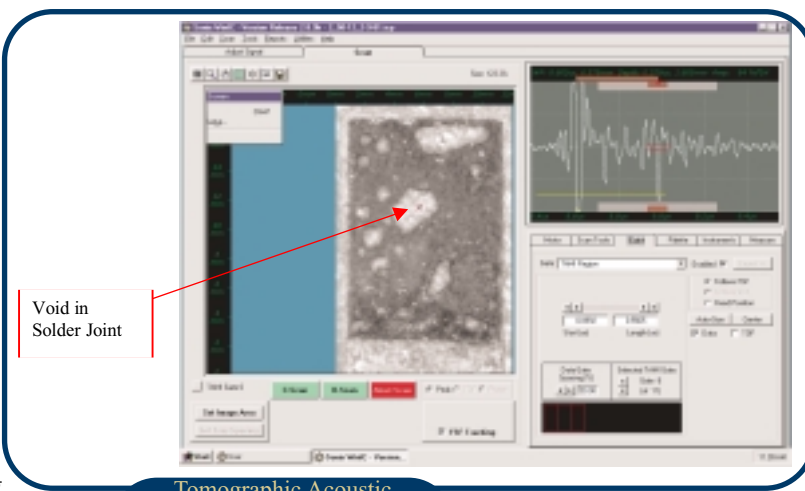
Direct copper bonding (DCB) or "brazing" is another attachment method employed in the power module design. This allows for the direct connection of thin copper conductors to

ceramic (Aluminum-Nitride) for thermal distribution and mechanical strength. The excellent thermal conductivity and CTE match with silicon provides the possibility of very close packaging of semiconductor devices. This translates into more power per unit of volume and improved reliability of power module based systems. Packaging trends use DCB as the basis for "chip-on-board" technology and implement a higher degree of integration for component attachment. During this progression into the future of power module manufacturing and device packaging, the EMPF will develop processes for solder attachment methods to use in higher levels of component to substrate integration. The ideal process will provide the solder joint characteristics required to maintain improved voltage drop and fusing current while not sacrificing the integrity of the power package.

Solder is the preferred choice of bonding agent for package to substrate interconnection. The EMPF is pushing forward

to optimize this interfacial layer by designing methods for removal or minimization of the voids in the solder joint. The heat generated by the devices is transmitted through the solder joint to the heat spreader, so the voids (or air gaps) that are present in the solder layers disturb the thermal conduction of the device and introduce anomalous thermal spreading. Voiding is mainly dictated by the outgassing of entrapped flux in the solder joint during reflow and the solderability of the metallization. Maximizing the flux activity and the solderability of

the metallization will decrease the voiding and lead to improved thermo-mechanical properties in the interfacial joint. The EMPF is using the knowledge of various solder patterns and solder paste formulations to combat the mechanisms of voiding and optimize the bonding process. This approach is intended to reduce the outgassing phenomenon and reduce the interface layer to an appreciable thickness. Results will yield a reduction in air gaps, thermal hotspots, mechanical stress and strain, and thermal resistance. Moreover, the thermo-mechanical properties will improve to a level that greatly minimizes deterioration.



Tomographic Acoustic Micro Imaging (TAMI) scan of solder interface between semiconductor package and substrate.

"ThinPak Technology Shrinks Power Modules, Power Hybrids and Ultra-High Speed Switching Devices," PCIM Magazine, May 2000, pp. 34.
"ThinPak Technology Shrinks Power Modules, Power Hybrids and Ultra-High Speed Switching Devices," PCIM Magazine, May 2000, pp. 34.
Haque, Liu, Lu and Goings, Power Elec. Packaging Lab, CPES, and Sonix Inc., "Thermal Management of Power Electronics Modules via Acoustic Micrography Imaging," Article from Virginia Tech and Sonix Inc., pg. 1.
Wen, Huff, Lu, Cash, and Lorenz, "Dimple-Array Interconnect Technique for Interconnecting Power Devices and Power Modules," Article from Virginia Tech and U. of Wisconsin- Madison, pp. 1.
"What is DCB and Where is it Used," IXYS Website, 1998, pp. J-23.
Hague, Lu, Goings, and Sigmund, "Characterization of Interfacial Thermal Resistance by Acoustic Micrography Imaging," Article from Virginia Tech and Sonix Inc., pp. 2.

Ask the EMPF Helpline!

CUSTOMER ISSUE

Recently, a customer called the EMPF Helpline requesting assistance in the evaluation of a printed wiring board (PWB) assembly for manufacturability as it applies to IPC-A-610.

EMPF HELPLINE RESPONSE

The EMPF Helpline team evaluated the PWB using IPC J-STD-001, IPC SM-782, and IPC-A-610 industry standards documents. Non-destructive magnification and laser measurement tools were used to verify dimensional specifications.

Evaluation Results:

- Surface Mount components land patterns are within the IPC SM-782 requirements. Achieving pasting, placing, and reflowing with acceptable results should be possible.
- The PWB was a double sided board with significant SMT and through hole components.
- Majority of the through hole components are inserted by hand.
- Land patterns are gold plated. The manufacturer must adjust process to solder to nickel. Hot Air Solder Leveled (HASL) finish would provide an easier soldering surface than nickel. The surface is very robust and flat but a higher than normal temperature profile will be required. The board thickness and heavy copper layer count will require special temperature profiles to achieve acceptable reflow soldering process results.
- The PWB is approximately 0.090" thick with heavy and multiple internal ground planes. The through hole components are typical for 0.062" thick PWB, causing the leads not to protrude through the PWB and making the heat transfer difficult. Difficulty in heat transfer will not promote good wicking to satisfy vertical solder fill requirement. The level of difficulty to obtain a class three assembly is very high based on compliance to IPC-2222 design standards. If the PWB does not comply to standards, the process results will not comply with IPC-A-610 acceptability standards.
- The secondary components should be glued to the board and wave soldered with the through hole components. Some shadowing may occur due to the position of 0603 chip components. This shadowing may result in insufficient solder and solder skips.
- Adhesive application will require stringent process control parameters. Components on the secondary side of the board are quite small and resistor packages with 0.03" pitch castellations push the limits of adhesive printing. Adhesive dispensing would provide good control but could slow the process down.
- There are a number of SMT components on the primary side of the board placed under sockets. Connectors will require hand installation.
- The capability of In Circuit Testing (ICT) is minimal due to the accessibility of components under connectors and the board design itself.
- Double sided reflow process with selective wave soldering of the through hole devices could be used provided a fixture is designed to prevent shadowing and sufficient heat transfer to the board. A connector with solder performs may aid in the soldering process since the leads do not protrude through the board. Pin in Paste with a tight process control window is a valid soldering option as well.

Recommendations:

Process yields from this assembly will depend on good process control. Application of adhesive, wave soldering process, and the reflow temperature profile will demand special attention. A high skill level may be required to achieve acceptable hand soldering assembly. The test cycle will be costly as there appears to be little provision in the design to support testing.

If you have an electronics manufacturing problem, call the free EMPF Helpline at (610) 362-1320

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American Competitiveness Institute
 One International Plaza
 Suite 600
 Philadelphia, PA 19113
 (610) 362-1200 • FAX: (610) 362-1290
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