empfasis

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The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

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DoD COLLABORATIVE EFFORT ON THE ARS-6

The American Competitiveness Institute (ACI), under direct support of the U.S. Army CECOM and in partnership with the U.S. Navy and joint DoD program offices, are collaborating with industry partners to redesign the Air Radio Set (ARS-6). This radio is used by military aircraft for conducting search and rescue missions to locate personnel equipped with PRC-112 survival radios. The Open Architecture's non-custom, proprietary redesign effort will reduce cost, improve both reliability and supportability, and include new feature upgrades such as the Global Position System (GPS) currently being designed into the next generation military radios.

Background:
The AN/ARS-6 Radio Set is the airborne part of a system for Combat Search and Rescue (CSAR). The system includes a handheld radio (responder) that addresses a Personnel Locator Set (PLS). The AN/ARS-6(V) Radio Set is the essential airborne component of the PLS, and provides the rescue team with the identification, direction, and distance to the responder radio. (See Figure 1)
Together, the responder radio and the AN/ARS-6 Radio Set are the standard CSAR system for the U.S. Army, Navy, Air Force and NATO. The airborne guidance system covertly and precisely locates downed or missing pilots - in a single pass under harsh operating conditions - while concealing the war fighters' location from the enemy.

The existing AN/ARS-6 Radio Set is a unique, custom design composed of the following components: control display unit, antenna switching unit, receiver/trasmitter, mounting base, remote display unit, antenna set.

The cost of sustaining this system is expensive, and is considered excessive by the government.

Current Status & Areas for Improvement:
Field maintenance of the AN/ARS-6 Radio Set is limited to task categories at the operator's Aviation Unit Maintenance (AVUM) and the Aviation Intermediate Maintenance (AVIM) levels. In essence, this permits only exchange of Line Replaceable Units (LRUs), and excludes any attempt to repair these units in the field. For repair, the LRUs are returned to the U.S. Army Depot at Tobyhanna, Pennsylvania (TYAD).

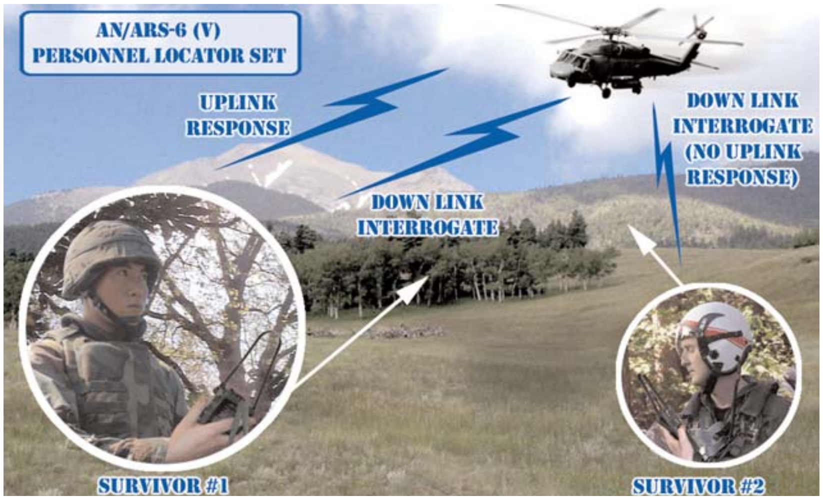

Figure 1: The Personnel Locator Set (PLS) consisting of the ARS-6 transceiver located in the helicopter communicating with the survival ground radios.

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DoD COLLABORATIVE EFFORT ON THE ARS-6
(continued from page 1)

It is now necessary to upgrade the obsolete electronics of the ARS-6 system. Replacement of the outmoded through-hole technology of these modules with state-of-the-art surface-mount technology does decrease the cost of these modules, overcomes the increasing problems of component obsolescence, and miniaturizes the systems with concurrent savings in both weight and space. This creates the opportunity for the addition of increased functionality into the AN/ARS-6 Radio Set, such as inclusion of integrated GPS capabilities.

Re-Design Packaging:
To mitigate the current maintenance and repair problems of the AN/ARS-6 Radio Set, while substantially decreasing both the initial and lifetime cost of operation, the American Competitiveness Institute (ACI) has initiated the following engineering re-design approach:

1. Implement an Open Architecture re-design for the ARS-6 using COTS components/modules, and base it on industry standards with interface specifications that are public domain instead of proprietary, or "closed" custom designs.

2. Top level system design identifying the COTS modules and dividing the RF and control sections (reference Figure 3). Through the use of high level building blocks, such as a single board computer, power supply module, RF power amplifier, low noise amplifier, RF relay, splitter, and even the use of major portions of the existing PRC-112 and developing CSEL survival radios themselves, the need to do low level detailed design is greatly diminished. Also, in the event of a component or module obsolescence issue, this open architecture design concept permits relatively easy replacement of the COTS module rather than a complete redesign.

3. Software simulation of the system to ensure that all requirements and functional specifications are satisfied per the system document.

4. The ARS-6's new software will be developed for a COTS single board computer based on a standard operating system. This effort will require code for both operational control of the unit as well as diagnostic and test routines. Again, as with the COTS hardware modules, the objective is to write the code with a well documented Open Architecture that is readily understood and maintainable by an average skill-set programmer.

Re-Design Goals:

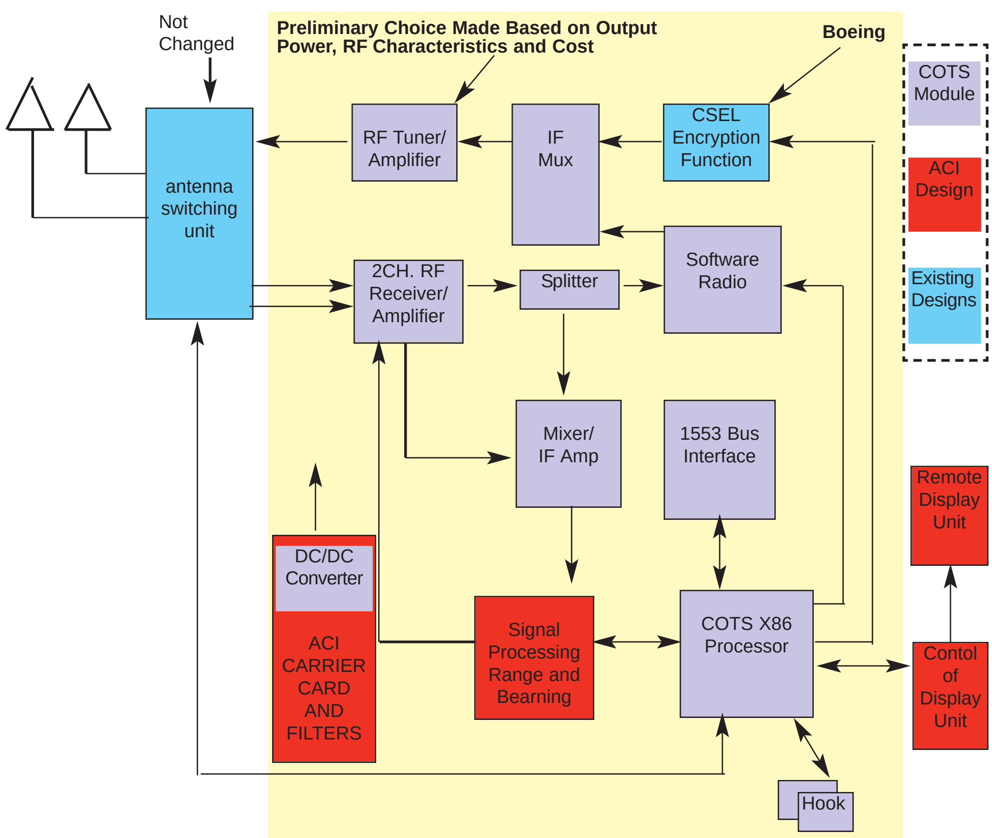
- Reduced cost (goal of < $25K) alternative ARS-6+ Receiver-Transmitter module. Modern COTS sub-assemblies and displays will provide more durable and affordable alternatives to those currently spefied, while fully matching the current display and ARS-6 system in function. It should be noted that defective displays are the most frequent LRU returns to the depot.

- Redesign of the RT-1532 Receiver-Transmitter. These RCM and SPM Module boards currently use outmoded through-hole mounting technology. The redesign will use state-of-the-art COTS surface-mount components and modules, allowing cost improvement through improved maintenance capabilities, avoidance of obsolescence problems, and miniaturization for weight nd space savings that allow incorporation of additional functionality such as GPS capability. (See Figure 2)

- Expand the self-diagnostic capabilities integral to the ARS-6+ by incorporating additional algorithms to identify not only the disabled LRU, but also the site of failure within the LRU. This information will greatly facilitate the troubleshooting operations at the depot and further reduce the quantity of LRUs that must be returned to the contractor for replacement.

A bench-top redesigned ARS-6+ open architecture system will be developed and tested at ACI. It will then be provided to the Tobyhanna Depot for functional testing and evaluation before proceeding to the next stage of developing Air Worthiness Release qualification prototype hardware.

For more information regarding the ARS-6 Open Architecture program at ACI, please contact the Helpline at (610)-362-1320.



LEAD FREE MANUFACTURING

Today lead is used in the electronic manufacturing process as a tin lead alloy solder to attach and electrically interconnect components such as IC (Integrated Circuit) chips and resistors to PWBs (Printed Wiring Boards). But that will change!

Electronics manufacturers are being required to convert their production lines from tin lead solders to lead free solders. In Europe, the Waste Electrical and Electronic Equipment (WEEE) Directive and the Restriction of Hazardous Substances (RoHS) legislation stipulates that lead will be prohibited from electronic hardware by July 1, 2006. In Asia, specifically Japan, the Ministry of International Trade and Industry (MITI) has stipulated that commercial hardware must be 75% Lead Free by January 1, 2006. In the United States, while there is no formal legislation banning the use of lead in electronics, the Environmental Protection Agency's (EPA) Toxic Release Inventory Status requires that electronic manufacturers report lead usage greater than 100 lbs annually. Therefore, it can be concluded that Lead Free Solders will be implemented into electronic hardware in the near term.

When lead is banned, the electronic manufacturing industry will have to switch to solder that contains only tin, and perhaps some small amount of silver, copper, bismuth, or antimony to improve mechanical properties of the solder. These lead free soldering alloys, such as tin-copper-silver, have much higher melting temperatures than the tin lead solder currently used. This higher melting temperature is the source of many manufacturing issues. Electronics manufacturers must take into account how these materials will interact when incorporated into the manufacturing process.

There are specific challenges to introducing lead free solders in a production environment. Lead free solders do not wet as well as tin lead. Aggressive solder fluxes and nitrogen are recommended to improve solder ability. Components and board materials are more sensitive to moisture due to lead free solder's higher processing temperatures. From an inspection perspective, because lead free solder joints have a grainy dull appearance, the IPC is revising their visual inspection requirements to compensate for lead free solder joint differences.

The process variables for performing rework and repair operations with lead free solders also needs identification and quantification. There are concerns about the quality and reliability of lead free solders, which undergo rework and repair, as well as the impact that the solders higher temperature has on the board, the components, and the assemblies.

ACI recognized that Lead Fee Soldering impacts electronics manufacturing from system development through transition to production and sustainment. Since 1999, ACI has been actively investigating Lead Free Soldering. In 2000, ACI hosted an industrial forum with the IPC on Lead Free Soldering. In 2002, as member of the Lead Free Components Focus Group, ACI was awarded Soldertec's 2002 Lead Free Soldering Award for "pioneering work on the investigation and development of lead free and lead free components in the United States". This team proved that it was feasible to meet high reliability requirements with Lead Free solders. These activities are consistent with MANTECH's objectives; to identify manufacturing challenges early and to provide timely solutions.

In order to understand the requirements of Lead Free Manufacturing, ACI has developed a Lead Free Manufacturing course. The course's objective is to introduce the technical variables associated with implementing lead free solders in a production environment. The two-day course is hands-on and utilizes ACI's Demonstration Factory. For more information on the course call the EMPF registrar at 610-362-1320.

Ask the EMPF Helpline!

CUSTOMER ISSUE: The caller was observing solder joint separations within a surface mounted transformer. They stated that initially good solder wetting was observed after re-flow of the paste. However, soon after, the component was able to be lifted off of the board. The customer provided ten pristine components, along with an assembly with obvious cracks, referred to as the "bad" assembly. They also provided a "good" assembly with no apparent separation.

Investigation Technique:

The customer requested quantitative solderability testing on the transformer. Since the component was a leaded surface mounted component, the solderability of the transformer was evaluated in accordance with IPC J-STD-002B 4.3.1 test E - Wetting Balance Test (Leaded Components). Since the failure was occurring with this particular component the source of the failure was thought due to the component and not the board. In addition to quantitative solderability testing, the following analysis techniques based upon ACI procedures were used to evaluate the failure: optical microscopy, micro-sectioning in conjunction with scanning electron microscopy (SEM) and energy dispersive spectroscopy (EDS)

The component incorporated four pins/leads which made direct contact with the pad areas. As a result of this configuration, it was necessary to section the leads from component. Only five of the ten components were analyzed for a total of ten actual measurements. Based upon the information provided to ACI by the customer, the leads were composed of a copper substrate with ductile nickel which had an electrodeposited tin finish 4 x 10-4 inches thick

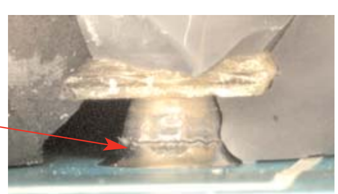
Both the "bad" and "good" assemblies were prepared for micro-sectioning during which measures were taken not to stress the solder joints. However, because of the weak solder joint and the vibrations generated from the cutting mechanism the component on the "bad" assembly dislodged from the board surface. It was determined that the sectioned board area from the "bad" assembly be prepped for SEM analysis without further treatment except for sputter coating of gold (Figures 7 and 8).

Results:

Visual Inspection of "Bad" assembly before destructive testing

Solder joint fracture

Figure 1 - Right lead at 60X.

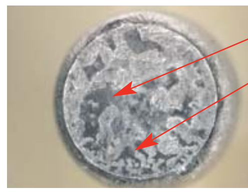


Solder joint fracture

Figure 2 - Left lead at 32X.

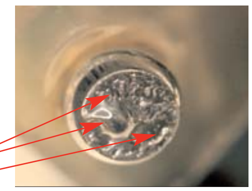
Wetting Balance:

Initial analysis of the base of the leads was not able to generate a detectable wetting force as a result only visual analysis was pursued (See Figures 3 through 6 which show the base of two leads before and after soldering).



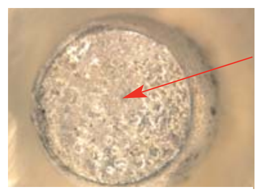
Pockets within the surface plating

Figure 3 - Before soldering at 63X.



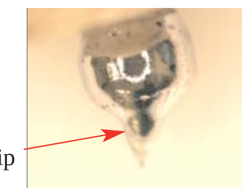
De-wetting observed

Figure 4 - After soldering at 40X.



inconsistent surface

Figure 5 - Before soldering at 63X.



good wetting at tip

Figure 6 - After soldering at 40X.

In summary, two of the ten leads analyzed showed poor solderability similar to Figure 4. The other eight leads tested showed partial wetting as in Figure 6.

SEM analysis of "bad" and "good" assembly:

Gas voids

Figure 7 - "Bad" assembly at 50X

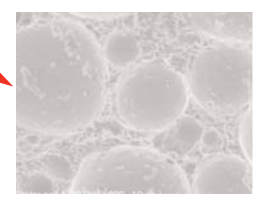
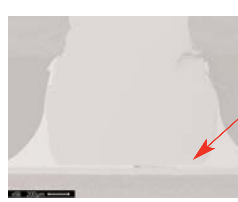


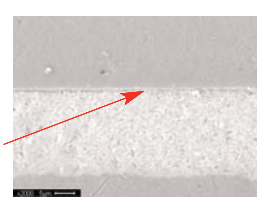
Figure 8 - Shows Figure 7 at 890X

All four pads had similar appearances as that in Figures 7 and 8.



Void Present

Figure 9 - cross-section of “good” assembly at



Demarcation line present, no intermetallic formed

Figure 10 - Figure 9 at 2000X

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Sustainment Interfaces

Sustainment engineering is receiving a great deal of DoD focus due to the large number of aging systems which are still in use. Sustaining these older systems involves a whole gamut of problems such as replacing components, boards and subsystems due to obsolete components that have become maintenance issues. Unexpected change, high cost to repair, and a desire for enhanced performance are also reasons for sustainment engineering. High cost of repair is not only increased part cost, but also the costs associated with labor and repair time. A factor that can also contribute to the high cost of maintenance is unintended damage. Older equipment becomes more fragile with age and damage can be caused when assembling, disassembling, soldering or reworking a failed unit. Wires can be broken or burned and, as the units are reworked, the solder joints fatigue and break. Circuit cards or mechanical assemblies can also be stressed and damaged.

An example of successful sustainment engineering where labor costs were reduced is ACI's approach to the C6533A/ARC Intercom. The interior of this unit had a tremendous number of wires divided into several bundles that provided point-to-point wiring (Figure 1). ACI was able to eliminate all hand wiring by placing all components on two PCBs and using mass terminated connectors to connect the two PCBs (Figure 2).

Figure 1

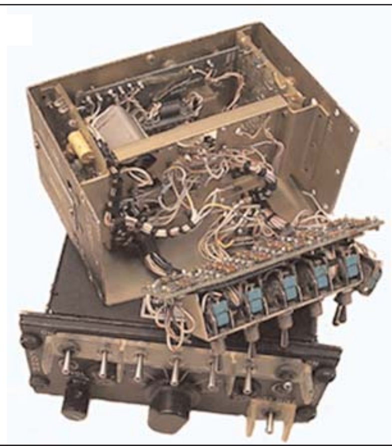

Figure 2

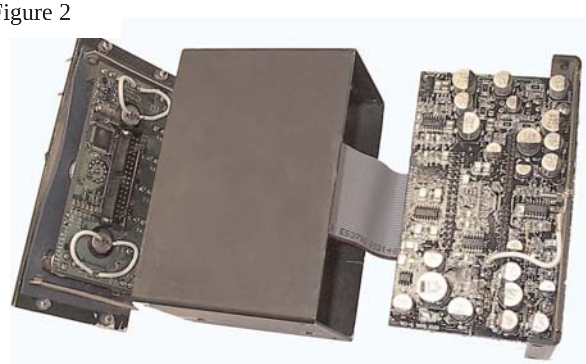

Figure 1 shows the original intercom interior, while figure 2 shows the redesigned unit

Interface Engineering takes into account all characteristics of each port of the unit or system. Figure 3 shows a generic system. Each input and output is connected to the processor (not necessarily a computer). Each of the interfaces A thru E in Figure 3 have unique requirements. One interface can be connected to several different types of equipment in different system applications as shown in output A and output B.

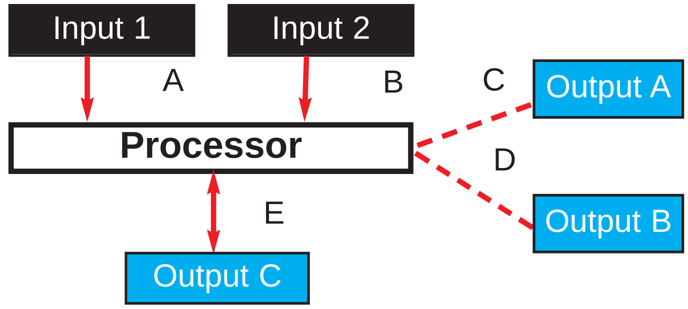

Figure 3

When system components are modified, interfacing can be a major effort because the interfaces may be old and the knowledge base is lost. The interface engineer must be able to get all of his information from schematic testing and analysis.

Types of Interfaces and Considerations -
The two basic types of interfaces are analog and digital. Each of the types can be bidirectional. Digital interfaces tend to be better defined and the protocol standards are available. In most cases, one must deal with the characteristics which were originally designed into the system in order to maintain compatibility. The older digital types of interfaces, which need sustainment engineering, have to be designed carefully especially if there is a mixing of technologies. The older types of logic, which may be in part of the old system, may not be compatible with all the logic families available today. Another consideration is protection of the interface circuits from transient voltages that are not generally defined, depending on which technology was used in the original design. Newer components may need increased protection. There are conditions in the interfaced equipment that are not always in the specifications, such as noise pickup and crosstalk. These problems get magnified by increased rise times and higher density interconnect connectors. Each of the basic types has its own set of considerations and the better the understanding of the equipment's requirements and technologies used, the better and smoother the effort will proceed.

The analog interface can be difficult because the original design may have utilized a component which is now an obsolete component, like an IC or transformer. Analog ICs are not usually a large problem. With the ability to use COTS (Commercial-Off-The-Shelf), there is usually a functional replacement available but with a different footprint. New PCBs may be required, which increases the size of the effort, but with the new drafting tools subsequent modifications make it an easier task. In the case of a discontinued transformer, where no suitable substitute is available in either pack-

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Help line (continued from page 4)

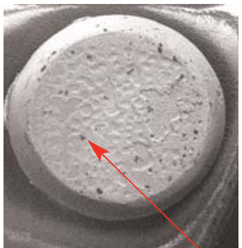

Figure 11- SEM analysis of base of lead from pristine component at 50X

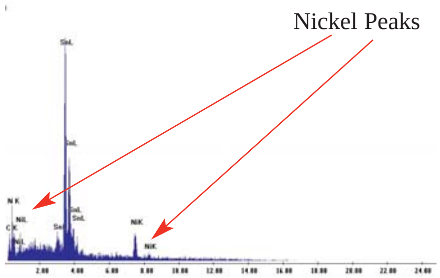

Figure 12 - EDS analysis of dark spot from Figure 11.

Dark Spot on Figure 11

Conclusions:

The components did not generate a measurable wetting force; they did not comply with J-STD-002 B quantitative solderability standards. Most leads tested exhibited de-wetting. The poor wetting or de-wetting is probably the result of the inconsistent surface plating. In some instances voids as in Figure 11 were observed allowing the underlying nickel surface prone to oxidation making the surface un-solder able.
The large voids observed at the pad of the dislodged component (Figures 7 & 8) are reminiscent of volatile gases trapped in the molten solder during re-flow and can be the result of excessive flux, improper re-flow profile, poor flux selection or poor solderability.

The poor wetting from the exposed nickel along with the voiding at the pad surface resulted in a mechanically weak solder joint.

Recommendations:

Confirmation of a uniform, proper plating thickness was recommended in addition to routine Wetting Balance analysis of incoming components. Pursuit of a second source of transformers was also recommended. Such qualification and consultation support would be available through ACI.

Sustainment Interfaces (continued from page 5)

aging or the electrical performance, the solution must be found by some other method. Opto-isolated analog circuits can provide high voltage isolation with a high accuracy and a high bandwidth. If the transformer provides a high impedance, a new circuit must be designed.

ACI's C6533A/ARC intercom had interesting interfacing challenges for which a suitable replacement output transformer with high secondary winding impedance was not available. The challenge was with the bidirectional analog signal. The interface requirement was further complicated because there are up to 6 other units on the system which also had to communicate over the same port, a 150 O resistor in the aircraft wiring.

The new circuit had to be designed to supply both isolation and high output impedance. The new ACI design used available COTS components. The circuit used a transformer for isolation and two transistors in a push pull configuration to provide the high output impedance. The circuit was designed and implemented and exceeded the system requirements.

Specifications May Not Tell All -
A system may have several different configurations. In Figure 3, output A and output B are connected to the same port but the voltage requirements may be different. The two units may not have been designed at the same time or one is a later addition for some special function.

The C6533A/ARC did not have detailed specifications. From the depot maintenance manual, the requirement was Vout must be 0.3 Vac to 0.46 Vac into a 150 O load. At first this condition was an easy specification to understand, just a gain stage with the proper output. When it was installed in another type of aircraft, the interface did not operate as it did in the first type of aircraft.

To summarize the problem, the second type of aircraft interfaced to a different box which on its input had two silicon diodes back-to-back. From inspection, the setup requirements of .4 Vac is insufficient forward bias for the diode. To fix this problem reverse engineering on the original equipment showed a 1KO in the output to the port. ACI's original design had a 27O resistor in place of the 1KO. The open circuit output voltage out of the amp was:

0.4 V to the input# 150 O is the 0.472 Volts AC

A 1Kohm resistor, in series with an amplifier output that is implementing a 0.4V AC across the resistor, creates an open circuit output of 3.067 Volts. This voltage will forward bias the diodes and the Intercom will operate both components of the system.

In summary, be sure you understand both sides of all of the unit's interfaces into the system. New components will not always behave the same as the old components they replace. Whenever possible, survey the site where the equipment is used.

This article is based on some of the issues which were solved by the ACI engineering staff. If there is a question related to this or other interfacing problems, please call the Helpline at 610-362-1320.

Tech Tips...

Design for Sustainability

Introduction:
With careful use of the principles of Design for Sustainability (DFS), a company can keep a product fully functional and fielded for a much longer time. The best time to extend a product's lifetime is at the very beginning, at the design stage. It is here that it is most beneficial because it is the place where changes have the least impact on the total production cost. This article will outline some of the more important considerations of DFS.

I. Systems Level Approach:
The systems level, or Top-Down, approach is ideal for implementation of DFS in that each step in the development process progresses down the design hierarchy. By utilizing the Top-Down approach, the system is first described by major function or system, as in a block diagram. Once each major function or system has been thoroughly defined, all of the sub-systems, which are required to handle all of the inputs and outputs that define that particular block of the system, can then be defined. The use of Commercial-Off-The-Shelf (COTS) components aids in this approach as the sub-systems have already been designed and manufactured, so the engineer only has to make the interconnects. This approach lends itself to the next consideration: Modularity.

II. Modularity:
The three main tenets of the modularity approach are: ease of manufacturability, ease of upgrade, and ease of repair. By making a product modular in design, only one particular portion of the system may need to be upgraded at any given time. This increases the sustainability by reducing the re-design cycle. Modularity reduces time and cost to repair an item as the Line Replaceable Unit (LRU) becomes a part of the whole unit, instead of the unit itself. The third advantage to modularity is the ease of manufacturability. This advantage lies in the fact that a product can be designed to have many options that the customer can choose from without having to make custom modifications. A base unit, which would only need to be designed once, could accommodate any number of device options. Each option can then be designed independently and if changes to that design are needed, only that particular module is affected. An example of such a unit would be a universal power supply. Universal power supplies are those power supplies that have an input voltage and frequency range. Some universal power supplies also have the ability to be configured with different outputs. This is an ideal situation as a company's product can be upgraded at any time and used anywhere in the world. Economically, it is more advantageous to use a modular approach for product development because the costs of sustainability are greatly reduced.

III. Standard Parts:
The use of exotic, custom parts is one of the main causes of the shortening of the lifetime of a product. This is due to the fact that these custom parts are typically only made for short periods of time and are then discontinued. Using more standard parts and components increases the sustainability of a product as they would be more readily available. Using parts that are second sourced is also a good way to increase sustainability because there are more suppliers that make that part.

IV. Standard Busses and Interfaces:
The use of industry standard busses and interfaces allows for the incorporation of COTS components into a company's product. This allows for greater sustainability as industry standard busses and interfaces have been around for many years, ex: RS-232, RS-485, MIL-STD-1553, VME, CPCI, etc.

V. Hardware vs. Software Implementation:
The critical consideration, whether to implement a function in hardware or software, plays an important part in sustainability. For complex calculations and the ability to easily change the desired output, software is more beneficial. However, the cost of maintaining a software based system is potentially higher than a hardware solution because the code needs to be supported and maintained. To minimize these costs, a company can use a top-down, modular approach to code generation. This allows changes to be made quickly, and due to the modularity, only partial compilation is necessary. In addition, writing code that is processor independent makes porting the code to a different processor simple. Also, good, clear documentation of the source code is essential for long term sustainability. For those systems that are less complex, a hardware solution may be the best choice. A hardware implemented function may require more cost up front in the selection of stable, low-drift components so that tuning needs to be done only once. With no code to maintain, the hardware solution can be designed in a modular fashion that will make changing the functionality easier and increase sustainability.

VI. Associated Costs:
The costs associated with DFS are often called Life-Cycle costs. These costs come in five different categories: design, production, maintenance, logistics, and disposal. The design costs are only a small fraction of the Life-Cycle costs. Once a product has been designed, it can be built in quantity. Then, that product needs to be supported by both maintenance and logistics. The logistics costs can be very high if there are a lot of components in the device. Each of these components needs to be ordered and stocked.

continued on page 8

Design for Sustainability (continued from page 7)

There are also disposal costs. These costs can be minimal for simple systems, or can be very expensive for more complex systems. Another critical aspect of costs is in which cycle a change occurs; the further along in the process, the more the cost. Therefore, it is critical to catch any problems as early in the process as is possible. The cost of a unit's sustainability is lowest when problems are discovered early. The best way to make sure that problems get taken care of early is the subject of the next consideration: Inter-Disciplinary Communications.

VII. Inter-Disciplinary Communications:
One of the most important aspects of DFS is inter-disciplinary communications. It does a company no good to design a great product if it can not be manufactured. For maximum sustainability, it is best that all departments communicate with each other and meet face-to-face during the critical design stages so that there will be no confusion as to what the critical issues are. A good method of increasing inter-disciplinary communications is the building of Product Development Teams. These teams have representatives from each of the departments who stay in constant contact and let the rest of the team know of issues as soon as they arise.

Example:
An example of a system that has been designed for sustainability is LINK-16 (see figure 1). This is a military communications system that utilizes many different modes: Ground-Air, Air-Air, Air-Sea, etc. The main reason that the LINK-16 system is highly sustainable is that it is modular in nature, and was designed with that in mind.

Link 16 is designed to work with existing Army, Navy, and Air Force communications systems as well as to incorporate new systems. As each of the Armed Forces evolves, its communications needs will most assuredly change as well. If a branch of the Armed Forces wants to deploy a new communications system, it can do so by designing a new module for the LINK-16 system as well as re-fielding its existing systems to lower echelon elements, thus extending the sustainability of the overall system far into the future.

When a company exercises good DFS principles, it can be assured that its products will be sustained long into the future. If you have any questions, or would like advice on implementing Design for Sustainability practices, please call the EMPF Helpline at 610-362-1290

Manufacturer's Corner - Metcal

At the EMPF, our staff conducts various demonstrations on SMT equipment daily. One of our busiest sections in the demonstration factory is the Ball Grid Array (BGA) rework area. The EMPF engineers and the training department utilize this equipment to conduct extensive research on new solder pastes, fluxes and epoxies and the training of OEM and CEM technicians in the use and repair of BGA, Chip Scale Packaging (CSP), Land Grid Arrays (LGA's) and Leadless Lead Frame packages (LLP's).

It is commonplace for practioners to speak of smaller, faster, cheaper, better. Each is a given in today's electronics manufacturing environment. If anything, the current downturn has accelerated miniaturization and further pushed everyone into deep cost reductions. Doing more with less is no longer a goal to be achieved someday - it is a necessity to be accomplished now…or if truth be told, yesterday.

Given these undeniable industry drivers, it is not difficult to see that the equipment and processes that electronics manufacturers use must evolve to meet the above critical drivers. Part of the evolution will include more functional, smaller profile and smaller footprint components such as LGAs, LLPs and CSPs. In mobile phones, PDAs and digital cameras, are the packages of choice - not only for their size and functionality, but also for their low manufacturing cost.

In particular, CSPs have the speed, density and manufacturability that OEMs and CEMs require. Moreover, since they can be placed using today's standard SMT processes and machinery, CSPs allow designers and manufacturers to do more with less.

Rework Just Won't Go Away

Electronics manufacturing is more automated than ever; placement machines, ovens, dispensers, etc., can all work at breakneck speeds. Logically, it would seem that the need for rework should decline, but it has not. In fact, just the opposite is true. Higher density assemblies with more solder joints and smaller packages inevitably lead to increased levels of rework. More solder joints mean more chances for defects - and more, not less rework.

The face of rework itself has changed. Once the "hidden secret" of CEMs and OEMs, and long considered a profit-draining process, successfully reworking an expensive assembly (thus saving both production time and materials) is often a critical key to long- and short-term profitability. In this arena, CSPs excel. Unlike flip chips, many CSPs do not require underfill. If they have a flexible layer between the solder ball and the die, no underfill is needed. In this case, they can be more "easily" reworked - given the proper equipment and good operator training.

In theory, rework is rework - be it basic SMT components, advanced packages or 0201s. No matter, the steps are similar. The keys to effective CSP rework, however, can be found not in the similarities, but in the differences that can make or break successful rework, and in the essential tools needed to get the job done quickly and efficiently.

The Basic Steps Required

The basic steps to the removal and replacement of CSPs are straightforward enough:

1. Establish thermal profile
2. Remove failed component
3. Clean and prepare site
4. Replace component with flux or solder paste
5. Reflow
6. Inspect

Convection is the heating method most used. This allows for tight process control, that is essential in establishing a good, repeatable thermal profile and won't over heat the component, or hold it for too long above reflow.

Establishing the correct, ideal profile takes experience and patience, although the basic requirements for any profile are well understood.

Standard reflow

This process is particularly critical when working with lead-free assemblies. The higher temperatures needed for lead-free (up to 225°C), coupled with the thermal sensitivity of CSPs, can be problematic without the ability to ramp temperatures at a rate that will not harm packages. The latest technology rework systems are more likely to employ four heating zones and one cooling zone. Most solder systems work with a more traditional three-zone model and no system for cooling down. The addition of a controllable preheater to a rework system helps meet future process demands, including lead-free. Efficient, controlled pre-heating avoids the thermal damage risked when working expensive but sensitive packages unsuitable for heating above 240°C with quick reflow times.

Zone	Time Duration	Target
Pre heat	100	130-to-140
Soak	90	140-to-170
Ramp	100	170-to-225
Reflow	15-to-30	225-to-235

Some lead-free reflow profiles are as small as 15 seconds above specified reflow temperature.

Typical lead-free profile is shown with peak temperatures around 223°C to 235°C and times as low as 15 seconds in the reflow zone. This means excellent temperature controls and profile controls are essential.

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To help protect packages from the increased heat required for lead-free processes, independent top and bottom heater control is essential. In short, as lead-free alloys become mainstream, greater care must be taken to develop a thermal profile that can reflow the new alloys without damaging CSP/BGA/LLP packages.

Zone	Time Duration	Target Temp
Pre heat	60-90	100-120
Soak	60-90	155-175
Reflow	30-60	200-220

Through closed-loop, time, temperature and airflow parameters, contemporary rework systems can help operators adapt to lead-free. In addition, and just as important, enhanced process control features guarantee repeatability, which is critical for companies with multiple locations in various parts of the world. In many cases, different voltages and frequencies can affect machine performance.

On any reflow soldering system that heats both sides of a PCB assembly, the required solder joint temperature is a function of how much heat is applied to both sides. While it is possible to reach a specific solder joint temperature with a number of heat settings, the incorrect combination can lead to low yields and, in some cases, catastrophic results, including warping due to excess heat on the top side. This often causes bridges in the corners of BGA and CSP packages.

It is here that an experienced operator using equipment that allows for precise process control can play a paramount role in successful rework. Even the occurrence of minimal warpage, for example, a BGA lifted by just 0.1mm (0.005") across the device, is enough to cause an open circuit. If the board/component survives this process with no apparent defect, the joint will be constantly under strain as the board returns to its normal shape, causing long term reliability problems.

Eliminating warpage generally involves creating a better balance between the bottom and top side of pre-heat temperatures. This is best achieved with full convection, as in the assembly line reflow ovens.

Convection and Airflow

Convection systems employ either high or low airflow. In CSP rework, for instance, low airflow systems are preferred. As already stated, CSPs are normally found on high density PCBs. Space is at a premium and adjacent components can be easily reflowed and moved out of place during the rework process. High airflow systems increase the changes of moving adjacent - ruining alignment and creating more rework. Low airflow systems reduce the chance of shifting components, provided airflow levels are below 15 l/min and they feature a low velocity reflow nozzle design.

Once reflow is accomplished, component removal is generally accomplished with a vacuum pick-up. Care must be taken as excessive vacuum pressure can cause the solder to collapse and adhere to the PCB, making clean up slower and more difficult.

Cleaning

Once the component has been removed and pad integrity has been checked, the site is prepared for component reattachment.

Removing residual solder using a soldering braid is the preferred method, as a braid allows the operator to achieve flat pads (which are preferred when solder paste is to be applied for reattach). This process must be carried out in the case of Leadless Lead Frame Packages.

If dome-shaped pads are preferred, then only flux will be applied, and a wave solder tip is best for site cleaning. Of course, this process can only be used when pad geometry is uniform. Otherwise, solder joint heights will differ. When applicable, the method is a reliable and less damaging way to remove residual solder. Special solder tips called 'hoof tips' are available for this purpose.

In either case, to prevent thermal damage, and to speed the cleaning process by eliminating the need for constant setting and resetting of heating parameters, many rework facilities are moving away from "traditional" soldering irons in favor of tools that automatically control tip temperature.

In general, any tool that increases process control, thus reducing operator variability and allowing for "copy-exact" rework from facility to facility, is preferred. As the industry itself moves into China and other remote manufacturing sites, the need for transparent tools, those that can take the guesswork out of rework, will increase dramatically.

Material Deposition - A New Approach

When working with array packages, either flux (dip transfer method) or paste can be used for reattach. The device type and/or solderball composition will determine whether solder paste or flux is used. In either case, operators must pay close attention to material deposition. How accurately the solder or flux is deposited will directly affect the yield and size of a joint. With a conventional SMT component, a defect in the rework can be easily rectified by retouching. With array packages, however, a single failed solder joint would necessitate starting the entire rework process from scratch.

Stencils can be used to apply solder paste to the PCB itself. This process can be difficut and significantly reduces the yield. This traditional method of paste deposition creates problems, as stencil flatness and position are troublesome, and there are concerns about access due to the close proximity of the adjacent components.

Printing onto a PCB, when fully populated, is difficult due to size and packaging density around the devices. To alleviate this problem, a method of printing on the package has been developed. This solution prints the standard thickness of paste used in assembly, but onto the package. If this method

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is followed, this will control the solder volume for replacement in the rework process.

Printing directly onto the component is a relatively easy process. A specially designed plate is used to apply solder paste to the component with the same size and shape as originally done on an inline screen printer. The goal is to place approximately the same volume of paste as was originally deposited by an inline printer during the original manufacturing process.

The direct deposition process involves printing solder paste onto the component before it is picked up by the placement head. Not only is this new process simple, it is also quick to perform and can increase productivity up to four to five times in place of stenciling the PCB substrate. This is an ideal process for small components and situations where traditional stencil access is limited by the close proximity of adjacent components.

When working with LGAs, the component body outline is used to register the component to the stencil. Direct printing onto the component is especially useful with LGAs with different pad dimensions on the same component, as it allows operators to print different amounts of solder at a uniform height across the bottom of the device. It should be noted that on these devices flux and drag-solder pad cleaning methods cannot be used.

For packages with solderballs, the balls themselves can be used to align the stencil. With LGAs, however, there are no balls on which to locate. In these cases, the stencil is made to help locate the component body by registering on the edge of the component itself.

Replacing the Component
A split-optics vision system is necessary to help operators achieve higher process yields and better quality. The component is aligned, placed with the vacuum pick-up tube and reflowed with hot air or gas. The thermal profile developed for removing the component is again employed so that the new device is not damaged during reattach. Adjusting the profile, however, may be necessary depending upon the type of flux or paste being used.

Automated placement features and better vision systems on newer rework systems help operators improve accuracy. X- and Y-axis control are standard and necessary - better machines incorporate Z-axis motorized control to help place components at the exact height required, without crushing the paste. Accuracies to 0.025mm (0.001") are ideal for precise, repeatable CSP placement and LLP placement.

Inspection
With leaded components, it is a simple matter to look for good solder joints and the absence of shorts, using a low magnification inspection system.

With CSPs and other array packages, inspecting the integrity of solderballs (size, positioning, bump geometry, etc.) requires either X-ray systems and/or optical inspection systems to see underneath the components.

X-ray inspection can highlight certain faults, such as voids, shorts, and bridging; however, equally serious problems like component opens or joint cracking and partially soldered joints are not easily found. Additionally, there are some things that X-ray can not detect such as, process-related problems like unsoldered joints, flux contamination and grainy joints.

To detect these faults, optical inspection systems using an endoscopic-type mechanism are preferred. With advances in optics and improved software, latest technology optical inspection systems can catch 90% of errors - often eliminating the need for expensive and time-consuming X-ray. For those already using X-ray, an optical inspection system can be employed as an additional tool -- as the first line of inspection, before assemblies are sent to X-ray.

There are a few requirements for effective optical inspection. Given today's high package densities, any inspection system must be able to maneuver between component spaces as tight as 1.1mm (.043”). Some endoscopic systems can perform in these tight spaces, others cannot. For complete optical inspection, systems need to be able to "see" under array packages with low standoff heights, down to 0.05mm (0.002") for micro-SMD as an example.

A final caveat: underneath the typical BGA or CSP there resides a large number of solder joints and 100% inspection may not be practical or cost effective. Both optical inspection and X-ray methods are, however, essential tools in good process development.

Conclusion
CSPs, LLPs and other array packages continue to gain in popularity as devices get smaller, cheaper and more complex. In spite of automation, rework remains an integral part of successful electronics manufacturing. Reworking array packages, in particular CSPs, is challenging - particularly in light of industry trends that include higher board densities, far-flung manufacturing sites, the need for repeatable process control and lower paid wage workers who ultimately perform the rework process.

Reworking CSPs is, in many ways, not very different from standard SMT devices. Effective rework demands adapting existing processes to the realities of hidden solder joints and temperature sensitive components. Equipment must evolve as well. Better vision, more accurate temperature profiling, more accurate placement and process repeatability must become standard in every rework system. It's not "if" we will need to consider these new packages, it is "when."

At EMPF, the Metcal BGA Rework station is used to assist in the repair of commercial and military PCB assemblies and in instructional classes such as SMT and BGA rework classes. If you would like to see a demonstration, please call Jeff Stong at the EMPF at 610-362-1200.

American Competitiveness Institute - 2004 Course Schedule

Skills

2003 CLASSES

BGA Manufacturing, Inspection & Rework
December 1-2

2004 CLASSES

SMT Manufacturing
February 23-27

BGA Manufacturing, Inspection & Rework
January 26-27

Chip Scale Manufacturing
January 21-23

Electronics Manufacturing

2004 CLASSES

BOOT CAMP A - Week 1
February 2-6

BOOT CAMP B - Week 2
February 9-13

Certifications

IPC-J-STD-001 Instructor Recertification
December 8-9

IPC-A-610 Instructor Recertification
December 11-12

IPC Challenge
December 10

2004 CLASSES

IPC J-STD-001 Instructor Certification
January 5-9
March 1-5

J-STD-001 Instructor Recertification
January 26-27
March 22-23

IPC-A-610 Instructor Certification
January 12-16
March 8-12

IPC-A-610 Instructor Recertification
January 29-30
March 25-26

IPC-7711/7721 Rework, Repair and Modification of Printed Boards and Electronic Assemblies (Operator)
March 15-26

IPC Challenge
January 28
March 24

WHMA-A-620 Wire Harness Manufacturing (Operator)
January 21-23

Continuing Professional Advancement in Electronics Manufacturing

2004 CLASSES

Lead Free Manufacturing
January 15-16
March 8-9

Design for Manufacturability
February 19-20

Failure Analysis and Reliability Testing
March 15-17

Characteristic Properties of Materials
March 29-31

IPC member

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

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