empfasis

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The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

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Wide Band Gap Technology for Navy Applications

Utilization of silicon carbide (SiC) material for the fabrication of electronic components represents revolutionary technology because it allows significantly higher performance and durability while demanding less power, weight and space. SiC semiconductor devices hold promise for major breakthroughs in performance and capability.

Wide band-gap (WBG) materials such as SiC and Gallium Nitride (GaN) offer the necessary materials properties to address performance challenges. SiC and GaN show promise in operating from VHF through X Band frequencies while providing higher breakdown voltage, better thermal conductivity, and wider transmit bandwidths than legacy silicon (Si) and gallium arsenide (GaAs) power devices. WBG semiconductor materials provide breakthrough technology in the development of high power and high frequency semiconductor devices. Benefits include device and system miniaturization providing savings in size and weight, improved performance, and increased durability and temperature operability ranges.

Multifunctional Information Distribution System (MIDS) for LINK-16 - a future insertion for WBG materials

Newer military electromagnetic systems will require active aperture antenna arrays with a linear amplifier behind each antenna element. SiC and GaN amplifiers are expected to become the amplifier of choice for many of these applications. WBG material promises big improvements in the performance of ultra-wide bandwidth communications and radar systems. Power delivery of WBG devices at microwave frequencies can be ten times greater than the Si and GaAs semiconductors used in cellular telephones, military radar systems, and satellite transmitters. To a designer of radio communications, electronic warfare and radar, these improvements will enable the design and implementation of smaller, more efficient microwave transmitters with simplified cooling requirements. These are all enhancements that cannot be performed with current vacuum tube technology.

New emerging communications systems require higher performance and more functionality in smaller enclosure volumes. Multi-mode military transmitters in the VHF (30-300 MHz) through S-Band (2-4 GHz) frequency regimes are being proposed to meet these tactical system demands, while strategic military communications systems range from 7-44 GHz and beyond. Radar traditionally requires very high pulse powers in the microwave bands from UHF to X-band (8-12 GHz) and beyond, and includes a wide variety of ground, air, ship, and mobile platform installations. To provide this performance, power amplifiers must be more efficient, provide higher power densities, cover wider transmit bandwidths, and operate reliably in more harsh thermal environments. They must also contribute to savings in size, weight, and life cycle cost.

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Environmental Testing at the EMPF

As part of a printed circuit board (PCB) design and manufacturing cycle, environmental stress screening (ESS) should be used to verify that the product will survive the expected environmental conditions. Environmental stress can be in the form of temperature (outdoor environments, high power applications), mechanical shock and vibration (transportation of the product, automotive applications, aerospace applications), exposure to humid environments (refrigeration atmospheres, marine atmospheres) or simply high temperatures (desert environments). Once the design is complete, and the PCB is known to be manufacturable (presumably after design for manufacturability steps have been taken), reliability verification in the form of ESS is usually pursued. The goal of ESS testing is to identify latent defects (such as manufacturing defects, component defects, material compatibility problems, or defective solder joints) and take corrective action before a product is shipped. This article describes some of the most common ESS methods used in a manufacturing environment.

Common ESS test methods are usually grouped according to the particular environmental stress to which the PCB will be exposed. Temperature tests include thermal cycling and thermal shock, the difference being the speed at which different temperature extremes are attained. Typical thermal cycling changes the chamber temperature between 4°C and 10°C per minute. For example, if the temperature is ramped between 0°C and 100°C at 5°C per minute, it would take 20 minutes. Thermal shock changes the temperature of a board much more quickly - from 10 seconds to one minute. This causes much more stress on a board, and often will produce different failure mechanisms than thermal cycling. Both methods often have a "hold" or "soak" step as part of the method. Common duration at each extreme temperature is 10 or 15 minutes.

Mechanical test methods include vibration (sine wave or random) and drop testing. Typically, a test board or finished assembly is placed on a vibration table, and the table is shaken in an electro dynamic shaker at certain frequencies and amplitudes. The test is usually repeated at each axis (x, y, and z). This can be a very important test for PCBs that must undergo aerospace applications such as a space launch or on a high performance aircraft. Usually the final product will have a vibration profile to which the PCBs must be tested. Other vibration profiles are also available (see Table 1).

Tests that use humidity can also greatly stress components and finished assemblies. A heat/humidity chamber is needed to perform this type of testing. The PCB is held at a predetermined temperature and humidity level. Common conditions are 85°C and 85 percent relative humidity. Various test methods are available (see Table 1), or the conditions of the final assembly can be programmed into the test chamber.

The heat/humidity aging can take a long time to complete. For example, the IPC-TM-650 2.6.3.4 test method listed in Table 1 takes 120 days. What can be done if there is not enough time to complete such a test? Fortunately, there is another heat/humidity method, the highly accelerated stress test (HAST). The HAST chamber allows high humidity levels at high temperature (typically over 120°C). This is combined with high pressure (up to two atmospheres). This allows a heat/humidity test to be completed in much shorter time (less than one week) than the weeks or months associated with heat/humidity testing at atmospheric pressure. HAST is also used to determine if the seal of a moisture sensitive device is working properly, as the conditions inside the chamber cause materials to absorb moisture at a very high rate.

Many PCBs intended for outdoor use will come in contact with a salt environment. This can be from a marine environment or from salt put down on roadways. Salt fog is a test method that exposes a PCB to a fine mist of salt spray. Common conditions are one week in a salt fog chamber held 35°C using a five percent sodium chloride (NaCl) solution.

Many of the methods described in this article are conducive to monitoring the PCB solder joints in situ, or while the test is in progress. A test board can be wired in a daisy chain fashion, and the resistance monitored with time. This allows the identification of failures as they happen. The failure can then be identified, a replacement component added if necessary, and the ESS test can continue.

The EMPF is currently assisting a customer using many of the methods described. The customer is qualifying a manufacturing process for a final product. Boards are being put through a thermal cycling (-40°C to +85°C at 5°C per minute), thermal shock (-65°C to +125°C, 100 cycles), and 120-day heat humidity test (85°C, 95 percent relative humidity). Additionally, the conformal coating adhesion is being measured before and after each test, to evaluate the ability of the coating to withstand each test method. The goal of the project is to validate that the manufacturing process produces a reliable final assembly.

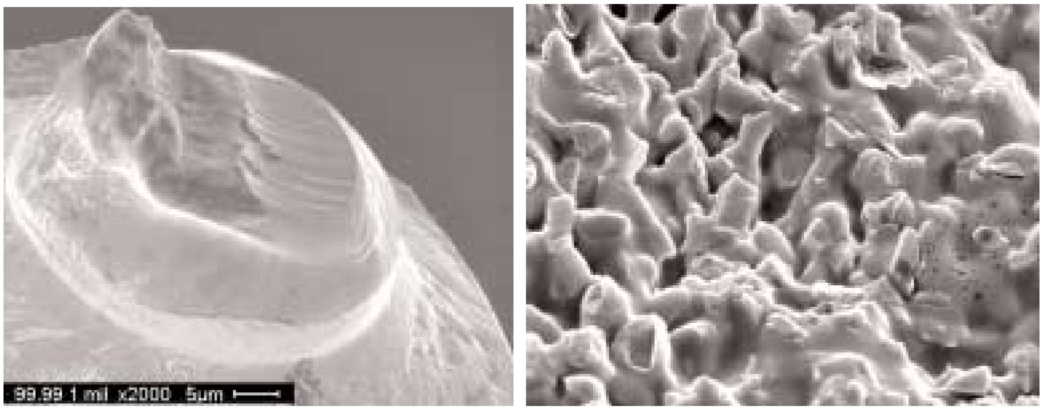
For more information on environmental testing, please contact the EMPF Helpline at (610) 362-1320.

Table 1 - Common ESS Test Methods

Environmental Stress	Test method
Thermal Cycling	JESD22-A104-B
	IPC-TM-650 2.6.6B
Thermal Shock	JESD22-A106-A
	IPC-TM-650 2.6.7A
Vibration/Mechanical Shock	JESD22-B103-A
	JESD22-B104-A
Heat/Humidity	JESD22-A101-B
	IPC-TM-650 2.6.2
	IPC-TM-650 2.6.3.4
HAST	JESD22-A106-A
	IPC-TM-650 2.6.16.1
Salt Fog	JESD22-A107-A

The Use of SEM in Failure Analysis

The Scanning Electron Microscope (SEM) is widely viewed as the most useful tool for failure analysis, process development, and quality control for all levels of electronics manufacturing. The ease of sample preparation, high magnification capabilities (over 100,000x), and wealth of data obtained are the main reasons that a SEM is a standard piece of equipment in analytical laboratories. When coupled with energy dispersive X-ray spectroscopy (EDS or EDX), the SEM's capability is further enhanced producing elemental information crucial to most investigations. The capability for scanning electron microscopes to image solder joints, component and board plating, integrated circuits, PWB features, and metallizations has been key in the development of improved components, materials and processes.



Secondary electron SEM image of the fracture surface of a gold stud bump at 2000X (left). The depth of field created by electron imaging is superior to optical microscopy. High resolution image of silicon carbide grinding surface (right)

Secondary Electron Imaging (SEI)

The incident electron beam that interacts with the sample produces a secondary electron from the sample surface. This is an outer shell electron used to image the topography of the sample surface. These electrons emanate from approximately the top 10nm of the surface. The secondary electrons are collected in a biased detector and produce high magnification images with excellent depth of field that cannot be paralleled by an optical microscope. The depth of field obtained using SEM is extremely helpful with the investigation of fracture surfaces. Secondary imaging can also be used for such common failure mode identification tasks as dimensioning traces, verifying the geometry of solder bumps and wire bonds, identifying fatigue cracks, determining breaks in metallization layers, and identifying component die level defects.

Backscatter Electron Imaging (BSI)

The same incident beam will produce electrons that are elastically bounced back from the electron shells near the nuclei of atoms on the surface. These electrons are termed backscatter electrons. Because these electrons are high energy, these electrons come from deep beneath the sample surface and require a different detector than what is

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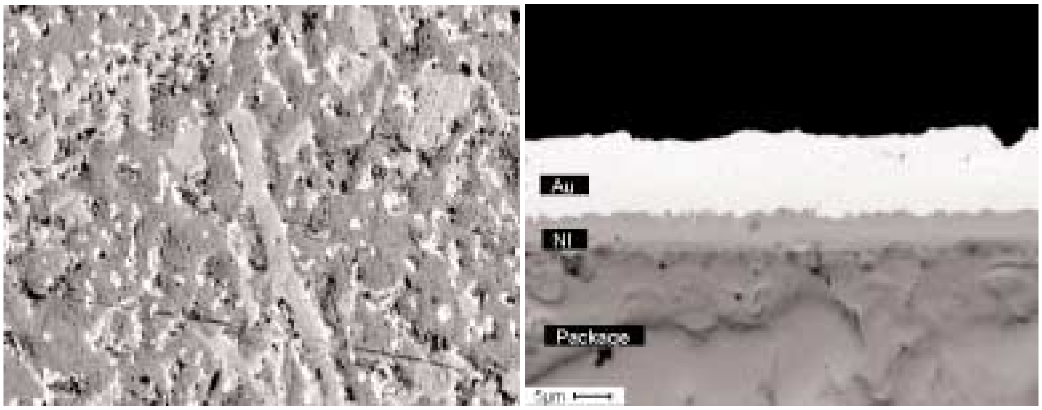
Depth of focus is the major separator between the SEM and optical microscopes often found on workbenches and in laboratories. The SEM uses electrons, which have a smaller wavelength, instead of light, to image a sample. The electron beam from a typical SEM is generated from a filament composed of tungsten or lanthanum hexaboride (LaB6). These filaments are heated to generate electrons that are accelerated towards the sample. The interaction between the electron beam and the sample produces a plethora of information about the surface of that sample.



Backscatter SEM image of a gold enbrittled solder joint (left). The dark areas are tin, the medium dark areas are gold-tin intermetallic and the bright areas are lead. Cross-section of a gold-nickel pad (right) showing defined contrast between the gold plating and the nickel pad.

The Use of SEM in Failure Analysis

(continued from page 3)

Common Electronics Manufacturing Failures and Defects that the SEM can detect include:

- Pb migration and grain coarsening
- Dendrite formation
- Gold enbrittlement
- Stress fractures
- Metallization damage from electrical over stress (EOS)
- Wire bond fractures
- Intermetallic growth
- Surface contamination
- Electromigration
- Dewetting
- Insufficient intermetallic formation
- Poor plating and plating layer failure
- Surface finish defects
- Interconnect separation
- Oxide breakdown
- Substrate "popcorning" and epoxy delamination
- Whisker growth
- Voiding and porosity

used for secondary electron imaging. One of the main advantages of using backscatter electron imaging is the elemental contrast produced when the beam interacts with the elements. This contrast is created by the number of electrons backscattered to the detector, which is a function of the atomic number of the element. Because of this, elements with a higher atomic number, like lead (Pb) appear brighter than elements with a lower atomic number like tin (Sn). This elemental contrast is useful when investigating solder microstructure, intermetallic growth, trace damage, plating dimensions, contamination, voiding and solder coverage.

Energy-Dispersive X-ray Spectroscopy (EDS)

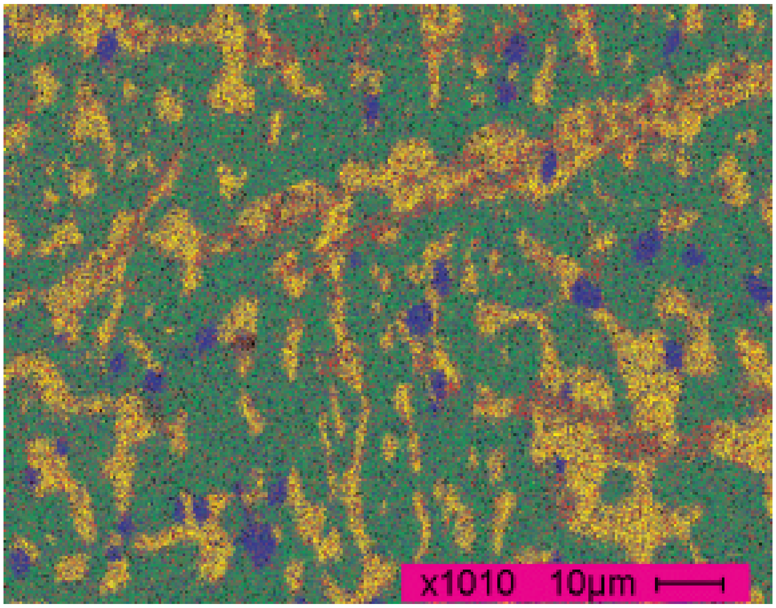
One of the most important interactions between the incident beam and the sample is the excitation of characteristic X-rays. These characteristic X-rays are used to identify the elements present in the sample. Each X-ray carries energy that is a function of the electron make-up of the atom. A silicon-lithium (Si-Li) detector collects X-rays that produce spectra used to qualify and quantify elemental composition. Characteristic X-rays can also be imaged. This X-ray image, commonly referred to as a dot-map, records the location of the emitted X-rays producing a representation that identifies the location of each element. X-ray maps are one of the most functional of all images produced by SEM. The EDS detector is usually a separate unit and may not be available for all electron microscopes.

There are many other imaging and data collection techniques that can be accomplished using SEM including wavelength dispersive X-ray spectroscopy (WDX or WDS), voltage contrast, and electron induced beam current (EBIC). These techniques however, are not as common and often require modifications to existing SEMs.

Samples that are to be investigated using the SEM must be conductive, otherwise an accumulation of electrons on the samples surface (charging) distorts the image produced. Most non-conductive samples can be coated to produce conductive surface with little to no degradation of sample resolution. Coatings of platinum, gold, palladium, or carbon are often applied with thickness in the nm range and become virtually transparent when the sample is viewed under the SEM.

While the SEM can be used for low magnification imaging, the most common magnification used for SEM failure analysis investigations falls between 100 to 100,000x. This wide range allows SEM users to investigate both macro and microscopic areas.

For more information on the use of SEM in failure analysis, please call the EMPF Helpline at (610) 362-1320.

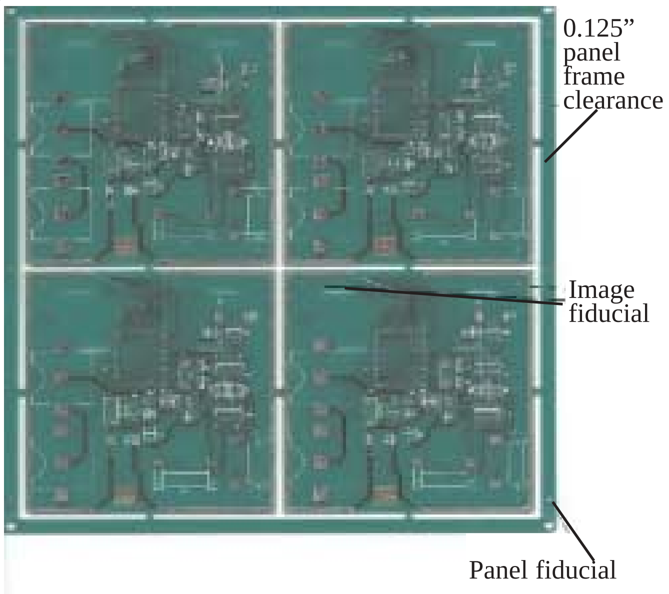


Elemental x-ray image of the microstructure of a tin-lead-silver solder joint. The location of silver emitted x-rays are shown in blue, lead emitted x-rays in yellow, and tin emitted x-rays in green.

Design Guidelines for SMT Manufacturing - Part II

In the first section of this article presented in last month's *empfasis*, we ended with a discussion of the impact that proper land design and via design plays on the manufacturability of SMT assemblies. In this issue we will continue to examine PCB fabrication issues relative to panelization, board size and fiducial design and location. We will also discuss issues that drive the selection process for components used on a particular design and how these issues such as machine limitations, vision recognition, component packaging, population density and component availability all play a role in determining the manufacturability of the SMT assembly.

The cost associated with the setup of a manufacturing process is usually fixed for a given design. The time required to develop equipment programming and fixturing will be the same whether we are building ten pieces or ten thousand pieces. How efficiently the assemblies are processed is what determines manufacturability. Let us examine some PCB fabrication issues that will have a direct impact on manufacturability.



Multiple image array panelization enhances process throughput

Most PWB fabricators have minimum and maximum substrate size limitations. In most cases the minimum PWB/panel size is 60mm x 100mm and the maximum PWB/panel size is 600mm x 685mm. Standard PWB thickness range from 0.40mm to 6.0mm. Panelization of the PCB substrates will go a long way in increasing process throughput. When determining the quantity of individual PWB's that constitute a panel array, the designer needs to understand the requirements of the PCB fabricator and the limitations of the automated processing equipment. All etched PWB features should be a minimum of 0.125 inches from the substrate edge. Orientation of the individual substrates within the panel array will also help to increase manufacturability. Most automated component pick and place equipment incorporates specific software features for the handling of panelized arrays. Keeping all of the substrates within a panel oriented in the same direction will greatly reduce the initial programming requirements of the processing equipment and also allow for faster throughput. This is particularly true of component pick and place equipment and Automated Optical Inspection (AOI) equipment.

Most assembly processing equipment utilizes a vision recognition system for alignment and registration. Providing fiducial marks on the panel array, the individual images within the panel and at fine pitch component locations is a great aid to the processing equipment used throughout the manufacturing process. The shape and location of fiducial marks is critical to the process success. The most common fiducial shaped used is a 0.050 inch diameter etched circle with a 0.100 inch solder mask relief. A minimum of two fiducial marks are required for registration and should be located near opposite corners of the PWB, no closed than 0.125 inches from the PWB edge.

Proper component selection has great impact on the manufacturability of a PWB assembly. Although functionality drives the component selection process, the types of component packages chosen, orientation and population density affect the overall efficiency at which an assembly can be manufactured. Minimize as much as possible the quantity of different component types and values. This will reduce programming and setup times for automated component placement equipment as well as reduce the amount of different component feeders required, reduce the potential of placement mistakes and also reduce the costs associated with material handling.

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Design Guidelines for SMT Manufacturing - Part II

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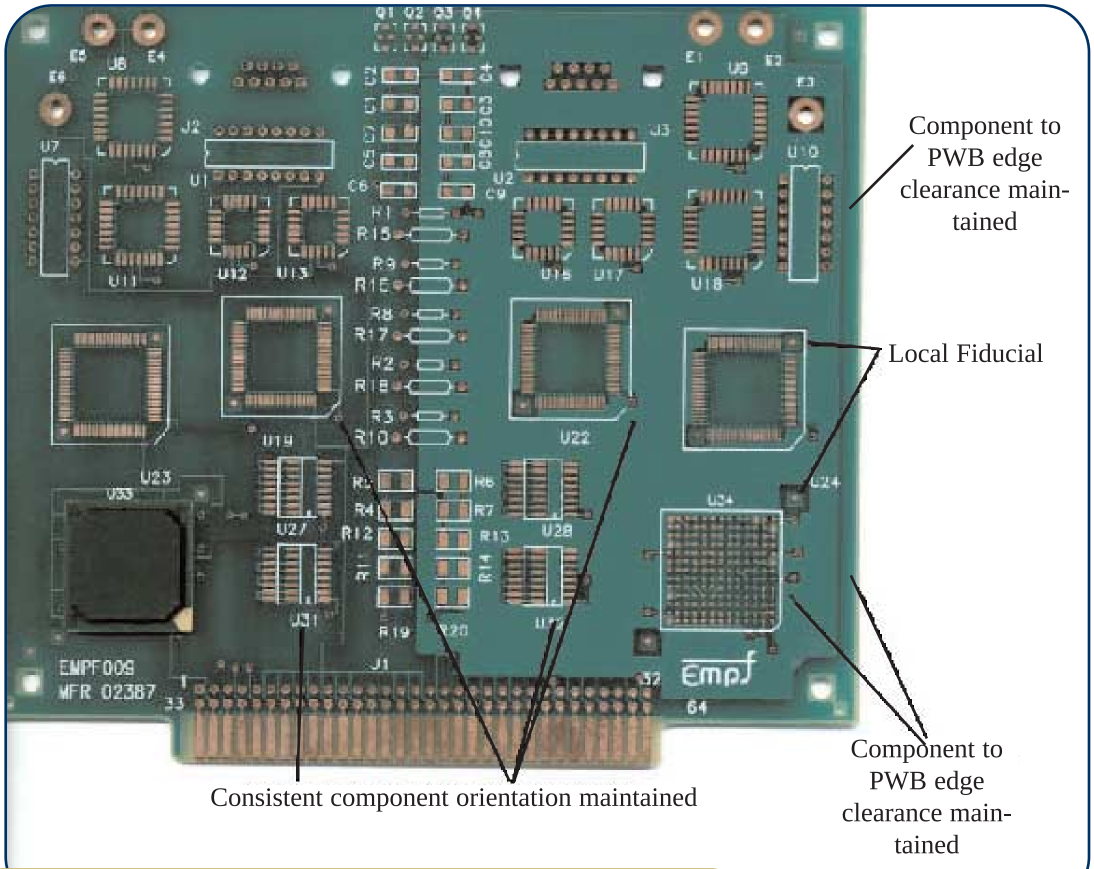


Properly designed PWB's aid the manufacturing process

Whenever possible avoid the use of cylindrical bodied components such as Metalized Electrode Leadless Frames (MELFs). These types of components historically are difficult for automated equipment to handle and can yield less than desirable solder connections as defined by accepted industry standards. Similar components should be orientated in the same direction wherever possible and component spacing should be adequate to meet the clearance requirements of all assembly and rework equipment. Avoid the use of odd shaped components, which may require special tooling for handling. Select component packages that are compatible with your processing equipment. Choosing the types of component packages and delivery media that is most compatible with your assembly equipment enhances the overall efficiency of the assembly process. PWB silkscreen markings aid in both the assembly and inspection stages of production. Wherever possible reference designators and polarity indicators should be clearly defined and visible after insertion of the component. Avoid using heat sensitive components that may not withstand the high temperature of the reflow process and also avoid components that require additional processing steps such as epoxy bonding and underfilling.

The use of chip on board (COB) components allows the design engineer increased versatility in the utilization of available PWB real estate, however the cost associated with the additional processing steps required such as wire bonding and underfilling may be prohibitive. The use of area array components such as BGA's, Micro BGA's and flip chips are a viable alternative to standard component packages because of the high density I/O and relatively small footprint. When designing assemblies using these array packages, proper land and via design plays an increased role in production yields. The incorporation of thermal relief vias and properly design solder mask patterns are integral to successful implementation of these types of component packages.

It is clearly understood that knowing the requirements and limitations of the processing equipment involved directs many aspects of the design stage. Allowance for these limitations during the design stage not only increases product yield in terms of performance but will also enhance production throughput and time to market as well.

In the next and final section of this article, we will focus on the selection of process materials and how they impact the manufacturability of the assembly. Choices such as substrate material, use of embedded components, PWB finishes, stencil design and process chemistries will be examined to determine their impact on the overall manufacturing process.

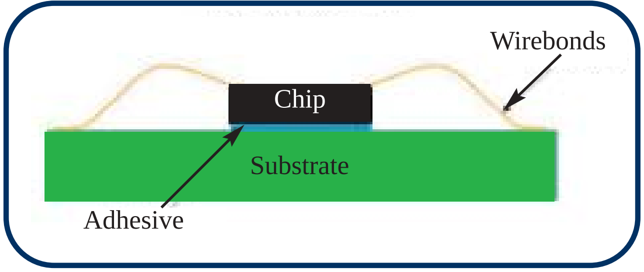
Electronics Manufacturing Productivity Facility

TECH TIPS...

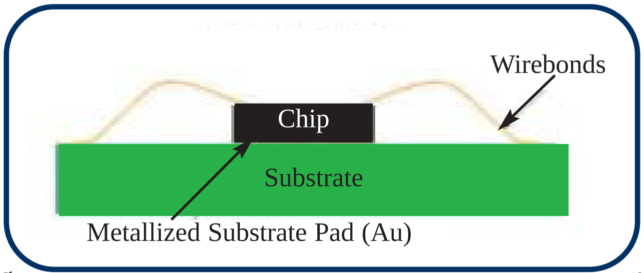
Die Bonding

Die bonding is one of the most important process steps in making direct chip attach (DCA) electronic assemblies. DCA, which includes chip-on-board (COB) and flip-chip techniques, allows designers the ability to keep pace with today's market that continues to push electronic devices smaller and smaller. DCA components typically have a smaller footprint than typical packaged devices including quad flat packs (QFPs) and ball grid arrays (BGAs).

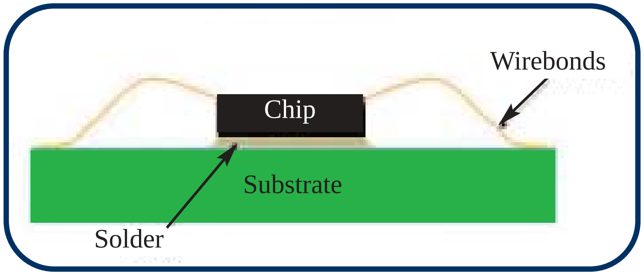
The common bonding processes for DCA components include epoxy, eutectic and solder.



Adhesive Die Attach



Eutectic Die Attach



Solder Die Attach

Epoxy used for die bonding is filled with a conductive material, silver is commonly used, allowing electrical signals to pass from the chip to the board and vice versa. Epoxy is dispensed onto the bond pad either in a pattern or as a line or dot. The chip is then precisely placed onto the pad and the epoxy is then cured. Curing is usually accomplished by placing the assembly into an oven for a designated time to speed the curing process. The advantages of using epoxy are that it is significantly less expensive than the other processes. The temperatures used are also lower than other attach methods. Problems that can occur due to the use of epoxy for die attach include voiding and poor electrical and thermal conductivity when compared to eutectic and solder die attach methods.

A eutectic die bond is made with the absence of a separate adhesive. Typically the substrate is metallized with gold and heated. The die (silicon) is then scrubbed against the substrate to form a eutectic (Au97-Si3) bond. A forming gas atmosphere is often employed to prevent oxidation. Eutectic gold-tin (Au80-Sn20) is also used in to the eutectic die bond method, where both the substrate and the die have the same eutectic metallization. The bonding method is exactly the same for either of the materials used. Some of the advantages associated with eutectic die bonding include good thermal conductivity and fatigue resistance. The drawbacks for this method are that the process temperature is quite high and the die may need a backside metallization for bonding to occur.

A solder die attach uses a solder material in addition to the substrate and die. The solder can be applied as a preform or paste. The assembly is profiled to determine the correct ramp rate (heating and cooling) and dwell time. A flux or forming gas is necessary to ensure a good solder joint is formed. High power devices often use this method because of the good electrical and thermal conductivity of solder. Using the solder die attach method also allows for the possibility of rework, if necessary. However, in order for the solder die attach method to be successful both the substrate and die must not only be metallized, but wettable.

The previously mentioned die attach methods, epoxy, eutectic and solder, for DCA components represent the most common die attach methods used today. The evolution of smaller products and advances in technology will continue to drive this field.

References:
1.http://www.twi.co.uk/j32k/protected/band_3/ksnrs001.html
2.http://ap.pennnet.com/Articles/Article_Display.cfm?Section=Archives&Subsection=Display&ARTICLE_ID=75796&KEYWORD=Die%20Bonding

Characteristic Properties of Materials Used in Electronics Assemblies

Understanding the materials from which electronic components and assemblies are comprised is crucial to the success of any project or assembly. The Electronics Manufacturing Learning Center (EMLC) currently offers a course entitled "Characteristic Properties of Materials used in Electronics Manufacturing" that deals exclusively with materials related issues in electronics. The course relates material properties to product and process quality.

The course objective is to prepare participants to make informed decisions about the materials used in their components and assemblies and how the material properties influence the performance and reliability of their product. Engineers, quality managers, technicians, and designers attend the course to gain an understanding of the fundamentals of material properties. The course curriculum was developed with both the experienced and inexperienced in mind and translates complicated concepts into real world knowledge.

A wide range of topics are covered including:

- Ceramic and composite substrates
- Fluxes
- Semiconductors
- Solder alloys
- Lead materials
- Plastic packaging
- Wire bonds
- Underfills and adhesives
- Solderability
- Contaminants
- Advanced packaging materials
- Board finishes
- Viscosity
- Electrical properties
- Corrosion
- Diffusion

The curriculum is divided into three areas, Selection, Behavior, and Testing.

Selection

Material selection is one of the most common tasks for design engineering. The ability to interpret data sheets and assess the material's impact on the performance of a product is crucial for reliable performance.

Behavior

The actual behavior of a material can be much different from the reported theoretical value. This course discusses the causes of this and teaches the participants how to troubleshoot property variation.

Testing

The testing of material properties is widely understood to be the key to obtaining data for a project, performing failure analysis, or understanding material interactions. Material testing also provides information on the quality of incoming and outgoing products. Inspection test equipment and techniques are demonstrated for a wide range of materials and assemblies during the class. This provides the participant with both knowledge of the common failure modes observed in electronics and the proper techniques for evaluating them.

Participants in the class are first exposed to the definition of material properties. These material properties are then linked to the chemistry and physics that influence product yield, reliability, and quality. Throughout the class there are a number of hands-on laboratories and demonstrations to improve understanding of the topics and relate them to current manufacturing situations:

- Metallography of intermetallics and solders using Scanning Electron Microscopy (SEM)
- Glass transition temperature measurement of polymer materials using Differential Scanning Calorimeter (DSC)
- Characterization of halide content of fluxes and circuit boards
- Wire bonding
- Oxide characterization and quantification

Attendees are encouraged to bring sample products from their companies to use as examples during the labs. A three-day course layout provides the proper format for comprehensive understanding. Each student that successfully completes the course will leave with a better understanding of material properties and how they relate to their individual projects.

For more information about the Learning Center and for course information, please call (610) 362-1320 or e-mail: registrar@empf.org

Cut here and save!!

Manufacturer's Corner

Technical Devices

There is a continual world-wide environmental movement away from the use of tin/lead solder and going towards "environmentally friendly" products. Various alternatives have replaced the traditional use of lead in wine bottle capsules, fishing weights, casting alloys for toys, lead-free ammunition as well as solders for certain plumbing applications.

Additionally, there are now a series of initiatives worldwide that outline targets for electronic equipment re-use and recycling. Legislation potentially affecting the solder and electronic assembly industries is now being proposed by the European Commission via the Waste Electrical and Electronic Equipment (WEEE) directive and Japan with the Ministry of Trade and Industry (MITI) outlining targets for electronic equipment re-use and recycling. This proposal also seeks to limit the use of hazardous materials to improve the ease of recycling. This legislation will impact not only solder alloy issues but also issues concerning component finishes, component temperature ratings, board finishes and flame retardancy. Although a number of states are heading towards lead-free and/or recycling regulation there is not yet a published federal position.

Technical Devices EVS Solder Recovery System

In another step to expand the public's right to know concerning toxic chemicals released into local communities, the EPA is mandating more public reporting by industry on lead emissions. The EPA has lowered the threshold for reporting on lead under its Toxic Release Inventory because lead remains in the environment for long periods of time and is toxic to humans. Previously, manufacturing facilities where not required to report their lead usage. Under new regulations, the reporting threshold is 100 pounds of lead per facility per year and a substantial increase in the amount of information made available to the public.

One piece of equipment that the EMPF utilizes to reduce the amount of lead waste disposal is the Technical Devices EVS Solder Recovery System. This system processes dross into usable solder that is as free from impurities as the initial solder used. The solder recovery process is initiated by raising the temperature of the solder dross to 310ºC, then applying an external pressure of approximately 80 PSI, while maintaining constant pressure and heat. The spirally wound heater bands create a small magnetic field of energy. This encourages the iron oxide in the dross to adhere into a matrix while allowing the molten solder to flow into the ingot tray.

The model EVS 2000 can handle up to 20 pounds of dross per six minute cycle, while the model EVS 4000 can process up to 40 pounds of dross per 10 minute cycle. This size is adequate for the de-drossing of even the largest wave-soldering machine in one operation. With recovery rates averaging 75% of the dross by weight being converted to usable solder, the potential cost savings with the EVS systems are commendable.

The benefits of solder recovery are:
- Reduction in handling of lead contaminated solder dross
- Ease of use - minimal training is required and no extra labor costs
- Short ROI - The SRS can pay for itself within a matter of months depending on the usage of your wave solder machine
- Environmentally friendly and may help your company achieve ISO 14001 compliance.

The EVS Systems provide a closed environment system (when used with its ancillary equipment and options) for the recovery of solder from the solder dross produced during the wave soldering process. The EVS 2000 system includes a mobile support cart, dross delivery system, and a stand-alone filter, which consists of a four-stage filter and a high-speed centrifugal fan. The two systems are designed to be a stand-alone unit, which can operate at the convenience of the user company, without the need for external extraction.

These systems are optimized for use with hot solder dross. The patented process uses pneumatic pressure to extract the solder from the dross at temperature. The solder collected from the process may be stored or returned immediately to the solder bath. The EVS system heats the loaded dross to preset operating temperature. Pressure is then applied via the pneumatic cylinder in order to compress the dross loaded into the machine. This process enables the majority of retained solder in the solder dross to be extracted. The spent dross is deposited from the operating chamber in the dross bucket via the dross chute. No operator involvement is required other than pressing the start button.

The fume extraction unit draws a current of air across the heating chamber, and filters this air before returning it to the atmosphere. This process removes any dust particles, which may accumulate during the solder recovery process or during the dross ejection phase of the process.

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Manufacturer's Corner - Essemtec

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The drop-through dross-collecting chute is constructed from galvanized mild steel and is a two part telescopic design to be attached to the underside of the EVS Systems. The chute will provide a sealed conduit to allow the dross remaining at the end of the cycle to be deposited into a dross container.

The EVS System saves money by reducing the amount of solder that needs to be purchased and by decreasing the amount of dross that needs to be disposed. The price of lead free solder will be 3-4 times that of present solder so that the savings and payback from using Solder Recovery System (SRS) technology will become a standard, making solder recovery a crucial part of all circuit board production. SRS machines of all types will be able to process lead free solder without modification.

This system helps the EMPF comply with local and EPA safety regulations on the safe disposal of lead. If you would like a demonstration of the Technical Devices solder recovery system or visit EMPF, please contact Jeff Stong at 610-362-1200 x224 or jstong@aciusa.org.

**For more information,
please contact the Equipment
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Wide Band Gap Technology for Navy Applications

(continued from page 1)

SiC and GaN devices have several immediate opportunities for insertion to naval applications. The technology deployment will allow for instant savings in power consumption, heat dissipation, and weight, as well as provide new levels of mission capability and performance not attainable using current technology, i.e., solid-state microwave power generation. SiC and GaN devices also have increased robustness, which is ideal for military applications such as:

- Joint Tactical Radio System (JTRS) next-generation, common DoD radio L, S, C, X-band radar applications for military mission radar and commercial navigation and weather radar
- USQ-146 jammer (a new ground version of the USQ-113)
- Military DSCS SHF satellite communications (X-band)
- Commercial terrestrial wireless and satellite communications (L, C, S, X bands)
- New ISM commercial no-license equipment (S, C-bands)

The need for high power at L and X band, plus affordable compact replaceable radar modules, is pushing technology beyond anything available today in production semiconductor technology. We expect to see similar radar sets proliferate to other platforms and applications once the technology is proven to be feasible and affordable.

Production process of SiC technology is is still immature and there are some legal and proprietary issues that need to be worked out. Therefore, the required process technology and devices are unavailable for widespread DoD and commercial use.

A few proficient industrial organizations have developed SiC devices using their own highly proprietary technology; however, the industrial base for vertical integration and widespread application of the material technology is insufficient. The technology's biggest hurdle is the lack of an affordable substrate material. The most widely used substrates are sapphire and silicon carbide. Sapphire is more economically attractive, but SiC is the military's preferred substrate over sapphire for high-power microwave devices requiring high thermal conductivity for optimize performance. Using the SiC wafers fabricated in parallel stages of the project with an epitaxial active GaN layer, the devices produced will have all the electrical advantages of a GaN device with all of the thermal advantages of SiC.

Recently, WBG material suppliers, device fabricators, system end users, and government agencies met at Rockwell Scientific (RSC) to discuss the idea of forming an industrial collaboration. The collaboration would create an open-market for RF WBG devices and WBG PA modules. This would establish a steady and cost effective supplier chain that would provide real WBG devices to the Navy and DOD. The transition panel would also seek opportunities within the Navy to help advance this technology and assist the technology transfer.

Currently, the EMPF and the Electro-Optics Center (EOC) are jointly conducting a survey to assess the status of WBG technology and future technology development in order to provide a recommendation for WBG Mantech programs and investment plans.

Ask the EMPF Helpline!

CUSTOMER ISSUE: Recently, a customer called the EMPF Helpline needing help in replicating Gerber files for a board that was to be put into production. The board consisted of six layers and was built for through-hole technology. The customer needed a soft copy of the layers, drill file and dimensions to have a board fabricator build new boards.

Helpline Response: It is possible to generate a set of Gerber files for new boards to be built. Since there are no hard copies of the layers, the board must be delaminated in order to retrieve images of the layers.

After checking on the type of board, the EMPF scientists decided on the use of Methyl Ethyl Keytone (MEK). This would soften the material but not ruin the board. With this notion, the process of delaminating the board began.

The first step was to remove all components off the board. For this particular board, all the through-holes were checked to ensure of removal of all solder present in the holes. After the board was clear of components and solder, an image of both sides of the board was taken. This provides a reference on how the board looks.

For the delamination process, the tools used were a chisel-like X-acto knife, a hot plate, and a hood for fumes. To be sure which process would work best for this material, samples of the board were taken from breakaway pieces. One sample was soaked in MEK for a specified period of time, another was soaked in MEK and heated at about 40°C for a specified period of time and the last was dipped into the MEK for a few seconds. For this small test run of the board samples, it was determined that heating of the MEK helped the solution soak into the board more quickly.

The board was placed in a pan and MEK was poured into the pan letting the board be engulfed by the MEK. The pan was then placed on a hot plate and heated to 40°C. To keep the MEK from evaporating quickly, the pan was covered with a hood and a pin hole was made to allow gas pressure to slowly release. As the MEK soaked into the board, the chisel-like X-acto knife was used to pry at the edge of the board and determine a top layer. This process needed to be done very cautiously because of the potential damage to the copper trace or pad. Once determining a layer, it is best to keep the layer as in-tact as possible. Though the layer may bow once released from the board, it may be placed down with a weight to flatten it. As each layer was carefully separated from the board, an image or picture was taken for reference.

Once the layers were separated, they were scanned into a program called SCANCAD, where Gerber files were generated. Two reference points on the board were chosen and were aligned as each layer was scanned. When beginning a scan, it is recommended that you scan each layer as they are stacked in the board. You may have to mirror or flip the image that was scanned so that you are either looking through the top to bottom or the bottom to the top. Orientation can be a problem if you are not sure of the stack up or the reference points.

Before placing pads or traces onto the scanned images, sizes of the pads, traces, and holes are measured and noted accordingly. The scanned images are referred to as raster images. These raster images cannot be manipulated except for flipping or mirroring on the X or Y-axis. The raster image provides an image that could be traced over digitally. In a very clean scan, the raster image could be the exact size of each trace and pad and spacing. This provides a perfect match to the board.

With the completion of the Gerber files for the copper layout of each layer, an additional Gerber file is created where the dimension of the board outline and milled out sections were generated. Along with this was the drill file, which was created from a Gerber file that only had pads that were to have holes drilled. One last Gerber file was produced to do the silk screen on top of the board.

After all the Gerber files were done, a report was given to the customer indicating the stack-up of the Gerber file layers of the board, the description of the drill file, the silk screen, the stack-up, and the dimensions. In addition, the type of board, the thickness, no masking as for this case, plating of the exposed pads, mention of the number of copper layers, and any special requests were addressed.

The customer needed verification of the Gerber files to ensure proper layout of the traces and pads. The best way to verify this was to have the schematics handy and the printout of each layer including the silk screen onto transparencies. After the process was complete, the Gerber files were sent to a board fabricator for the build of replicated boards.

If you have an electronics manufacturing problem, call the EMPF Helpline at (610)362-1320.

American Competitiveness Institute - 2002 EMLC COURSE SCHEDULE

Electronics Manufacturing

Electronics Manufacturing BOOT CAMP A - Week 1
May 6-10 Sept. 16-20
Oct. 28-Nov. 1

Electronics Manufacturing BOOT CAMP B - Week 2
May 13-17 Sept. 23-27
Nov. 4-8

Skills

SMT Manufacturing
Jun. 17-21 Aug. 19-23

SMT Soldering/Rework
May 20-24 Jul. 15-19
Nov. 18-22

BGA Manufacturing, Inspection & Rework
Jun. 3-4 Aug. 5-6
Oct. 7-8

Advanced Packaging Techniques
Jun. 5-7 Aug. 7-9
Oct. 9-11

Certifications

IPC J-STD-001 Instructor Certification
May 20-24 Jun. 3-7
July 15-19 Aug. 5-9
Sept. 23-27 Oct. 14-18

J-STD-001 Instructor Recertification
May 13-14 Jul. 8-9
Sept. 16-17 Nov. 4-5

EMPF J-STD-001B Instructor Recertification
Jul. 29-30

IPC Challenge
May 15 Jul. 10
Sept. 18 Nov. 6

IPC-A-610 Instructor Certification
Jun. 10-14 Jul. 22-26
Aug. 12-16 Oct. 7-11

IPC-A-610 Instructor Recertification
May 16-17 Jul. 11-12
Sept. 19-20 Nov. 7-8

IPC-A-600 Acceptability of Printed Boards Instructor Certification
Jun. 26-28

IPC-7711/7721 Rework, Repair and Modification of Printed Boards and Electronic Assemblies
Jun. 10-14, 17-20
October 7-11, 14-17

Continuing Professional Advancement

Design for Manufacturability
Jun. 24-2 Aug. 19-20
Oct. 21-22

Failure Analysis and Reliability Testing in Electronics Manufacturing
Aug. 12-14 Nov. 13-15

Characteristic Properties of Materials in Electronics Manufacturing
Jul. 22-24 Oct. 14-16

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

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