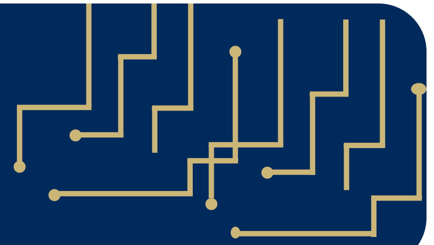
empfasis



A publication of the National Electronics Manufacturing Center of Excellence *July 2003*

American Competitiveness Institute
One International Plaza
Suite 600
Philadelphia, PA 19113
(610) 362-1200 • **FAX**: (610) 362-1290
HELPLINE: (610) 362-1320
WEBSITE: www.empf.org

The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

EMPF Director
Michael D. Frederickson
mfrederickson@aciusa.org

In This Issue

Page 1: MMIC Program - M. Allemang
Page 3: Nanotechnology - A. Vigliotti
Page 5: Custom Training - G. Ramsey
Page 7: SMT Rework - M. Morrison
Page 9: Manufacturer's Corner - J. Stong
Essemtec Expert
Page 11: Ask the EMPF Helpline - J. Butler
Page 12: Upcoming EMLC Courses

Office of Naval Research
Director of Manufacturing Technology
Steve Linder
linderst@onr.navy.mil

ONR Program Officer
Richard Henson
hensonr@onr.navy.mil

MMIC PROGRAM

The next generation of radar systems requires electronic microwave sub-assemblies to replace the older mechanical scanning methods currently in place. The new Active Electronically Scanned Array (AESA) radar, currently being developed for the Navy's F/A-18, requires new processes and manufacturing techniques to assemble reliable, low-cost Monolithic Microwave Integrated Circuit (MMIC) Flip Chips at a high yield. A Navy MANTECH program for the F/A-18 is presently underway involving ACI, NAVAIR Program Office PMA 265 and Raytheon Electronic Systems. ACI's role in this program involves three major tasks. The first is to manage the performance of the program for the Office of Naval Research (ONR); the second is to ensure a non-Raytheon second source foundry that understands the process of this new interconnection; and the third is to perform reliability testing on wafers produced by these second source foundries. The ultimate goal for this program is to ensure a cost-effective, reliable, high performance MMIC interconnection that supports the needs of NAVAIR and the USAF radar systems.

An understanding of the different methods used in flip chip technology is necessary in order to apply a solution that will be cost-effective, manufacturable and reliable. A flip chip microelectronic assembly is defined as the direct electrical connection of face-down flipped electronic components onto substrates, circuit boards, or carriers, by using conductive bumps on the chip bond pads. In contrast, wire bonding, the older technology which flip chip is replacing, uses face-up chips with a wire connection to each bond pad. Due to flip chip materials and equipment available, the advantages that flip chips present over other packaging methods are performance, higher density, flexibility, reliability, and cost due to the flip chip materials and equipment available.

The three stages in making flip chip assemblies are:

1. bumping the die or wafer
2. attaching the bumped die to the substrate
3. filling the area under the die between the bumps with an underfill epoxy (if permitted)

Figure 1 shows a typical cross-section view of a flip chip. Flip chips have survived tests that simulate artillery firing, as well as millions of hours of actual use in computers and automobiles.

The main requirements that bumps must fulfill are:

1. provide a conductive path from the flipped chip to the substrate, or
2. provide a thermal path to carry heat away from the chip to the substrate, and
3. provide a spacer to prevent electrical contact between the chip and substrate, and
4. relieve mechanical strain between chip and substrate

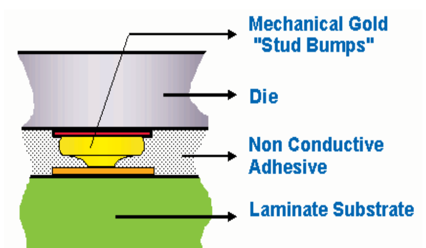


Figure 1. Example of flip chip using stud bumps. Photo courtesy of Valtronic.

continued on page 2

The type of conductive bump and the materials used to attach the flip chip are different for each type of flip chip assembly. The cost, space and performance required will determine which method is best for a particular application.

The three main types of flip chip bumps considered here are: solder bump, plated bump, stud bump

Solder bumps require an Under Bump Metallization (UBM) to be applied to the chip bond pads by sputtering, plating, or other method to define and form a proper surface area for solder wetting. This UBM consists of successive layers of metal. The adhesion layer must provide good contact to both the bond pad metal and the surrounding passivation, providing a strong, low-stress mechanical and electrical connection. The diffusion barrier layer limits the diffusion of solder into the underlying material. The solder wettable layer offers a wettable surface to the molten solder for assembly. A protective layer may be required to prevent oxidation of the underlying layers. [1]

Plasma cleaning and removal of insulating oxides may be necessary before bumping occurs. Solder is deposited onto the UBM by evaporation, electroplating, or screen printing of solder paste. The bumped die are aligned to the substrate pads by a pick and place machine and the assembly is heated to make a solder connection. A comparison of solder bump methods is shown in chart 1.

Method	Advantages	Disadvantages
Solder-Bump - Evaporated	◆ longest production history ◆ extensive reliability data ◆ highest production volumes ◆ uniform bump heights	◆ process limited to lead solders with binary alloys ◆ not easily scaled up to larger wafers ◆ high equipment costs and licensing fees
Solder Bump-Electroplated	◆ lower cost than evaporation ◆ uniform bump heights ◆ close bump spacing (30-50 µm) ◆ best suited for high bump count chips	◆ alloy and bump variation controlled by bath solution ◆ limited to binary alloys
Solder Bump-Printer Chart 1	◆ lower cost than evaporation ◆ excellent reliability in volume ◆ good control of paste bump composition ◆ variety of alloys can be used (lead free)	◆ exposed metal except pads must be passivated ◆ bump spacing limited to 150 µm or greater

Plated bumps use wet chemical processing to plate conductive metal bumps onto the wafer bond pads. One common plated bump is nickel-gold. Electroless nickel plating is used to put the target nickel thickness onto the aluminum bond pads. Next, an immersion gold layer is added for protection.

Silver plated bumps have also been used in applications where an underfill is not desirable, such as with MMIC devices where underfills interfere with microwave performance. The final attachment is usually made by solder or adhesive which can be applied to either the bumps or the substrate bond pads. A comparison of plated bump advantages and disadvantages is shown in chart 2.

Method	Advantages	Disadvantages
Plated Bump Chart 2	◆ lower cost without masks or sputtering ◆ high throughput with parallel processing ◆ scalable to larger wafer sizes ◆ very uniform across wafer height	◆ requires all exposed metal to be passivated ◆ back side of wafer may require protection ◆ plating bath contamination must be low ◆ bump pitch limited since plating process is isotropic

continued on page 10

NANOTECHNOLOGY

Nanotechnology is more than the science of nanoscale materials, carbon nanotubes, and quantum electronics but also represents advancements in technology that can improve the capability of Navy systems and future combat war fighter needs. The American Competitiveness Institute has been requested by the Office of Naval Research to determine the maturity of these, and other nanotechnology areas, and their relevance to DoD and Navy applications.

Nanotechnology did not begin with, but has been spurred on by, the well-known National Nanotechnology Initiative. This research and development funding in the President's 2004 budget at $847 million has increased modestly over previous years for the multi-agency effort. These monies are a fundamental science-based initiative, but the DOD also applies its investment to applied research (6.2) and to exploratory development (6.3). The focus of this effort is in line with transitioning science discoveries in innovative technology through MANTECH programs.

There are different types of nanotechnology, each with different levels of maturity, that ACI has determined through a survey of industry manufacturing capability. Nanoelectronics is an advanced realm of nanotechnology that uses devices such as quantum dots and wires for terahertz computing speeds. The downside of this advanced technology is that relatively few have been produced and testing of these devices is difficult. Focus within nanoelectronics has been on development and understanding and will continue to be so for the next eight to ten years as prototype processes are replaced with manufacturing ones.

Carbon nanotubes are another area of nanotechnology that has greater maturity than nanoelectronics but they are still in a research and development mode and currently have scale up concerns. Carbon nanotubes are a form of carbon that has a rolled-up graphite like or tube-shaped structure. Interesting properties of these materials are that they interact with light efficiently and can react to gases and molecules present in the air to act as high surface area sensors.

One company called NanoLab, Inc. grows bulk carbon nanotubes and is scaling to large volumes. The company can also grow aligned nanotubes on various substrates for customers up to 3" square. They are at a research and development stage with uses for their nanotubes such as field emission displays and nanoscale tweezers. They envision breakthrough applications for nanophotonics, biosensors, and energy storage. Current work for the Army is focused on toughening the armor that our troops wear in Iraq.

Another company, Carbon Nanotechnologies, Inc. (CNI) produces single-wall carbon nanotubes (SWNTs or Buckytubes), also in prototype quantities. They describe these materials as being 1nm in diameter, thousands of nm long, largely defect-free molecules of pure carbon. They continue to say that SWNTs are the strongest, stiffest, toughest material that will likely ever be known. They are the only organic material that conducts like a true metal and the most thermally conductive material known. They also have high thermal stability (500 C in air, and greater than 1400 C under anaerobic conditions). Breakthrough applications they see are strong, stiff, tough, lightweight composites (aerospace), conductive polymers (low observable), high performance fibers (ballistic protection), fuel cells, and field emission displays.

Scale, process efficiency and quality control are current issues of these manufacturers. Once solved for them and for better affordability and availability, two major concerns of MANTECH, these materials could be used in Navy and DoD applications.

The maturest area of nanotechnology that ACI has identified is nanomaterials or nanoscale powders as they are also called. From discussions of current capability and maturity with industry, ACI has identified that his technology has the highest potential for technology transfer within the next three to five years.

Some nanoscale materials take advantage of applying nanoscale coatings to very fine particles. For instance, Powdermet, Inc. is manufacturing production level nickel coated microballons for EMI shielding applications. They have also produced copper coated reinforcement materials that have applications for high thermal conductivity and low expansion substrates. These materials are of interest to electronics manufacturing for Navy applications in that they may lower cost of system designs and provide to designers substitutes to conventional system packaging techniques.

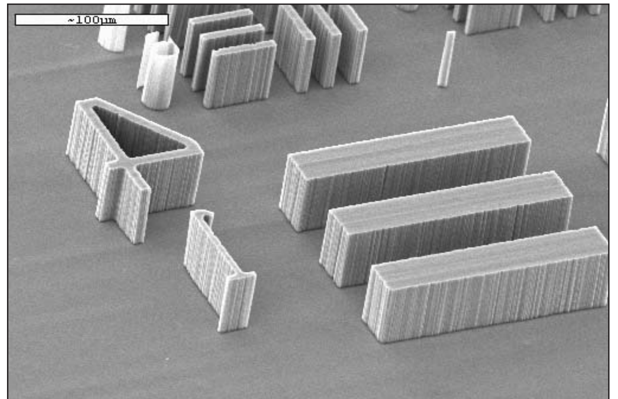
There is a tremendous amount of research into nanotechnology with potential application areas. The filtering process, used to identify industry sources with manufacturing capabilities, has been substantial. Many of the companies that ACI has contacted have been small companies that focus solely on invention and technology, and are unaware of DoD and Navy needs. To aid these small companies, ACI believes that a larger system integrator may be necessary.

continued on page 4

NANOTECHNOLOGY (continued from page 3)

ACI is also determining DoD and Navy applications where nanotechnology might be applied. ACI is working with areas of the Navy such as SPAWAR, NAVSEA, and NAVAIR, to determine where we might apply nanotechnology to satisfy a need for improvement of capability and performance. NAVSEA is providing requirements that ACI is analyzing against nanotechnology areas in order to make recommendations on areas that warrant further investigation.

Once application areas are determined, we can transition and link advanced materials and nanotechnology to these DoD and Navy systems. Specific manufacturing issues of industry will be known and we will establish recommendations for manufacturing capability to transition the technologies. Links between program acquisitions, application developers, and industry nanotechnology will in this way then provide increased capability to Navy and DoD systems.



This photo, courtesy of Nanomaterials Research, LLC, depicts structures with nanoporous features used in micorelectronics applications.

Skills-Based Training

at the Electronics Manufacturing Learning Center

BGA Manufacturing, Inspection & Rework

December 1-2

Chip Scale Manufacturing

November 5-7

Contact the Registrar for details and registration 610-362-1320

registrar@empf.org

Design for Manufacturability

Course at the

Electronics Manufacturing Learning Center

November 17-18

Contact the Registrar for details and registration

610-362-1320

registrar@empf.org

Custom Training

The pace of change in the electronics industry requires an ongoing commitment to acquire new knowledge and skills. Competition demands maximum value from every dollar. In order to ensure proper balance, organizations, and individuals alike, must consider training investments in conjunction with other strategic initiatives. Off-the-shelf programs may not be adequate to achieve goals. Industry-consensus training programs may not be sufficient to ensure competitive advantage. What is your position on the continuum from mainstream to cutting edge? Where do you need to be?

- Identify the gap
  (a process known as needs assessment)
- Define the training objectives
- Select training techniques
- Implement the program.

This article will discuss rational opportunities to develop competitive advantage through customized training programs. Training should provide resources needed to achieve the organization’s overall goals as well as the personal goals of the employees. Training plans must be developed systematically. Companies that purchase training programs without regard for the current and future needs of the organization, set upon an uncertain path.

Ideally, a team should develop the training plan. Input from representatives of all business functions should participate in a forum for defining the goal of the program. Be sure to include strategic management, supervisors, workers and training providers. Many companies have a wealth of information and quality data such as statistical data collected from product lines and customer feedback surveys.

Numerous other analysis tools lend themselves to needs assessment. Be sure to consider market surveys, internal audits, job shadowing, focus groups, skills assessment tests, and self-assessment by workers. Needs analysis tools should provide accurate quantitative and qualitative information while being sensitive to company time and cost restraints.

The assessment phase of planning must identify the difference between desired employee performance and actual performance. The scope of the training plan is important. Do not try to establish the rational for training in the middle of an implementation phase.

Discipline and planning are critical when waste can not be tolerated. Activity without objectives can not be evaluated. Objectives without goals may lead down a dead-end path. Goals should answer a strategic requirement. Objectives should be the result of a process road map to achieving the goals. Goals need not be measurable but objectives should be specific, measurable, attainable, and fixed in time.

Place emphasis on what is needed before deciding a method of delivery. The actual instructional approach depends on several factors. The planning team must consider the nature of the tasks and skills to be learned, the number of employees to be trained, and the employer's resources. The best method in each instance can be identified by considering cost effectiveness, desired program content, appropriateness of the facilities, student preferences and capabilities in the context of learning principles.

ACI offers a variety of instructional programs selected and designed to meet our client base. In many cases our standard programs are capable of providing needed training at reasonable cost. Standard programs are scheduled for needs related to:

- Career Based Training
- Certification Based Training
- Skills Based Training

Our unique combination of factory, technical instructors, academic instructors, and lab facilities provide a hands-on approach, best suited to technology transfer.

Larger organizations may find an advantage when planing training programs. Individuals and small institutions may not be able to justify customizing programs to achieve specific organizational goals in a manner consistent with management's philosophy and strategy. In some cases, our clients are able to achieve a better value through custom training, training designed specifically for a client's training objectives or work environment. ACI utilizes a systematic approach to development of curriculum. ACI's team of instructional designers and subject matter experts work closely with its clients in order to ensure the program is successful from the start, through design, development, implementation and evaluation.

ACI's team will first meet with key members of the client’s organization in order to help determine needs and establish goals as well as perform assessments of the performance environment, student’s potential, and the training site.

During the next step of the process, ACI's team will develop performance objectives that will address the

continued on page 6

client's requirements, needs and ultimate goals of the project. Upon approval of the performance objectives by the client's organization, the team will proceed with the development of assessment instruments that will determine whether the trainees have met the client-approved performance objectives. Assessment instruments may include written or oral tests, as well as laboratory exercises. Once assessment instruments have been finalized, the instructional design team will continue through the development of instructional materials and an appropriate instructional strategy (instructor-led, activity-based, computer-based, or a combination thereof).

The instructional strategy will be identified as one that will effectively maximize the transfer of skills and knowledge from the classroom to the client's work environment.

The instructional design team will continue to be involved through the implementation of the training and assessment process in order to properly evaluate the instructional materials and validate the assessment instruments. Follow-up evaluation is customarily completed with the client in order to determine that goals of the project were met to the client's satisfaction.

The standard programs offered by ACI are exhaustive, covering nearly every aspect of electronic manufacturing. Generally, a custom program is based on one or more of our standard programs, assembling modules to emphasize or eliminate material specific to the program objectives. ACI has customized training programs based on curriculum material found in:

- Boot Camps
- BGA Manufacturing
- Cleaning
- SMT Rework
- SMT Manufacturing

Custom training can focus objectives on the client's specific equipment, unique manufacturing environment, and unusual customer needs. In larger original equipment manufacturers or contract manufacturing service organizations, this focus can reduce training times and at the same time improve skills and knowledge transfer.

Depending on the scope of the project, custom training programs can be developed in a few weeks. Enterprise-wide programs may require months to develop. ACI has the expertise and experience to satisfy your training needs with surprising speed.

ACI has working relationships with federal, state and local educational agencies. There are significant opportunities to obtain funding assistance, including full grants, partial grants and loans to pay for training.

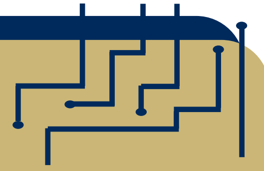
Please review our program schedule located on the last page of this publication for details. Our catalogue and course schedule are also available on-line at www.aciusa.org or by calling the registrar at (610) 362-1200 ext. 250.

For information on custom program development contact the EMPF Helpline at (610)362-1320.

Cut here and save!

TECH TIPS...

SMT REWORK



Many manufacturers have made great strides in defect reduction through process control and continual improvement. Statistical process control shows that because of inherent variation, defects can be greatly reduced but not completely eliminated. There will always be some percentage of assemblies that do not conform to requirements and must be reworked. The need for rework will vary among manufacturers, products, production equipment, production shifts, and even days of the week, but it will never completely be eliminated.

The advancement of SMT technology in electronics manufacturing has produced many significant benefits. One benefit not often discussed is the ease of repairing and reworking SMT component defects when compared to through-hole technology defects. Twenty years ago, replacing a 16-pin DIP package IC required great skill and ability. Repair technicians not only had to be concerned with damage to component leads, but also to the PCB laminate and plated through-holes. Many technicians resorted to destructive component removal, clean up and repair of the land area, and then installation of the new component.

Today, even fine pitch QFP and BGA IC packages can be replaced by repair technicians with little concern about damage or reliability. Modern hot air and IR rework systems often employ product or part specific thermal profiles which are repeatable and make consistently reliable solder connections. Though SMT has made rework easier, advances in technology have not eliminated rework problems. Component size is decreasing while placement density is increasing, making the possibility of affecting adjacent parts during rework a growing concern.

There are several types of SMT rework equipment available to manufacturers. Hot air convection, IR radiation, and resistance-heated conductive tip systems are the most common. Manufacturers purchasing SMT rework equipment must weigh the pros and cons of these unique systems as they vary greatly in cost, accuracy and ease of use.

In general, conductive tip systems are less expensive but require greater skill and manual dexterity. Hot air convection systems offer good reliability and repeatability but care must be taken in tip and barrier selection to ensure adjacent components are not damaged by air flow. IR systems offer greater control of the thermal foot print through focusing lenses but require greater technical expertise and knowledge because IR absorption rates vary greatly between differing components, and materials.

No matter what rework system or method is employed, the goal is to provide quality solder connections when replacing SMT components without damaging the substrate or adjacent components. The following suggestions are provided as universally accepted guidelines and best practices to help ensure that goal is met.

For All Rework Systems -

1. Minimize the number of times a component is removed and replaced to prevent internal damage to the PCB and to prevent excessive inter-metallic growth which could adversely affect solder joint reliability and wetting.

2. Clean components and PCB as soon as rework is accomplished.

3. Use of high activity flux is highly discouraged. Only no-clean or rosin flux should be used when performing rework or repair.

For Heated Conductive Tip Systems -

4. The temperature of soldering tips should not exceed 700 degrees F (370 degrees C). The potential for PCB or component damage increases exponentially beyond 700 degrees F.

5. When using conductive tips, heat should not be applied to the land area for more than 3 seconds. Research indicates that for tip temperatures between 550 degree F and 850 degree F, it only takes 1.5 seconds for eutectic solder to reflow. Remaining on the land area for longer than 3 seconds only multiplies the possibility of thermal damage.

6. Use conductive tips that will heat all of the component leads simultaneously. When all of the solder on all of the leads has reflowed, the part may be removed with tweezers or, in some cases, the tool itself. Special tips are provided by manufacturers of conductive systems to fit a wide range of component applications. In the event an in-house tip must be constructed, it should be made of tin plated copper.

continued on page 8

American Competitiveness Institute 610-362-1200

SMT Rework (continues)

For Modern Computer Controlled and Automated Hot Air or IR Equipment -

7. Investment in the time and effort needed to create an accurate profile will pay huge dividends when installing BGA's, PLCC's and HD QFP's. Variables induced by humans are virtually eliminated in such systems. Expect longer profile times as these sys-ems provide for pre-heat, soak and reflow slopes similar to large mass reflow ovens.

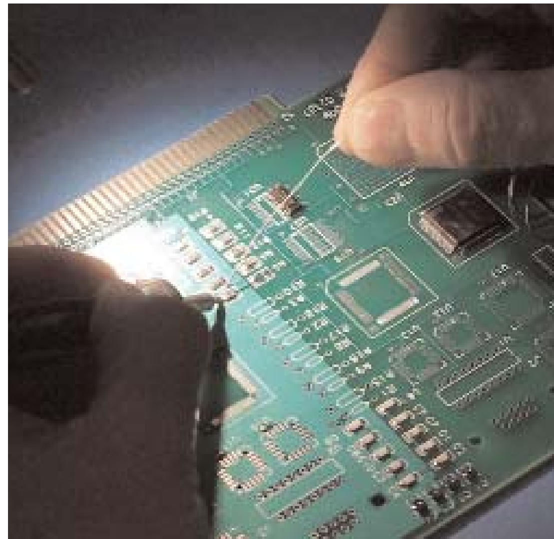
For Older Hot Air Rework Equipment (not programmable or automatic)-

8. PCB's should be pre-heated before component removal. This will help to create a homogeneous temperature of the repair area and reduce thermal shock during removal.

9. Components should be pre-heated prior to installing into liquidus solder. Cold component leads entering hot liquidus solder will cause the solder to cool and solidify before lead wetting can occur. The solder joint would then have to be driven back into reflow to allow the component leads to properly wet. This creates excessive time under temperature, growing the inter-metallic region, and possibly exhausting flux agents which may lead to de-wetting.

10. Care should be taken to direct the flow of air in convection systems toward the component to be removed. Time and temperature controls should allow removal of components within 20 seconds, without charring flux or damaging the PCB. Some PLCC's may require heating exposure longer than 20 seconds, and will probably result in some flux charring which is difficult to clean. Thermal profiles running longer than 50 seconds run a high risk of PCB discoloration and damage.

For further information on SMT rework, the EMPF offers detailed skills-based rework and repair courses. Please see the back of this EMPFASIS newsletter for a complete list. The EMPF also has many new and cutting edge rework systems manufactured by industry leaders that are available for demonstration.



An example of SMT rework

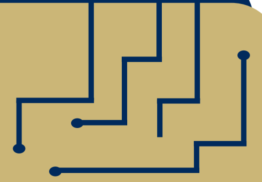
For complimentary Electronics Manufacturing support, contact the Helpline!

610-362-1320

Cut here and save!

Manufacturer's Corner

Essemtec Expert



With the time-to-market of consumer electronics rapidly decreasing, the demands on equipment manufacturers has increased to meet these needs. A good example is the personal computer industry and the quick release of higher speed microprocessors and integration of new capabilities (i.e. USB or "Fire Wire" ports). Quick turnaround on small lot sizes and prototyping units has become a desirable service to the electronics industry.

Military electronics, on the other hand, demands high quality and high reliability (mission critical), again putting an increased demand on equipment manufacturers. A machine that the EMPF utilizes to address both the demands of the consumer and the military is the Essemtec Expert. The Expert is a semi-automatic, precision protype assembly station.

The Expert pick-and-place machine not only enhances the EMPF's capability, but also fulfills a need for assembling a prototype unit for a customer. The Expert has been important in the prototype build of a redesigned communications device for the EMPF. The communications device consisted of seven plated through-hole (PTH) boards with dated technology. These seven boards were reduced to one SMT board with current and proven technology. The Expert was particularly important in the assembly because of its easy programming, precision, and virtual graphics capabilities.

The Expert is able to achieve precision through its linear incremental glass scale and CAD download capabilities. The CAD download provides you with the component location for placement, while the linear incremental scale provides precise X-Y axis coordinate information. For fine pitch device placement, an automatic lowering function is integrated, using air suspension to carefully lower the component. An adjustable down stop mechanism prevents unintentional contact of the component with the solder paste before alignment. After the fine alignment, the operator lowers the component automatically onto the PC Board without the danger of misalignment. The technique is extremely useful in the placing of MEMs devices on a substrate. This soft touch allows the MEMs device to be placed without damage. The Expert is capable of placing 0201 chips to QFP's with 16 mil lead pitch.

The Expert has an optical alignment system for BGA's, CSP's and flip chip placement. The up/down vision system and split vision allows operators to precisely align the component by overlaying the image from the board with the actual component leads before placing it onto the board. The pneumatic locking assures precision placement.

The PCB assembly can be programmed manually or through CAD conversion software. Once programming is completed, the software sequentially guides the operator through all of the pick-up and placement locations. Component placement and rotation is clearly displayed by a virtual component-on-the-screen, which indicates graphically pin number one or polarity points. The virtual graphics provide a beneficial aid for complete and proper assembly.

Adding to the Expert's versatility is the use of standard reel components, JEDEC matrix trays, "Cut Tape" (strips cut from reels), stick tubes, loose components, and bare die mini-pallets. This versatility in using industry standard feeding makes the Expert a true flexible machine.

Some key features include:

- 360 Degree rotation placement head
- Fast/Flexible clamping PCB fixturing
- Motorized, Random-access component turntable
- PC Control System
- Fine pitch placement system with locking x/y/z movement
- Fine X/Y adjustment
- Split vision camera system
- Placement area illumination
- Feeding system
- Tape feeders for 8, 12, and 16 mm tapes. (Up to 40 of a 8 mm type)
- Universal stick feeders
- Motorized turntable for loose components, 45 or 90 bins
- Waffle trays - JEDEC
- Strip feeders from small pieces of tape
- Bare die bins

MannCorp of Huntingdon Valley, PA offers this product in North America. Their Website is www.manncorp.com. If you would like to see a demonstration of the Essemtec Pick-and-Place, please contact Jeff Strong at the EMPF, 610-362-1200 EXT 224.

MMIC PROGRAM (continued from page 2)

Stud bumps of gold are processed by modifying a standard wire bonding technique. Gold ball bonds for wire bonding are formed by melting the end of a gold wire to form a sphere. This gold ball is bonded by ultrasonic energy to the chip bond pad as in a standard wire bonding process. Then the wire bonder procedure is modified to break off the wire at the ball interface directly after attaching the ball to the chip bond pad (see Figure 2). The gold ball, or stud bump, remaining on the bond pad provides a permanent connection to the underlying metallization. The stud bumps can be flattened or coined by mechanical pressure to give a flat top surface and uniform bump heights as well as flattening any remaining wire tail.

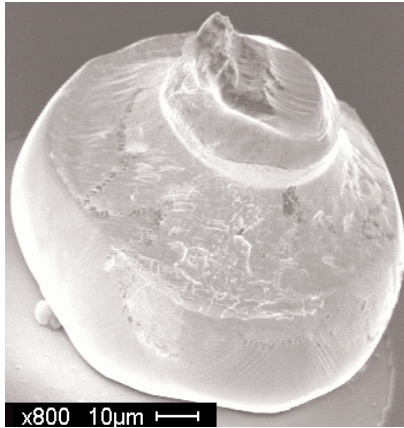


Figure 2

Gold stud bump flip chips can be attached to the substrate pads with adhesive or by thermosonic gold-to-gold connection[1]. A comparison of stud bump advantages and disadvantages is shown in chart 3.

It is usually desirable that the space under the flip chip and around the bumps be filled in with a non-conductive underfill adhesive that joins the entire surface of the chip to the substrate. The underfill will protect the bumps from moisture and provides additional mechanical strength to the flip chip assembly. The underfill will also help compensate for any thermal expansion difference between the chip and the substrate. The difference in the Coefficient of Thermal Expansion (CTE) between the flip chip and the substrate can be mitigated by a properly formed underfill so that electrical bump connections are not broken or damaged. Underfills can be needle-dispensed along the edges of each chip and drawn under the chip by capillary action. Heat is then used to form a permanent bond.

Method	Advantages	Disadvantages
Stud Bump	◆ wire bonder widely available and characterized ◆ bump pitches < 100 µm, pads < 75 µm ◆ flexible to both die and wafers ◆ does not require UBM ◆ easy to scale to high volume	◆ bumping time increases with number of bumps ◆ demands precise die placement equipment ◆ less tolerant of placement errors

Chart 3

In some cases, the underfill will interfere with the operation of the device and can not be used. This is the case with the MMIC flip chip described above since an underfill interferes with high frequency microwave operation. New techniques such as plating silver bumps without underfill have been developed to address these specific needs.

The MMIC Mantech program is pursuing a path to qualify a wafer bumping process utilizing silver. These methods, proprietary to Raytheon, were initially started at the former Hughes Research Lab. Establishing a high speed production effort at their Andover, Massachusetts RF components facility, Raytheon is also supporting the transfer of key characteristics of potentially two additional non-Raytheon vendors. Full qualification of these non-Raytheon foundries for AESA radar production will occur after completion of this program.

In conclusion, flip chip assembly has significant advantages over other microelectronic packaging. One can choose from several varieties of flip chip bumps including solder bump, plated bump and stud bump. The application, cost, underbump metallization, and underfill all contribute to choosing the best suited flip chip bump. ACI is aggressively working with various contractors and research laboratories that will improve the performance of flip chip interconnects, raise the reliability and availability of the assemblies and lower the cost. ACI is also pursuing various methods of inspection that would provide real-time, non-destructive testing of flip chip systems. The endeavors of the MMIC flip chip program will greatly benefit the various users of flip chip technology today and in the future.

References: [1] www.flipchip.com

Ask the EMPF Helpline!

CUSTOMER ISSUE: An EMPF helpline caller requested information on the proper application of terms found in the modified Coffin-Manson equation. The modified Coffin-Manson equation describes behavior of solder joint reliability in ball grid arrays (BGA) and in particular the effects of temperature on the same.

Answer: There are numerous mechanism(s) for failure with BGAs. The most common stresses which result in failure are thermal mechanical (e.g. thermal cycling), temperature/humidity, and thermal aging. Sub-categories exist for all of the above. For temperature effects: the wider the temperature extremes the larger the resulting acceleration factor. Making the temperature spread too large, may induce further damage. The utility of additional terms like solder height and coefficients of thermal expansion while adding accuracy may not be available to the experimenter or requires further experimentation. The Coffin-Manson equation can relate accelerated temperature cycling to actual field use. The test range should be larger than the expected temperature range in use.

In reliability analysis, once a set of test qualifications are known, acceleration factors can be calculated which predict lifetimes of the subsystem(s) later in time or frequency. In its simplest description, the acceleration factor (AF) relates a random variable x_0 like time to failure at operating conditions to a random variable x_t like time to failure at a test condition.

$$x_0 = AFx_t$$

To select an acceleration factor one needs to select a relevant acceleration model. The choice of a model is based on the failure mechanisms expected. It is important to define test parameters that result in observing the effects of a single, unique failure mechanism.

Many descriptions of the cyclic term in the modified Coffin-Manson equation set the use (field) f0 frequency equal to 6 (per 24 hours). In most cases this is done without explanation. The choice of 6 has been based on a "typically assumed value in the electronics industry". The choice is associated with the time to reach thermal equilibrium. The help line customer wanted to check the origin and validity of such a statement. One physical explanation is that maximum damage to the solder joint occurs within four hours. This damage has been ascribed to creep-relaxation. Longer times between cycles wouldn't further degrade the joint. In addition, there is a minimum usable field frequency of 2 owing to temperature changes over the course of a day. Any thing less is inappropriate for modeling with the equation.

Conclusion: The modified Coffin-Manson equation can be used as a first approximation to determine thermal solder joint reliability. This includes applicability to other solder types and/or grid arrays. Some of its limitations have been addressed to aid in the accurate use of the modified Coffin-Manson equation.

Epilogue: The most appropriate model for thermal cycling effects is the Coffin-Manson equation and variations on the same. The Coffin-Manson equation was based on an inverse power law originally used to model metal fatigue subjected to thermal cycling. Coffin-Manson in its simplest form takes into account temperature differences. The equation can include numerous effects as additional terms. The validity of the original Coffin-Manson equation is determined by the operating temperature (high) being lower than 0.5 times the melting temperature in degrees Kelvin. Typically this is good for high melt, 90-10 Pb-Sn solder but not eutectic solder [1]. Typical eutectic solder operating temperatures (>300K) are much greater than 0.5 times its melting point (456K). Thus the equation in its simplest form is inadequate for predicting thermal fatigue of eutectic solder connections. The exponential term corrects for this and renders the equation appropriate for eutectic solder. Other high temperature fatigue effects include grain boundary sliding that require more terms in the equation to account for this Variations include frequency terms and peak temperature. In our embodiment, the acceleration factor is a function of the cycle frequency, difference of temperature, and the maximum temperatures of test and field. This equation is known as the modified Coffin-Manson or Norris-Landzberg equation [2].

$$AF = \left(\frac{\Delta T_t}{\Delta T_0}\right)^{1.9} \left(\frac{f_0}{f_t}\right)^{1/3} \exp\left(\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_t}\right)\right)$$

Where ΔT refers to the difference between high temperature and low temperature during a given cycle, f refers to the number of thermal cycles (typically per 24 hour day), Ea is the activation energy, taken as 0.122eV/K, k is the Boltzmann constant, and T refers to the maximum temperature (K) of the cycle. The subscript 0 refers to the field while the subscript t refers to the lab.

References:

[1] Viswanadham, P. and P. Singh, "Failure Modes and Mechanisms in Electronic Packages"

[2] Gerke, R. D. Proc. of NEPCON/WEST 1994, 1087

For expert solutions to your electronics manufacturing problems, call the EMPF Helpline! 610.362.1320 helpline@empf.org

American Competitiveness Institute - 2003 EMLC Course Schedule

Electronics Manufacturing

BOOT CAMP B - Week 2
October 20-24

Skills

Chip Scale Manufacturing
November 5-7

BGA Manufacturing, Inspection & Rework
December 1-2

Certifications

IPC J-STD-001 Instructor Certification
October 27-31

IPC-J-STD-001 Instructor Recertification
November 17-18
December 8-9

IPC-A-610 Instructor Certification
November 3-7

IPC-A-610 Instructor Recertification
November 20-21
December 11-12

IPC Challenge
November 19
December 10

Continuing Professional Advancement in Electronics Manufacturing

Design for Manufacturability
November 17-18

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

issue:07-03

Emprasis is a publication of the ***American Competitiveness Institute* and the EMPF**
The EMPF is the U.S. Navy's National Center of Excellence dedicated to advancing the state-of-the-art in electronics manufacturing and increasing domestic productivity in electronics manufacturing.

WEBSITE: www.empf.org
HELPLINE: (610) 362-1320
(610) 362-1200 • FAX: (610) 362-1290
Philadelphia, PA 19113
Suite 600
One International Plaza
American Competitiveness Institute

PRESORTED
STANDARD
U.S. POSTAGE PAID
PHILADELPHIA, PA
PERMIT NO. 5490