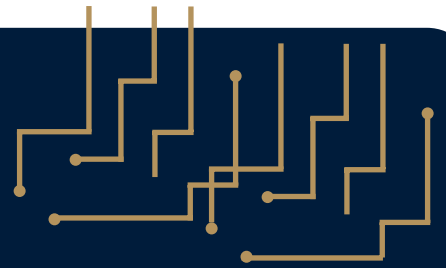


# empfasis



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*The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.*

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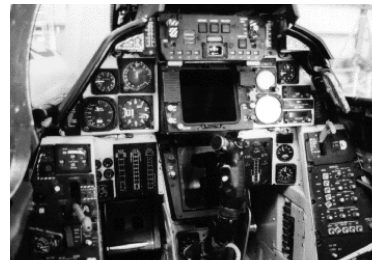
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## Aging Aircraft: Cost of Total Ownership

The total cost of ownership for any system starts accumulating at its inception and completes when the last system is disposed of - "from inception to grave." To control or minimize these costs, the inception and design phase must be thoroughly thought out. Designs and maintenance costs are fairly well "locked in" during the design phase and the costs to correct any deficiencies

lengthen the life of systems is an ever increasing requirement. To achieve long life, the ability to interject pre-planned product improvements, P<sup>3</sup>I, is a critical factor that must be defined in the design stage and must be followed during the operational phase of any program. An example of an aircraft that achieved a long life due to a pre-planned product approach was the Northrop Grumman F-14.



F-14 Cockpit before and after



Left: A-4A Skyhawk Right: A-4M Skyhawk.  
Notice the structural changes between the two versions.

become more and more costly as the systems age. The factors to consider in the design phase, so as to minimize the costs of ownership, include design costs, manufacturing costs, operational costs, and disposal costs.

In the design phase of the F-14, planned upgrades in power plants and electronics allowed for additional capabilities to be incorporated without major airframe redesign. As illustrated in the images above, the original

In the aviation community, the ability to maintain costs and

*continued on page 2*

## Aging Aircraft: Cost of Total Ownership *(continued from page 1)*

cockpit allowed sufficient space to bring in new displays, controls and switches required to support advancements in air warfare. On the other hand, the A-4 Skyhawk was subjected to several major airframe changes to accommodate upgrades that were not planned nor scheduled during the design phase. As illustrated in the photographs of the A-4 Skyhawks on the previous page, the addition of the “hump” in the A-4M was required to contain electronics and controls which the original airframe could not contain.

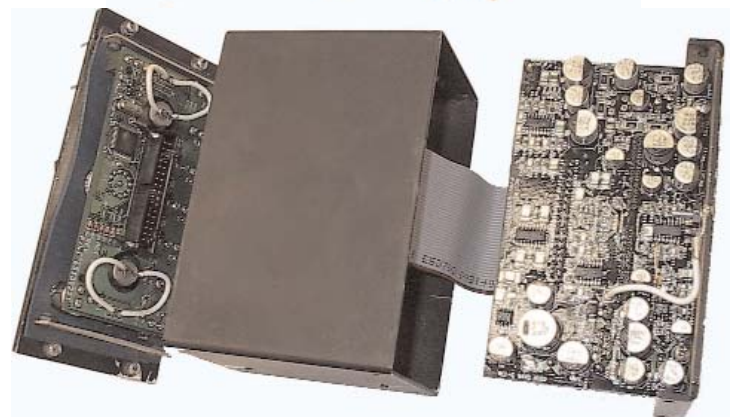
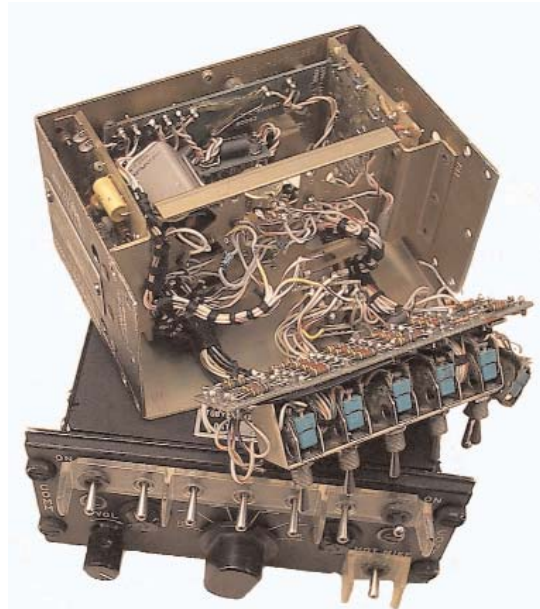
A major driver controlling Operational Availability,  $A_O$ , in aging aircraft is the electronics. As the age of the aviation fleet is extended, the ability to return electronic assemblies to service is impacted by parts and manufacturing techniques that may not be available. This has created the need for assembly cannibalization and costly partial redesigns that create excessive costs to the using organization.

How can the cost of maintaining systems be controlled and minimized? Incorporating the systems engineering techniques at the program inception is best - incorporating the systems engineering concepts during the operational stage is mandatory. Systems Maintenance Costs are comprised of the following categories:

- ◆ *Level of Maintenance Support.* Determine the sparing levels, maintenance personnel capabilities, and type of equipment available to perform the maintenance.
- ◆ *Repair Policy.* Where are the locations of the various repair centers (operational, intermediate and depot)? Is the maintenance performed by the owner or manufacturer? What is the scrap/repair policy, and where are the spares located?
- ◆ *Responsibility of Support.* Detail of diagnostic capability (Built in Test, BIT), accessibility, and readily removable functional package must be determined.
- ◆ *Major Elements of Logistics Support.* Standard test interface, test database requirements, training of maintenance personnel, and test philosophy should be established.
- ◆ *Effectiveness Requirements.* Mean time to repair (MTTR), frequency of scheduled maintenance, mean time between failures (MTBF), and administrative down time for logistics (ADTL - the time required to receive a spare part once ordered) are all major drivers to the size and therefore the cost of the spares pool.
- ◆ *Maintenance Requirements.* Skill level of maintenance personnel, calibration facilities, and facility requirements should also be established.

Regarding the maintenance development plan for aviation, the Aircraft Manufacturers Association Maintenance Planning Document (MSG-3), helps establish a logical progression to a maintenance and replacement policy. For Naval Air Systems, the governing documents that help establish the maintenance plan and redesign considerations are MIL-STD-2173 Reliability-Centered Maintenance Requirements for Naval Aircraft, Weapons Systems & Support Equipment.

ACI is re-engineering the C-6533 intercom for CECOM as well as providing support for the testing and analysis of the replacement gyro for the H-60 and H-47 helicopter fleet. ACI is also supporting NAVAIR Aging Aircraft in failure analysis, parts obsolescence and the desire to extend aircraft life and maintenance costs.



Legacy C-6533 intercom (top) was cost prohibitive for repairs. ACI redesigned the C-6533 (bottom) with current technology and significantly reduced maintenance costs.

# Chip Scale Manufacturing

When referring to "chip scale" component packages, it is still unclear exactly what constitutes a chip scale device. Does the term chip scale include microBGA packages as well as flip chip, chip on board and multi chip modules? Technically, the standard industry definition of a chip scale package is a package that is <1.2 times larger in total area than the area of the silicon die. For the purposes of this article, which is intended to discuss the various manufacturing techniques and processes involved in using chip scale packages, we will include processing methods for microBGA's, and direct chip attach technologies.

## Printed Wiring Board (PWB) Design Considerations

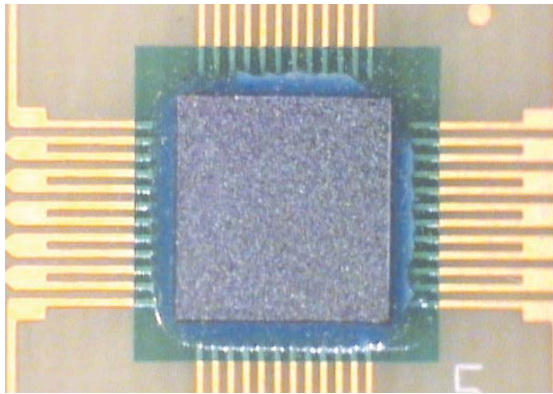
Successful processing of PCBs using chip scale component packages begins with the design of the PWB substrate. Issues such as circuit routing, land pattern and via design, solder mask and surface finish, all play an integral role in the overall success of the assembly process. Routing of circuit traces and associated vias increases in complexity when using area array devices. In order to compensate for the additional routing complexities, additional substrate layers may be required. The selection of land pattern design and solder mask placement is critical to solder joint integrity, reliability and verification. The use of non-solder mask defined land areas imparts less solder joint stress than does the use of solder mask defined lands. Providing a solder mask dam between the land area and any associated vias will prevent solder scavenging or solder flow into the vias during the reflow process. An additional concern is the PCB surface finish. When using microBGA and chip scale component packages, the fine pitch of the components usually requires coplanarity of the component land areas. The use of a standard HASL (hot air solder level) tin/lead surface finish will not provide the required coplanarity for these devices. Alternative surface finishes such as OSP (organic solder preservative), immersion silver or electroless nickel/gold (ENIG) may be required. Violation of these coplanarity issues will inevitably lead to open solder joint connections on the final product assembly.

## General Assembly Considerations

The incorporation of chip scale devices into circuit designs has become increasingly necessary in order to fulfill the industry requirements of more end product capability and performance into a smaller overall package design. Some of the process considerations that must be addressed in order to successfully manufacture products using chip scale packages include material dispensing (primarily for underfilling and encapsulation), inspection, cleaning and rework. The characteristics of chip scale components may require modifications to these assembly processes in order to compensate for decreased component package dimensions.

## Material Dispensing

Dispensing of underfills and encapsulants requires more sophisticated equipment than may be required for production of assemblies using standard surface mount technology (SMT) components. The ability of the dispensing equipment to provide underside heating and the ability to program a various array of dispensing patterns is crucial to assembly processes when using chip scale components. Underside heating of the assembly is required in order to allow the capillary wicking action of the underfill compound to take place. Having the underfill material completely fill the entire area under the microBGA or flip chip is crucial for overcoming coefficient of thermal expansion (CTE) mismatch between the PCB substrate and the chip scale component as well as for adding enhanced mechanical strength to the component. When processing assemblies that incorporate chip on board (COB) components, the dispensing equipment must be capable of encapsulating the COB component without risking damage to the delicate wire bond connections between the component and the PCB substrate.



Flip chip mounted to PCB substrate prior to underfilling

## Inspection

By design, the electrical connections between the PCB substrate, microBGA's and flip chip packages are hidden from visual inspection. There is some visual inspection

equipment that allows visualization of the underside of the component package. However, in most cases, the equipment is limited by the inability to fully examine the entire package. In these instances, process anomalies such as solder bridges, open connections and voids may not always be detectable. The most reliable and comprehensive method of inspection of chip scale component connections is through the use of X-ray technology. By providing images based on material density, X-ray images will show process defects such as solder bridging, open connections and solder voids within the solder connections. Although comprehensive, X-ray imaging requires special operator training in order to detect some of these anomalies that may appear as subtle changes in the image.

## Cleaning

Smaller chip scale components have a considerable difference in component standoff height from the PCB substrate than do standard SMT components. In some cases, the standoff height of a flip chip component may be as little as 0.5 mils (0.0005").

*continued on page 4*

# Chip Scale Manufacturing

(continued from page 3)

When using a no-clean chemistry in your process, standoff height may or may not become an issue. However, when using a process that requires assembly cleaning, the cleaning equipment must be able to penetrate these micro standoff distances to ensure effective residue removal underneath the chip scale component packages. This may require specialized cleaning equipment or modifications to the equipment and/or cleaning process currently in use.

## Rework

When considering the rework process requirements with the use of chip scale components, certain product design consideration must be incorporated into the assembly. Was the assembly designed with sufficient clearance around adjacent components (keep-out distance) to allow for rework tooling? Is the PCB substrate surface finish and land pattern design able to withstand the rigors of the rework process? If underfill material is required, is it reworkable?

From an equipment perspective, the use of split vision for component alignment, the capability to regulate the dynamics of the thermal process, and the ability to provide sufficient underside and topside heating is paramount to the success of the rework process. Another consideration is the training of the rework operators. Differences in PCB and pattern design, surface finish and thermal requirements of chip scale components compared to standard SMT components requires specialized operator training to avoid the potential of end product damage.

## Stencil Printing

When dealing with chip scale packages, the standard process of stencil printing solder paste onto the PCB substrate using a standard 6-mil thick stencil may not necessarily apply. In most instances, when using flip chip and microBGA components, tacky flux is used in place of solder paste, and the deposited material is approximately 2 to 4-mils in height. In some cases, depending on the component pitch, microBGA components can be placed into solder paste, however the standard height of the deposit will be less than the usual 6-mils customarily used on standard SMT components. How does this affect the stencil printing process? Primarily, the process will remain the same but major design changes to the standard 6-mil stainless steel stencil will be required. When dealing with ultra fine pitch components, a chemically

etched stencil will not yield the precision required; therefore, a laser etching or electroforming stencil manufacturing process will be necessary. This will increase the cost of the stencil. On PCB assemblies that incorporate both standard SMT and chip scale packages, step etching the stencil to provide for smaller material deposits on the ultra fine pitch component lands will be necessary. This means a more flexible squeegee blade, usually rubber or urethane, will be needed. Depending on the pitch of the components used on the assembly, it may be necessary to deviate from the standard mesh #3 solder paste and use a mesh size of #5 or #6. The fine mesh solder paste allows for better paste transfer through the stencil apertures and better release from the stencil apertures in fine pitch applications.

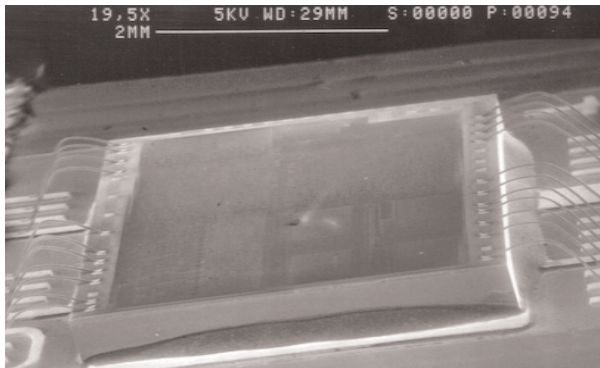
## Reflow Soldering

The reflow process for assemblies incorporating chip scale packages is similar to that of PCB assemblies using standard SMT components. There may be a need however to lower the volume of the convective air currents inside the reflow chamber when processing assemblies with extremely light weight components such as microBGA and flip chip components. It is possible to physically blow these components off of their mounting locations during the reflow process. If it is necessary to lower the convective air currents in the process, thermal profiling must be performed to verify the thermal dynamics of the process are viable.

## Summary

There are differences in process parameters that must be considered when processing electronic assemblies using chip scale packages. When these differences are understood and incorporated into the manufacturing processes, overall product yields should be compatible with assemblies using standard SMT components; however, when using COB components, the incorporation of wire bonding is necessary. The use of chip scale packages on an electronic assembly should be as straight forward as processing with standard SMT components.

ACI offers a specialized 3-day course specific to chip scale manufacturing. If you would like additional information on this course, please contact the EMPF Helpline at 610-362-1320 or via email at [helpline@empf.org](mailto:helpline@empf.org).



COB (chip on board) component mounted to PCB substrate with associated wire bond connections

# IPC-7711 & 7721: Rework and Repair of Electronic Assemblies

The EMPF Learning Center is now offering the IPC's Rework, Repair and Modification Training and Certification Program for Operators. This course provides participants with a hands-on approach to the restoration of electronic assemblies. Certification, which is valid for two years is received upon successful completion of the course.

The ability to customize training based on your company's needs is available. This offers companies the flexibility to select the modules in which their operators receive training. For example, a company that only uses through hole technology, and only wants their workers proficient in rework of through hole components would only want to select Module 1 & 3 of IPC-7711. If a company does not use conformal coating on their assemblies, but needs their operators to be proficient in repair techniques per IPC-7721, they would select Modules 1,7 and 9 of IPC-7721. Operators will be trained in only the selected areas.

The focus of IPC-7711 is on the rework of electronic assemblies. Students will learn and practice the techniques necessary to properly remove through hole and/or surface mount components utilizing the latest tools, materials, and technology available. All component acceptability criteria, based on IPC-A-610C, is reviewed for each module. Upon successful completion, students will obtain IPC Operator Certification in the areas where proficiency has been demonstrated.

Module 1 is a prerequisite for all other modules and is therefore required as part of the training program. Students will be taught general requirements and basic terminology of IPC-7711/21. This module will also teach students basic considerations used in analyzing rework and repair, tool and material considerations, proper handling techniques, and basic cleaning procedures. The satisfactory completion of Module 1 must be done prior to training in any other modules. The duration of Module 1 is one day.

Module 2 is designed to teach students the proper procedure for performing wire splicing. Students will learn to determine the feasibility of repair, the four types of splices used, as well as tinning and soldering considerations. The approximate duration of Module 2 is five hours.

Module 3 concentrates on through hole technology. During this module, students will demonstrate the skills of removing, land preparation, and reinstalling axial-leaded, radial-leaded and multi-leaded components on a PWAs using the continuous vacuum and wicking methods. The duration for Module 3 is one day.

In Module 4, students develop the skills necessary to remove chip and Metal Electrode Face (MELF) components, clean and prepare pads, and reinstall components. The use of various tips and techniques used in Industry is

taught. The duration for Module 4 is approximately six hours.

Removing Single Outline Integrated Circuit (SOIC) and Small Outline Transistor (SOT) components, cleaning and preparing termination areas, and replacing components is covered in Module 5. The duration for Module 5 is approximately six hours.

**IPC-7721 Repair  
of Electronic  
Assemblies:  
Duration 2-3 Days**

The focus of Module 6 is the removal, pad preparation and reinstallation of fine pitched (20-30 mil), multi-leaded J-Leaded and Gull/L wing devices. Students who successfully complete this module will be capable of demonstrating their skill at the advanced level. The approximate duration of Module 6 is one day.

IPC-7721 concentrates on the repair of electronic assemblies. Students will learn the latest techniques used to repair circuits and laminates, including conformal coating/solder resist removal and re-application. Upon successful completion, students will obtain IPC Operator Certification to IPC-7721 in the areas where proficiency is demonstrated. Module 1 is a prerequisite for Modules 7, 8 and 9.

In Module 7 of IPC-7721, students will learn PWB circuit repair. This includes learning the procedures applicable to, and demonstrating the skills used to fix a lifted pad/land repair, install an eyelet into a damaged plated through hole, repair a damaged trace and installation of a surface jumper wire. The duration of Module 7 is one day.

Module 8 focuses on laminate rework and repair. Students will learn the skill of repairing damaged laminate materials using the newest materials and tools available to the electronic manufacturing industry. The duration for Module 8 is six hours.

The procedures and processes for removal and replacement of conformal coating is covered in Module 9. Students will learn about various conformal coating removal techniques including mechanical, thermal and solvent methods. The duration for this Module is five hours.

For more information, please contact the EMPF Helpline at (610) 362-1320. Be sure to ask about multiple student discounts and IPC-7711 & 7721 Training at your facility!

**IPC-7711 & 7721  
Next Course Starts on September 22nd!  
Call the EMPF Helpline (610) 362-1320  
to Enroll! Spaces are going fast!**

# Chemical Testing at the EMPF

## Ion Chromatography

The EMPF performs ion chromatography (IC) analysis on electronic assemblies. This technique is used to measure cleanliness of assemblies, components, and bare board with precision. IC can determine the precise amount of F, Cl, Br, NO<sub>2</sub>, NO<sub>3</sub>, PO<sub>4</sub>, and SO<sub>4</sub>, down to 0.5 mg/cm<sup>2</sup>. A common test method employed by the EMPF is the IPC TM-650 2.3.28. The EMPF has analyzed thousands of assemblies, components, and bare boards using this technique.

## Resistivity of Solvent Extract (ROSE)

The EMPF performs Resistivity of Solvent Extract (ROSE) analysis on electronics assemblies. This technique is used to measure the cleanliness of assemblies, components, and bare boards. Bulk ionics are measured according to their conductivity in solution and referenced to a sodium chloride standard. A common test method employed by the EMPF is the IPC TM-650 2.3.25. The EMPF has analyzed thousand of assemblies, components and bare boards using this technique.

## Fourier-Transform Infrared (FT-IR) Spectroscopy

The EMPF performs FT-IR spectroscopy on a variety of sample types using both transmission and reflective modes as well as FT-IR microscopy on a routine basis. This technique is an excellent tool for examining organic materials such as adhesives, polymers, plastics, etc. The EMPF can obtain FT-IR spectra on surfaces, powders, liquids, and semi-solids. Common test methods include IPC TM-650 2.3.39B and ASTM methods. The spectra that are generated can then be analyzed against thousands of compounds in our spectral database and commercial spectral databases. This library search can be used to identify the compound being sampled.

## Ultraviolet-Visible (UV-Vis) Spectroscopy

The EMPF performs both transmission as well as reflective UV-Vis spectroscopy on liquids and surfaces. UV-Vis spectroscopy is a technique that measures the amount of UV-Vis light absorbed by the sample of interest. Our spectrometer can operate from 230 - 1100 nm and is calibrated against a NIST traceable white reference standard. The EMPF has developed UV-Vis chemometric techniques that are applicable to the electronics and aerospace industries.

## Sequential Electrochemical Reduction Analysis (SERA)

The EMPF has the equipment to analyze the surface oxides and sulfides on metals using sequential electrochemical reduction analysis (SERA). Any metal oxides or sulfides that are present on the surface can be identified and a thickness determined (within 50 angstroms). This technique can be used to identify and differentiate between SnO, SnO<sub>2</sub>, Cu<sub>2</sub>O, CuO<sub>2</sub>, Cu<sub>x</sub>Sn<sub>y</sub>O<sub>z</sub>, Ag<sub>2</sub>S, etc. The EMPF participated in the development of this technology and continues to employ this technology in failure analysis and surface analysis.

## Reduced Oxide Solderability Activation (ROSA)

The EMPF has a process available that removes any metal oxides that may be contaminating a surface, Reduced Oxide Solderability Activation (ROSA). This technique was developed to remove the oxides and sulfides that inhibit solderability such as, tin (II), tin (IV), copper (I), copper (IV), and silver oxides and sulfides. The process is electrochemical and takes place in an aqueous solution. The process is rapid, a typical treatment takes less than one minute. The samples are rinsed in deionized water and are immediately available for processing. The EMPF has reconditioned thousands of components and printed wire boards that have been used in assembly of various military and commercial systems.

## Wetting Balance Testing

Solderability is vital to producing quality electronic assemblies. The EMPF performs quantitative solderability testing as well as qualitative dip-and-look tests. The tests can be performed on leaded components, chip components, wires, and coupons, with the results compared to established evaluation standards such as the J-STD 002 and 003, as well as IEC-68-2-69 among others.

## Optical Microscopy

Optical microscopy at the EMPF is often coupled with digital imaging and analysis. ACI performs such tasks as dimensioning, annotation, archiving, and standardized inspections (e.g. IPC, MIL spec, and JEDEC). The EMPF specializes in bright field illumination and metallic contrast imaging using an inverted stage metallograph. Using various forms of optical microscopy, the EMPF examines components, circuit boards, solder, material microstructure, contamination, defects and anomalies, and other electronic materials at 2 to 1500 times magnification.

## Metallurgy

Using SEM, EDS, optical microscopy, and SERA, EMPF engineers investigate many of the metallurgical issues involved in electronics packaging. Metallurgy is used to study diffusion, intermetallic formation and growth, contamination, morphology, thermodynamics, and kinetics involving a number of electronics related metals, ceramics, composites, and semiconductors. This information can be used to study failure modes.

# Lead Free Soldering for Sustainment

Lead free soldering will influence commercial-off-the-shelf (COTS) implementation and long-term program sustainment. To appreciate the dilemma aerospace manufacturers are under, when considering lead free soldering for program sustainment, one has to understand the environment in which aerospace manufacturers operate. In the aerospace environment, military systems can be in the field for over 30 years. These systems are constantly being upgraded and repaired during their product life cycle. All aerospace hardware is manufactured with SnPb solders. According to the IPC, aerospace electronics represents less than 1% of the total electronics manufacturing market.

The Federal Acquisition Streamlining Act (FASA) of 1994 requires that, to the maximum extent practicable, contract requirements and market research should facilitate use of commercial items. Aerospace electronic manufacturers are qualifying COTS hardware to meet FASA goals. COTS components are currently being manufactured with SnPb.

Component manufacturers, such as Motorola, Tyco, Texas Instruments and Amkor, are converting their production lines to lead free finishes to meet commercial market demands. It is unlikely that component manufacturers will support SnPb component production to meet aerospace rework and repair operations due to aerospace electronics' small market share. It is conceivable that solder manufacturers will stop supporting SnPb solders since the bulk of their market, the commercial market, will be transitioning to lead free solders.

In a commercial electronics environment, commercial manufacturers do not perform rework and repair operations to hardware in the field. Due to the goals stated by the European Union's Waste Electronic and Electrical Equipment (WEEE) Directive and the Japanese Ministry of Industry and Trade Institute (MITI), commercial manufacturers will aggressively convert their production lines to lead free solders. Epson, Hewlett-Packard, Northern Telecom and Panasonic are a few of the commercial manufacturers that are beginning to convert their production line to lead free solders.

## Legislation Status

The European Union's WEEE Directive and the Restriction of Hazardous Substances (RoHS) legislation stipulate that electronic equipment sold to European consumers be lead free as of July 1, 2006. In Asia, MITI called for lead usage to be reduced by 67% by 2005. In the United States, the Environmental Protection Agency's (EPA) Toxic Release Inventory Status requires electronic manufacturers to report lead usage above 100 pounds annually. Therefore, one can conclude that electronics will be lead free in the near future.

## What Do We Know?

For first piece production, it is feasible to manufacture hardware with lead free solders. ACI has successfully implemented several lead free production runs which require hand soldering, wave soldering, and SMT reflow soldering. In general, lead free solders require higher soldering temperatures and thermal profiles, depending upon the alloy (Table 1). Various consortiums have proven that it is feasible to meet high reliability requirements. The Lead Free Components Focus Group and the National Electronics Manufacturing Initiative (NEMI) proved that one could meet IPC Class 2 and Class 3 inspection requirements.

Table 1. Examples of Reflow Soldering Temperatures For Specific Solder Alloys

| Solder Alloy | Peak Reflow Soldering Temperatures |
|--------------|------------------------------------|
| SnPb         | 220°C                              |
| SnAgCu       | 235°C                              |
| SnCu         | 240°C                              |
| SnBi         | 160°C                              |

There are specific challenges to introducing lead free solders in a production environment. Lead free solders do not wet as well as tin lead (SnPb). Aggressive solder fluxes and nitrogen are recommended to improve solderability. Components and board materials are more sensitive to moisture due to lead free solder's higher processing temperatures. From an inspection perspective, because lead free solder joints have a grainy dull appearance, the IPC is revising their visual inspection requirements to compensate for lead free solder joint differences.

## Program Sustainment: What Do We Need To Know?

The process variables for performing rework and repair operations with lead free solders need identification and quantification. It is acknowledged that most lead free alloys have higher soldering temperatures than SnPb. The impact of higher temperatures on the board, components, and the assemblies requires investigation. There are concerns about the quality and reliability of lead free solders that undergo rework and repair processes.

Lead (Pb) contamination presents new process variables. Pb contamination restricts the use of specific families of lead free solders. There is evidence that Pb and Bismuth (Bi) can form an intermetallic with a melting point of 96°C. Therefore, lead free alloys that contain Bi may not be considered for specific applications where intermixing SnPb and Bi lead free solders is possible.

*continued on page 8*

# Lead Free Soldering for Sustainment

(continued from page 7)

AIM Solders documented the possibility that Pb contamination will adversely affect solder joint reliability, based on their metallurgical studies. It is AIM Solders' contention that lead contamination will migrate to the last area of the joint to cool. For a leaded device, this is at the base of the solder joint (see Figure 2). AIM Solders performed tests with Pb-contaminated Tin Silver Copper (SnAgCu) solder paste, based on test method ASTM E606. Pb-contaminated lead free solder pastes failed this test, using 10,000 cycles as a pass / fail criteria (see Table 2).

This contradicts data from the Lead Free Solder Component Focus Group. The Lead Free Solder Components Focus Group manufactured hardware mixing SnPb with lead free components, board finishes, and solder paste. The hardware underwent thermal cycling tests, for up to 2,000 thermal cycles, from -55°C to 125°C. It was determined that the lead free soldered hardware, the SnPb soldered hardware, and mixed hardware had equivalent reliability performance (see Figure 3).

## ACI'S 2003 Lead Free Action Plans

ACI plans to continue research and development activities in lead free solders. ACI is developing a core competency program to document the process variables for performing rework and repair operations with lead free solders. ACI will perform rework and repair operations on hardware mixing lead free and SnPb solders, component finishes, and board finishes. Upon completion, hardware will undergo cross-section analysis to determine the metallurgy of rework solder joints. ACI will perform thermal cycling testing, based on MIL-STD 810F, from -55°C to 125°C to discover the lead free reworked solder joints' reliability.

Another project under consideration is to determine if Pb contamination presents a reliability concern. As with the AIM Solders' experiment, ACI plans to build lead free hardware with advanced electronic packages, using "doped" lead free solder contaminated with a known quantity of Pb. Cross-section analysis will verify the hardware's metallurgy. Thermal cycle testing will determine the solder joint reliability.

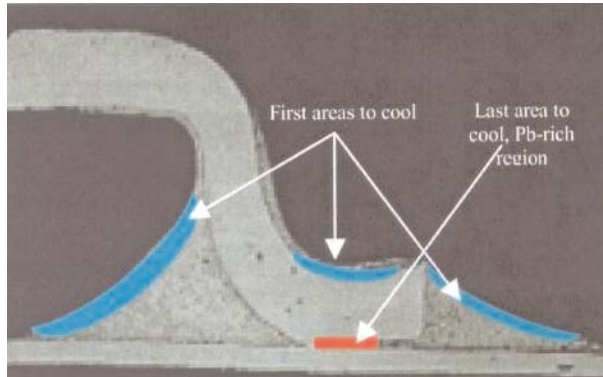


Figure 2. Leaded device cross-section with Pb contamination (Courtesy of AIM Solders)

Table 2. AIM Solders contamination testing results. (Courtesy of AIM Solders)

| Sample                | Cycles To Failure | Results |
|-----------------------|-------------------|---------|
| Tin / Silver / Copper | 13,400            | Pass    |
| 0.5% Contamination    | 6,320             | Fail    |
| 1.0% Contamination    | 3,252             | Fail    |

ACI continues to support the JG-PP Lead Free Solder Team. The JG-PP Lead Free Solder Team will be building lead free solder, using Surface Mount Technology (SMT) and Through Hole Technology. The program will be testing first piece production hardware and rework hardware to simulate sustainment activities. A variety of Environmental Stress Screening (ESS) tests will be performed to assure that lead free solders meet aerospace reliability requirements.

ACI is currently developing a Lead Free Manufacturing course. The course's objective is to introduce the technical variables associated with implementing lead free solders in a production environment. The course will be a hands-on course, utilizing ACI's Demonstration Factory. Participants will be encouraged to bring samples of their hardware to build with lead free solders.

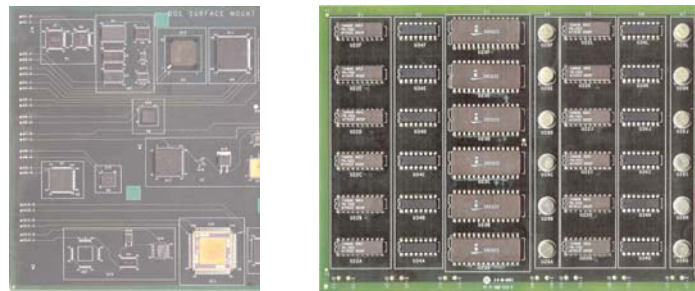


Figure 3. Lead Free Components Focus Group Test Vehicles - SMT test Vehicle (left), PWB Test Vehicle (right)



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Advice!**

**610-362-1320**

# BGA Manufacturing, Inspection and Rework Course at the Electronics Manufacturing Learning Center

## Overview

Manufacturing with Ball Grid Array (BGA) packages generally offers high, first-pass process yields. However, process errors do occur and the likelihood of a solder joint defect (insufficient solder, bridging, solder balling, etc.) under the BGA will require the need to remove and replace the BGA component. Because BGA rework will require the removal of the component, special considerations must be taken into account. For instance, excessive heat or improper removal techniques used during the BGA component removal step has the potential to cause damage to surrounding lands, other components, or the PCB itself. In short, proper rework requires sound practices, proper tools and quality training.

## Who Should Attend

This course is geared towards Manufacturing, Process and Quality Engineers responsible for implementing and/or controlling the BGA application and inspection process. Others who would benefit from this course are the person(s) responsible for training operators and technicians to perform BGA assembly inspection or control the manufacturing process.

## Course Content

### *Introduction to BGAs*

Upon completion of the instruction, the learner will be able to correctly identify the different types of BGA components and the different assembly considerations that must be taken into account when using a specific type of BGA component.

### *BGA Rework Practices*

Upon completion of the instruction, the learner will be able to correctly perform rework procedures on assemblies with BGA components. Proper rework techniques covered will include the development of a removal and replacement profile, component removal, PWB site preparation, solder paste application, component placement and component reattachment.

## Benefits

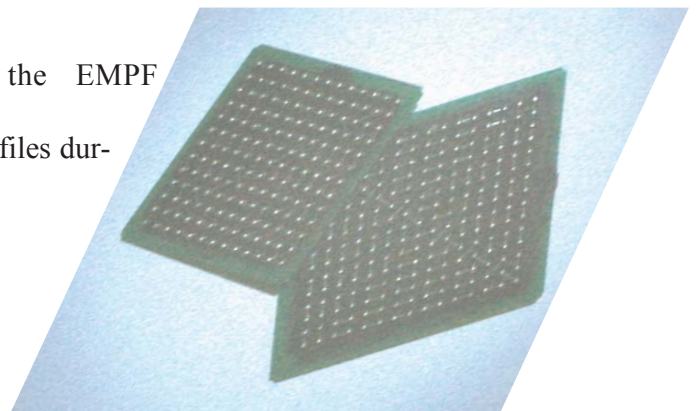
- ◆ Perform individual BGA rework techniques in the EMPF Demonstration Factory
- ◆ Gain experience developing removal and replacement profiles during the hands-on portion of the instruction in the EMPF Demonstration Factory

## Duration

Two days

## Registration

Contact the EMPF Learning Center at:  
phone: 610-362-1320  
email: registrar@empf.org  
www.empf.org



## Scheduled Dates

June 23-24  
August 25-26  
December 1-2

# Industrial Alliance Board

Rapid evolution of electronics technologies, the management process of identifying and maintaining qualified suppliers, and the replacement of obsolete COTS, parts poses a significant problem faced by all companies that do business in the commercial and military sectors.

An Industrial Alliance Board has been formed to collaborate on the critical issue facing today's electronic designers - parts obsolescence. The initial participants in this collaborative teaming effort include a portion of ACI's Industry Advisory Board which includes a large percentage of Defense Contractors along with ACI participating as both a team member and facilitator. This is an industry driven initiative with industry investment and industry commitment to better serve the needs of new and legacy designs.

Alliance members have agreed to collaborate to identify part obsolescence issues, share non-proprietary solutions to part obsolescence issues, define part qualification requirements and arrive at a consensus process leading to the resolution of the part obsolescence problem for the mutual benefit of the collaboration partners.

The Industrial Alliance will ultimately provide significant benefits for the Navy and DoD. The problem in today's commercial electronics market is that the military is experiencing an eroding market share in commercial electronics. As commercial electronics product life cycles continue to decrease, there will be an increase in obsolescence issues. The Industrial Alliance, through its sharing of parts level data, will help abate Navy program risks by providing notification of obsolescence issues while there is time available to implement low-cost and low-risk solutions. Overall, the Navy will see reduced program costs as Alliance members avoid duplicating efforts to resolve diminishing manufacturing source (DMS) issues pertaining to the same part. The Alliance will have the ability to measure real data as Navy programs move forward and report savings on a periodic basis.

A preliminary business case was conducted by ACI in support of the proposed collaborative effort and the result shows that a significant cost benefit would be realized by

all partners. Some of the benefits that the collaborative members would share include:

- ◆ Savings in time and effort based upon use of common part qualification information
- ◆ Savings in time and effort by teaming on component qualification efforts
- ◆ Increased awareness of specific concerns about components and vendors
- ◆ An expected ROI of 1:1 (100%) within one year

|  | Member A  | Member B  | Member C  | Member D  |
|--|---|---|---|---|
| <b>EXAMPLE 1</b><br>AD8170AR<br>Analog Devices-<br>Microcircuit<br>Cost to Qualify \$50K | Needs to be Qualified<br><br>Cost Savings of \$40K & immediate access to data | Qualification Requirements 80% Complete                       | May Fulfill Future Needs<br><br>Immediate access to data      | May Fulfill Future Needs<br><br>Immediate access to data      |
| <b>EXAMPLE 2</b><br>0603CS<br>Coilcraft Inductors (family)<br>Cost to Qualify \$20K      | Needs to be Qualified<br><br>Cost Savings of \$15K<br>4:1 ROI                 | Needs to be Qualified<br><br>Cost Savings of \$15K<br>4:1 ROI | Needs to be Qualified<br><br>Cost Savings of \$15K<br>4:1 ROI | Needs to be Qualified<br><br>Cost Savings of \$15K<br>4:1 ROI |

Example benefits of qualifying components.

By collecting information on obsolete part issues from each alliance member and then evaluating the data for common concerns or configuration item applications, a set of requirements can be established that are common among Alliance member businesses and, when satisfied, will lead to a mutually beneficial solution. By identifying those part obsolescence issues which are common among members, and then agreeing to collaboratively find a solution through the identification or qualification of suitable replacements, significant cost savings can be realized. The following scenarios are examples:

*Scenario One-* If an Alliance member identifies a component that they have a requirement to qualify, and another Alliance member has already conducted the qualification test for that particular component, then an immediate benefit is realized through the sharing of that information among the members. The table above illustrates examples of one member needing a COTS component qualified and another member having already qualified that component resulting in an immediate benefit to the membership.

*Scenario Two-* If more than one of the Alliance members requires component qualification information or addition-

## Industrial Alliance Board *(continued from previous page)*

al reliability testing for a particular COTS component, then the teaming effort will reduce the qualification cost by eliminating redundant efforts to individually repeat the same test process. In this case significant benefits can be realized by qualifying a family of components.

The objective of this effort is to create a collective knowledge base of component obsolescence and qualification information and reliability data at a central location that facilitates easy access by members. Benefits include:

- ◆ Cost-savings through elimination of redundant efforts
- ◆ Reduced technical risk by using "tried and true" part selection and qualification methodology
- ◆ Reduced schedule risk on development and production programs
- ◆ Enhanced performance in the maintenance
- ◆ A ROI of 1:1 (100%) within one year
- ◆ Increased opportunities and reduced costs to perform planned technology insertions on new and existing programs
- ◆ Reduced cycle time in the resolution of part obsolescence issues and in the selection of parts for new designs and design upgrades

The selected area of concentration is the issue of part obsolescence in new and legacy designs. Specifically, information from the following component management areas will be collected, evaluated and then shared amongst the team:

**Qualification data** - Goal is to establish a repository of test data resulting from qualification testing of Commercial Off-The-Shelf (COTS) components supplied by non-Qualified Manufacturing Line (QML) vendors. Each Alliance member will populate this database with qualification test data pertaining to specific parts. Qualification testing of parts will then proceed under a process which has a collective set of requirements defined as common by the Alliance members, thereby eliminating redundancy in effort. The data will be obtained via an agreed-to test methodology template.

**Obsolescence data** - Goal is to identify and prioritize commonly used components that have obsolescence issues. Subsequently, this task calls for the identification of suitable replacements by sharing non-recurring re-design engineering information or part substitution data among members.

A feasibility survey of existing component databases was conducted to determine if any duplication of effort exists and also how the resources could compliment that of the Alliance teaming. Organizations such as DMEA, DMSMS, GIDEP, IAC, SPANS, and STACK each were not found to be a duplication of effort with what the Alliance is seeking to accomplish.

### DMEA

The Defense Microelectronics Activity (DMEA) was established by the Department of Defense to provide a broad spectrum of microelectronics services to the DoD. They are located in Sacramento, California and have approximately 3,500 employees.

Their capabilities include looking at specific obsolete components and developing die to reverse engineering solutions. For example, if they have a component with a

|               | Qualification Data | Reliability Data | Obsolescence Information | Obsolescence Solutions | Component Supplier Audits | Joint Company Standard | Failure Analysis Information |
|---------------|--------------------|------------------|--------------------------|------------------------|---------------------------|------------------------|------------------------------|
| Ind. Alliance | ✓                  | ✓                | ✓                        | ✓                      |                           | ✓                      | ✓                            |
| DMEA          | -                  | ✓                | -                        | ✓                      |                           |                        |                              |
| DTC/DMSMS     |                    |                  | ✓                        | ✓                      |                           |                        |                              |
| GIDEP         |                    | ✓                | ✓                        | ✓                      |                           |                        | ✓                            |
| IAC/RAC       | ✓                  |                  | ✓                        | ✓                      |                           |                        | ✓                            |
| SPANS         |                    |                  | ✓                        |                        |                           |                        |                              |
| STACK         |                    |                  | ✓                        |                        | ✓                         | ✓                      |                              |

Comparison of existing databases.

specific I/O, they will design and build a replacement that has the same I/O.

They may indirectly have some qualification/reliability information, but they do not formally house these types of information as a service like that which ACI is providing in this effort.

### DTC/DMSMS

The Diminishing Manufacturing Sources Technology Center (DMS/DTC) provides in-depth DMS management and solutions. This is a Navy center that provides DMS and Material Shortages (DMSMS) information. Jack McDermott of ARINC Incorporated is the Joint STARS USAF/DoD Teaming Co-chairman and states,

*continued on page 12*

## Industrial Alliance Board *(continued from page 11)*

"The answer of are we duplicating efforts, the answer is I do not believe that we are."

From a teaming perspective, DMSMS finds commonality among DoD platforms and then tries to find common solutions. 83% of problems are microelectronics issues.

The teaming efforts are focused on government, industry, and suppliers partnering to provide solutions to situations caused by diminishing manufacturing sources and material shortages. The partnership consists of networking among the group to develop/identify common solutions.

### **GIDEP**

The Defense Technical Information Center runs the Government-Industry Data Exchange Program (GIDEP). GIDEP is a repository of data and information across the DoD and industry.

GIDEP is a cooperative activity between government and industry participants seeking to reduce or eliminate expenditures of resources by sharing technical information essential during research, design, development, production, and operational phases of the life cycle of systems, facilities, and equipment. Since GIDEP's inception, participants have reported over \$1 billion in prevention of unplanned expenditures.

### **DTIC/IAC/RAC**

The Defense Technical Information Center (DTIC) sponsors Information Analysis Centers (IACs) that support highly specialized technical areas. The Reliability Analysis Center (RAC) is run by the IIT Research Institute. They primarily collect, analyze, and store reliability data. This allows them to provide insight into potential reliability improvement areas.

They also maintain the Data Sharing Consortium that is an older style database that has component screening, quali-

fication, test and field performance data that has been used primarily by commercial subcontractors.

### **SPANS**

Supply Chain Practices for Affordable Navy Systems (SPANS) assists the Office of Naval Research (ONR). The SPANS approach is to integrate and optimize large supply chain issues relating to the building of naval vessels and equipment.

In general, SPANS seeks to improve supply chain practices for Navy systems by finding new, State-of-the-Art (SOA) practices and technologies and by conducting sufficient development work so that they can be piloted and deployed into a Navy weapon system.

### **Stack International**

Stack International is a group of multinational, independent electronic equipment manufacturers who share experience, "know-how," and workload, and cooperate closely in pre-competitive areas with each other and their suppliers to reduce individual members' cost and risk of component ownership.

ACI shall facilitate the storage of, and access to, relevant information pertaining to the above two areas of concern. This task will be completed most effectively through the solicitation of the Alliance member requirements, and then by conducting a trade study to arrive at a database infrastructure that adequately addresses Alliance member needs. Once the database is established, then cost benefits can be realized via component data sharing.

If you would like additional information about the Industrial Alliance Board, please contact the EMPF Helpline at 610-362-1320.



**For complimentary electronics  
manufacturing support,  
call the Helpline!**

**610-362-1320**

# Manufacturer's Corner

## Hepco



At the EMPF, working with one-of-a-kind (or limited use) Ball Grid Array (BGA) devices is a common occurrence. The EMPF is frequently called upon to assist in BGA repair. One tool the EMPF uses is the Hepco Model 9000-1 BGA Solder Sphere Replacement System to repair damaged BGA devices. The EMPF utilizes this unit in its training classes, performing demonstrations in the Demonstration Factory, prototyping and assisting original equipment manufacturers (OEM) in repairing BGA devices. The Hepco Model 9000 is used on military as well as commercial BGA devices.

The Hepco Model 9000 operates using a self-contained vacuum system to secure the BGA component while transferring the desired pattern of solder spheres in a full array. Alignment is achieved through precision pins and specific tooling for ease of use, repeatability, and accuracy in sphere placement. Its repeatable process control will insure co-planarity and uniformity of the sphere's placement. The unit will accommodate virtually all BGA layouts and sphere sizes. A self-contained system, no additional air/vacuum is required.

During the last few years, BGA usage has increased dramatically among OEM. This is due, in part, to the increased complexity of electronics circuitry and higher demands placed on the industry by commercial and consumer customers.

The technology and process knowledge to effectively and efficiently repair BGA devices exists. An added attraction for BGA packages is that this technology is compatible with existing surface mount technology (SMT) assembly processes and equipment, so rework is fairly simple.

### Preparing PCBs and Packages for Rework

Both the printed circuit board (PCB) and surface mount technology (SMT) devices, to be removed, are capable of absorbing moisture from ambient air. This may cause internal expansion and damage to the PCB and/or device during heating to the de-soldering temperature. Therefore, it is recommended to always bake PCBs and devices prior to any rework.

The recommended temperature depends on the maximum temperature that the devices on the PCB can withstand

without damage. Generally, the allowed temperature is between 50°C and 80°C. Furthermore, a higher baking temperature requires a shorter bake-time.

- At 50°C the recommended bake time is 48 hours.
- At 60°C the recommended bake time is 36 hours.
- At 70°C the recommended bake time is 24 hours.
- At 80°C the recommended bake time is 20 hours.



Hepco Model 9000

### Overheating & Warpage (Coplanarity)

PCB material is a mixture of fiberglass and resin, with copper tracks and vias, as well as a solder-resist coating on top. All of these materials expand at different rates during heating. If heating is unevenly applied, different sections of the same material will expand at different rates. This stress can lead to permanent distortion of the material. Warpage, as it is called, is usually a result of the buckling of the PCB. Warpage may make it impossible to solder a new device in the position where rework occurred, so the PCB is a reject.

In the case of BGA, where the heating of the balls in the center of the underside of the device is much slower, applying all the heat via the top of the board is not the

*continued on page 14*

## Manufacturer's Corner - Hepco (continued from page 13)

most ideal method. The application of heat in this manner would heat the PCB in that area too much, thereby causing warpage. Therefore, the PCB must be heated from the underside to a given temperature (depending on the board properties), preferably 80-145°C.

During the process of component removal, a component can be damaged. For example, BGA solder spheres can be damaged and the expensive device destroyed.

### BGA Re-balling Procedures:

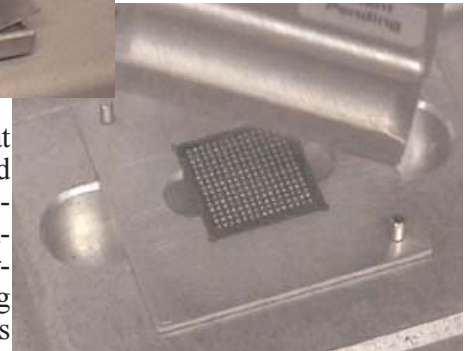
- ◆ Place the component in the alignment plate
- ◆ Turn on the vacuum
- ◆ Remove residual solder and/or contaminants. (Always remove excess solder and clean the device. This can be done using solder braid. Then, clean off any dirty flux with flux cleaner)
- ◆ Print the flux on the component using the appropriate stencil
- ◆ Load the wand with solder spheres using the vacuum pick-up
- ◆ Align the wand using tooling pins



- ◆ Depress the foot pedal to release the full array of spheres



- ◆ Lift the block
- ◆ Remove the component from the carrier
- ◆ Reflow the part using the proper temperature profile.



Restoring BGA's that have been damaged during the manufacturing process or end-user handling, by performing a reballing process that restores the device to equivalent-to-new condition, can be a cost-effective process. This reballing process will provide substantial cost savings to the customer because it eliminates the high replacement cost for expensive BGA devices.

If you would like to see a demonstration of the Hepco Model 9000-1 BGA Solder Sphere Placement System, please call Jeff Stong at the EMPF. He can be reached at 610-362-1200 Extension 224 or at [jstong@aciusa.org](mailto:jstong@aciusa.org).

**Register for the Design for Manufacturing  
course offered August 18-19 at the  
Electronics Manufacturing Learning Center.**

**Enroll now!**

**610-362-1320**

**[registrar@aciusa.org](mailto:registrar@aciusa.org)**

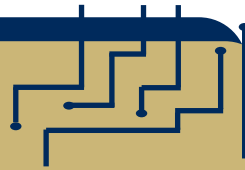




Electronics Manufacturing Productivity Facility

TECH TIPS...

Removing Conformal Coatings



Cut here and save!

All conformal coatings can be removed if the assembly in question requires minor or isolated repair/rework. There are a number of removal methods and they include solvent stripping, thermal degradation, micro-abrasive removal, mechanical removal, excimer laser and plasma stripping.

It is common to use a combination of procedures but it is critical that the coating manufacturer be contacted for the best possible method(s). Regardless of the procedure, it is critical that the affected area be rinsed with a chemically neutral material such as deionized water. Remaining residues can contain halides or other corrosive agents which can cause electrical failures if they are not removed.

**Conformal Coating Removal**

To determine the coating removal procedure, the coating first must be identified. Commonly, the type of coating is unknown. As a result, IPC has provided a general decision tree to coating classification (see Figure 1 on the following page). It should be clear that this procedure provides only general coating classification and not specific commercial identification. A coating's characteristics will affect the type of removal method. Although most conformal coatings are soluble in solvents, compatibility with the PWB and its components must be determined. Tables 1 and 2 provide general characteristics of the five major coatings and ranks the removal procedures (in ascending order) to use for various coating types.

**Special Note**

Removal should be done carefully and slowly during mechanical grinding, blasting, and/or abrading, especially when removing coatings which have an opaque appearance as components can be easily damaged. With thermal removal applications, IPC recommends testing the coating with a dull thermal parting device. If the coating becomes fluid or gums up, the temperature is too hot or the coating is not suitable for thermal removal. Most conformal coatings are soluble in solvents but, as mentioned earlier, compatibility with the PWB and its components must be determined. IPC states that "PBAs should not be immersed in harsh solvents"<sup>1</sup> and recommends isopropyl alcohol be used unless stated otherwise.

Table 1. Conformal Coating Characteristics courtesy of IPC

| Characteristics           | Conformal Coating Type |         |              |                |              |
|---------------------------|------------------------|---------|--------------|----------------|--------------|
|                           | Epoxy                  | Acrylic | Polyurethane | Silicone Resin | Paraxylylene |
| Hard                      | X                      |         | X            |                | X            |
| Medium Hard               |                        | X       | X            |                |              |
| Soft                      |                        |         | X            | X              |              |
| Heat Reaction             | X                      | X       | X            |                |              |
| Surface Bond- Very Strong | X                      |         |              | X              | X            |
| Surface Bond Strong       |                        | X       |              | X              |              |
| Surface Bond- Medium      |                        |         | X            | X              |              |
| Surface Bond-Light        |                        |         |              | X              |              |
| Solvent Reaction          |                        | X       |              |                |              |
| Non-porous Surface        | X                      | X       | X            |                | X            |
| Glossy Surface            | X                      | X       | X            |                |              |
| Semi-Glossy Surface       | X                      |         |              | X              |              |
| Dull Surface              |                        |         |              |                | X            |
| Rubbery Surface           |                        |         |              | X              |              |
| Brittle                   | X                      | X       |              |                |              |
| Chips                     | X                      | X       |              |                |              |
| Peels and Flakes          |                        | X       | X            |                | X            |
| Stretches                 |                        |         | X            | X              |              |
| Scratch, Dent, Bend, Tear |                        |         | X            | X              | X            |

Table 2. Conformal Coating Removal Methods courtesy of IPC

| Conformal Coating | Removal Method |         |         |                   |                |
|-------------------|----------------|---------|---------|-------------------|----------------|
|                   | Solvent        | Peeling | Thermal | Grinding Scraping | Micro Blasting |
| Paraxylylene      |                |         | 1       | 2                 | 3              |
| Epoxy             |                |         | 1       | 2                 | 3              |
| Acrylic           | 1              |         | 2       | 3                 | 4              |
| Polyurethane      | 3              |         | 1       | 2                 | 4              |
| Silicone Thin     | 1              |         | 2       | 3                 | 4              |
| Silicone Thick    |                | 1       |         | 2                 |                |

The detailed procedures for each technique can be found in IPC 7711 2.4.2 through 2.4.6 "Rework of Electronic Assemblies, Coating Removal" (sections on Solvent Method, Peeling Method, Thermal Method, Grinding/Scraping Method, and Micro Blasting Method, respectively).

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# Removing Conformal Coatings (continued)

Table 3: Removal Procedures

|                                     | Where is it used?  | How does it work?  | Problems associated w/use.  |
|-------------------------------------|--|--|---|
| <b>Solvent stripping</b>            | Will be coating dependent as some coatings do not respond to most common solvents. Consult manufacturer guidelines.          | Upon application of solvent coating will swell reducing adhesion allowing for removal through mechanical means (i.e. scraping, etc...) | Solvent can spread further than required. Incompatibility with PWA and components (Needs to be determined first).   |
| <b>Mechanical abrasion blasting</b> | Harder materials are best suited for blasting or grinding. Softer materials are best suited for brushing or cutting.         | A secondary material will contact the coating surface and either grind, blast or cut into the coating.                                 | High potential for damage from ESD. As a result, it is important to ground equipment and user. The removal must be done slowly as not to damage components especially with coatings which are opaque. |
| <b>Thermal degradation</b>          | Localized heating of the area in question w/hot knife or soldering iron.   | Melting of the coating or thermally degrading of the coating layer. Works with the major classes                                       | Damage to board substrate or temperature sensitive components.  |
| <b>Excimer laser</b>                | Similar to thermal methods but using a laser as the heat source. The laser provides better control and smaller area removal. | The coating is melted and either vaporized or degraded.  | As with the Thermal methods damage to the board and components is possible but not as likely.   |
| <b>Plasma</b>                       | Specifically for removal of Paraxylene.  | The coating is removed through the etching or reaction of thermally excited gaseous ions with the coating layer.                       | Like the Laser and Thermal techniques there is potential for board damage.  |

In addition, along with courses relating to conformal coatings, the EMPF offers the following certification course: IPC-7711/7721 "Rework, Repair and Modification of Printed Boards and Electronic Assemblies (Operator)".

## References

<sup>1</sup>IPC 7711 2.4.1 "Rework of Electronic Assemblies, Coating Removal, Identification of Conformal Coating"; February 1998



**Contact the Electronics Manufacturing Helpline!**

**610-362-1320**

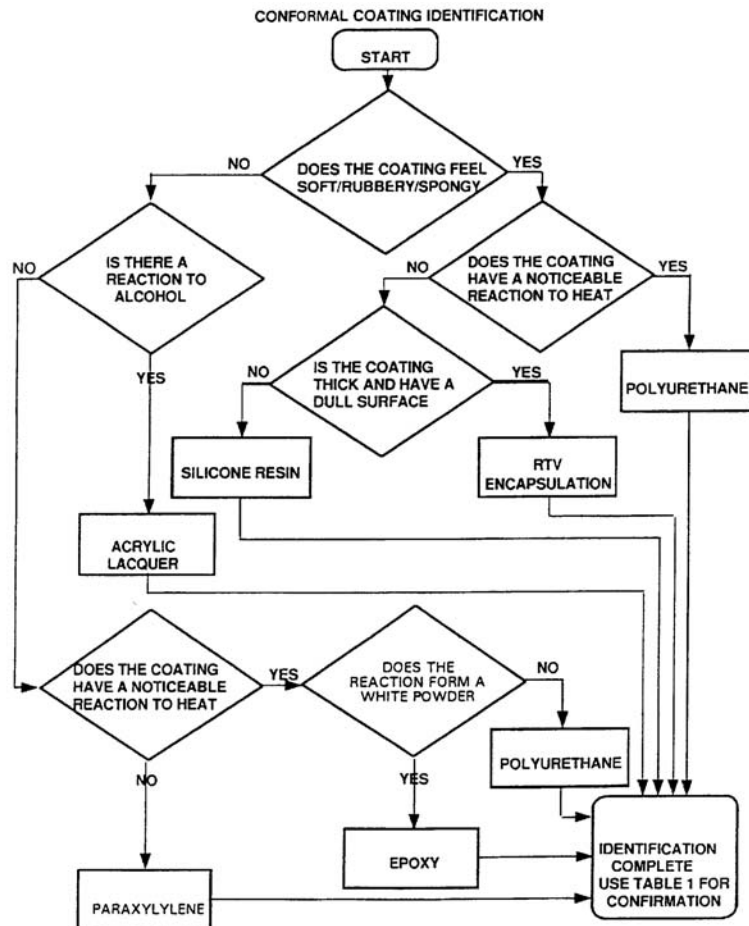


Figure 1: Decision Tree for Removal of Conformal Coating courtesy of IPC

# J-STD-001 and IPC-A-610 Compared

**I**PC-A-610 or IPC J-STD-001. Why two electronic assembly acceptance standards? What is Worker Proficiency Certification? How is the J-STD-001 Operator Proficiency Certification different? This article will answer these questions.

The IPC relies on industry volunteers, working in committees, to develop the standards. The committees are apportioned into eight major function categories. One of these, the Product Assurance Committee, has responsibility for the technical content of the IPC-A-610 standard through its IPC-A-610 Task Group.

The IPC-A-610 presents acceptance requirements for the manufacture of electronic assemblies. Essentially, the IPC-A-610 is a book of pictures and illustrations portraying acceptance criteria that reflect the requirements of other standards and specifications.

Historically, electronic assembly standards did contain more comprehensive and tutorial information relating to principles and techniques. One consequence, the standardization of methods, resulted in conflicts because process methods changed faster than the standards.

The Assembly and Joining Process Committee, with the EIA Soldering Technology Committee, developed the joint standard, J-STD-001: Requirements for Soldered Electrical and Electronic Assemblies. The IPC committee deals with automatic component placement, insertion, handling, attachment and joining techniques, as well as the cleaning operation prior to coating and encapsulation. The two documents will probably not be merged. The activities of the committees are different. We have the IPC-A-610, a picture book that provides clarification and definition to the end item requirements that should result from the use of materials, processes and design (by extension) requirements described in the J-STD-001.

Both the IPC-A-610 and J-STD-001 can be referenced on contracts to define end item acceptance. The IPC-A-610 preceded the J-STD-001 by a couple of years, therefore, the 610 was the more frequently referenced. However, the Department of Defense (DoD) adopted Handbook 001B and then J-STD-001C, consequently J-STD-001 is being referenced on many DoD High Reliability con-

tracts. In practice, the requirements of the two standards are well harmonized, but there are significant differences.

Consider this excerpt from J-STD-001 Section 3 General Requirements: The soldering operations, equipment, and conditions described in this document are based on electrical / electronic circuits designed and fabricated in accordance with the specifications listed in table 3-1.

The table, courtesy of the IPC, references Design Standards and Fabrication Specifications. These govern many characteristics of the boards. Paragraph 3.1.2 states: "Mounting and soldering requirements for specialized processes and /or technologies not specified herein SHALL be performed in accordance with documented procedures which are available for review."

Compare the above requirements with the following guidelines from the IPC-A-610. Paragraph 1.2 (Purpose) states: "The visual standards in this document reflect the requirements of existing IPC and other applicable specifications. In order for the user to apply and use the content of this document, the assembly/product should comply with other existing IPC requirements, such as IPC-

| Board Type           | Design Specification | Fabrication Specification |
|----------------------|----------------------|---------------------------|
| Generic Requirements | IPC-2221             | IPC-6011                  |
| Rigid Printed Boards | IPC-2222             | IPC-6012                  |
| Flexible Circuits    | IPC-2223             | IPC-6013                  |
| Rigid Flex Board     | IPC-2223             | IPC-6013                  |

Table 3-1 Design and Fabrication Specification

SM-782, IPC-2221, IPC-6011 and IPC-A-600. If the assembly does not comply with these or equivalent requirements, then the acceptance criteria needs to be defined between the customer and supplier."

We see in the paragraphs above a significant difference between the two standards. In the case of the J-

STD, referenced standards extend the standard. In the case of the 610, referenced standards are provided for reference, unless specifically identified as an extension of the standard.

Quoting from J-STD-001, "Section 5.2 Solderability: Electronic/mechanical components and wires to be soldered SHALL meet the requirements of J-STD-002 or equivalent, and printed boards SHALL meet the requirements of J-STD-003 or equivalent. When a pre-tinning and inspection operation is performed as part of the documented assembly process, that operation may be used in lieu of solderability testing." The IPC-A-610 is silent on the subject of solderability testing and dedicates one paragraph to "process control methods." These differ-

*continued on page 18*

# J-STD-001 and IPC-A-610 Compared

*(Continued from page 17)*

ences might go unnoticed, until something goes wrong in your customer supplier relationship.

Let's take a look at the training programs. The IPC-A-610C Worker Proficiency training will provide your company and employees with skills in discriminating acceptable conditions from defect conditions as defined by the IPC-A-610 Standard. The 610 training focuses on process results, defining what is acceptable and what is not at the end item. The operator level program requires about 24 hours of classroom instruction. Class A Instructor certification requires about 40 hours of classroom time. There is no hands-on skills component to the IPC-A-610 programs.

The IPC J-STD-001C Operator Proficiency training provides a modular approach to certification training. The J-STD program is a combination of lecture and hands on soldering skills training. There are five modules, with each module requiring about eight hours to complete. Module One is required, a prerequisite overview of the requirements of the standard. There is no hands-on component to Module One and proficiency is demonstrated through a closed book test. The remaining four modules all require operators to demonstrate proficiency in sol-

dering skills, defect recognition and in understanding the process requirements of the standard. Class A Instructor Certification is not modular. Instructors must demonstrate soldering skills, defect recognition and pass a comprehensive test covering the requirements of all five modules.

The J-STD's modular approach to training can also save money. When a smaller company has a few workers with specialized skills that parallel the content of the existing modules. The 610 program is appropriate for companies with specialized inspectors and for companies doing final assembly only, or in large Original Equipment Manufacturers (OEMs) and contract manufacturers.

For more information on certification training call the EMPF Helpline at (610) 362-1320.

## Electronics Manufacturing Learning Center

### IPC J-STD-001 Instructor Certification

July 14-18  
September 8-12  
October 27-31

### IPC J-STD-001 Instructor Re-Certification

August 18-19  
November 17-18  
December 8-9

*For more information or to register,  
please contact the registrar:  
registrar@empf.org or  
610-362-1320*

## Electronics Manufacturing Learning Center

### IPC-A-610 Instructor Certification

July 21-25  
September 15-19  
November 3-7

### IPC-A-610 Instructor Re-Certification

August 21-22  
November 20-21  
December 11-12

*For more information or to register,  
please contact the registrar:  
registrar@empf.org or  
610-362-1320*

## Ask the EMPF Helpline!

**CUSTOMER ISSUE:** The EMPF Helpline received a call from an EMS (electronic manufacturing services) provider who was experiencing failures on PWAs (printed wiring assemblies) that were in a large number of automobiles after only one year in the field.

The suspected source of the open circuits was 0402 ceramic chip resistors that had small black dots near the electrode terminations. They were failing in an electrically open condition. Surprisingly, electronics manufacturing processes had not changed. Only the environment had changed as the board was relocated from within the interior of the vehicle to under the hood.

Silver is quite reactive and tarnishes easily in the presence of sulfur. A household example is unused silverware on display, the dark tarnish is primarily composed of sulfur. Energy Dispersive Spectroscopy (EDS) determined that the chip resistors with small visible corrosion spots on the exterior of the component contained both silver (Ag) and sulfur (S). Through examination of their relative atomic percentages, it was suspected to be a non-conductive  $Ag_2S$  phase.

The failed resistors were then cross-sectioned from the assembly, and subjected, along with a series of new resistors from commercial vendors, to root-cause analysis tests:

- ♦ Cross-sectioning/SEM (Scanning Electron Microscope) analysis was used to look for cracks in the solder joints.
- ♦ EDS Energy Dispersive X-Ray analysis and elemental mapping was used to determine the presence of unwanted chemical species at the resistor contacts.

No indication of cracked solder joints or poor workmanship was found. However, sulfur contamination and the presence of  $Ag_2S$ , accounting for the electrical opens, were identified.

Upon confirmation of sulfur contamination as the root cause for the opens, samples of the product packaging plas-

tic components and gaskets were submitted for Fourier Transform Infrared Spectroscopy (FTIR) to determine candidate sources for the sulfur contamination.

### Results

Figure 1 reveals a plan view of nodules coinciding with the electrical open failure of a chip resistor in the product.



Figure 1. Nodules of corrosion product on failed resistor.

Figure 2 is an elemental analysis created at ACI using the EDAX capability of the SEM (Scanning Electron Microscope). The predominantly silver layer beneath the electrode contact of the chip resistor on a failed open resistor is shown. There is substantial S (sulfur) contamination in the silver (Ag) layer. The

material structure is identical to the material of the nodules noted near the electrode contacts of the failed resistor (see Figure 1). This material is reasoned to be  $Ag_2S$ , and is non-conductive. This is the apparent mechanism causing the electrical open failures of the resistors.

The next step was to determine likely candidates for a source of the contaminating sulfur. Several samples of plastic materials of the case, cover, and various gaskets used in the final product assembly in close proximity to the failed PWA were submitted by the customer to ACI for analysis.

FTIR (Fourier Transform InfraRed) scans of the plastic components and rubber gasket material were run at ACI.

There was a definite concentration of sulfur present in the gasket material that potentially was the source of the sulfur causing the failure. The plastics used in the container were confirmed by FTIR to be free of sulfur.

### Recommendations

Electrode terminations for ceramic chip resistors contain both silver and a minor amount of palladium (Pd) the latter serves to protect against corrosion mechanisms involving sulfur. The Pd amount present in the resistors was questioned, as well as the ultimate source of the sulfur. Use of resistors having higher Pd (3% or above) concentrations in the Ag layer under the terminal metallization on the resistors was recommended as a general precautionary measure. Furthermore, ACI recommended minimizing the use of rubber gaskets containing sulfur for this situation.

Consultation with ACI partner Cookson Electronics revealed that Parylene conformal coating although expensive, is expected to be very resistant to any sulfur contamination ingress. The natural tendency of sulfur is to be in a cluster of eight sulfur atoms per cluster, and the Parylene is known to have much smaller porosity structure.

Satisfied with these results and recommendations, the customer elected to change the resistors to those showing a more sulfur impervious boundary layer, and to change to sulfur free rubber gaskets for the products wherever possible. For this application, the cost for Parylene conformal coating, although expected to add additional protection, is prohibitively expensive.

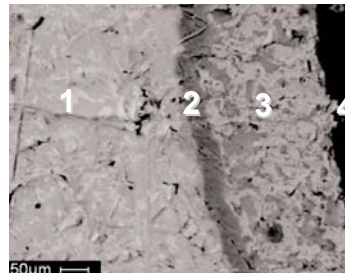


Figure 2. Backscatter SEM image of failed resistor component. Region 1 is SnPb solder, region 2 is Nickel diffusion barrier, and region 3 is predominantly  $Ag_2S$  non-conductive sulfur contaminated Ag layer. Region 4 is the resistor body.

or complimentary Electronics Manufacturing support, call the EMPF Helpline 610.362.1320

# American Competitiveness Institute - 2003 EMLC COURSE SCHEDULE

## Electronics Manufacturing

### BOOT CAMP A - Week 1

August 4-8  
October 13-17

### BOOT CAMP B - Week 2

August 11-15  
October 20-24

## Skills

### SMT Manufacturing

June 16-20  
October 6-10

### BGA Manufacturing, Inspection & Rework

June 23-24  
August 25-26  
December 1-2

### **NEW!** Chip Scale Manufacturing

September 10-12  
November 5-7

## Certifications/Recertifications

### IPC J-STD-001 Instructor Certification

July 14-18  
September 8-12  
October 27-31

### IPC J-STD-001 Instructor Recertification

August 18-19  
November 17-18  
December 8-9

### IPC-A-610 Instructor Certification

July 21-25  
September 15-19  
November 3-7

### IPC-A-610 Instructor Recertification

August 21-22  
November 20-21  
December 11-12

### IPC Challenge

May 21  
August 20  
November 19  
December 10

### IPC-A-600 Acceptability of Printed Boards Instructor Certification

October 8-10

**NEW!**

**IPC-7711/7721 Rework, Repair and Modification of Printed Boards and Electronic Assemblies (Operator)**  
September 22 - October 3

## Continuing Professional Advancement in Electronics Manufacturing

**NEW!**

### Design for Manufacturability

August 18-19  
November 17-18

### Failure Analysis and Reliability Testing

September 24-26

### Characteristic Properties of Materials

August 27-29

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org



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