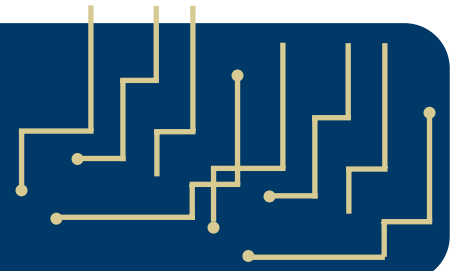


empfasis



A publication of the National Electronics Manufacturing Center of Excellence

October 2001



American Competitiveness Institute
One International Plaza
Suite 600

Philadelphia, PA 19113

(610) 362-1200 • FAX: (610) 362-1290

HELPLINE: (610) 362-1320

WEBSITE: www.empf.org

The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

EMPF Director

Michael D. Frederickson
mfrederickson@aciusa.org

EMPF Technical Director

Jerry McGowan
jmcgowan@aciusa.org

In This Issue

Page 1: **ACI Establishes an Alliance for Collaborative Electronics Manufacturing Technology Applied R&D**

Page 1: Technical Applications Guideline Handbook

Page 2: EMMA

Page 3: Advanced Packaging Assembly Process Overview

Page 6: 2002 EMLC Schedule by Course

Page 7: Tech Tips: Circuit Board Repair

Page 9: Manufacturer's Corner: Electrovert Bravo 4050 Reflow Oven

Page 11: Ask the EMPF Helpline!

Page 12: EMLC Course Schedule



Office of Naval Research

Director of Manufacturing Technology

Steve Linder

linderst@onr.navy.mil
(703) 696-8482

ONR Program Officer

John Olewnik
olewnij@onr.navy.mil
(215) 697-9526



ACI Establishes an Alliance for Collaborative Electronics Manufacturing Technology Applied R&D

The American Competitiveness Institute (ACI) has established an industrial alliance for collaborative electronics manufacturing technology applied research and development. The objective of the alliance is to facilitate the collaboration among leading companies in the manufacturing of electronic products and related services. The concept allows companies to collaborate on pre-competitive and non-competitive common manufacturing issues - creating a reduction in internal research and development expenditures and an improvement in internal capabilities centered around these issues. The end result is improved capability and more competitive positioning for those that participate.

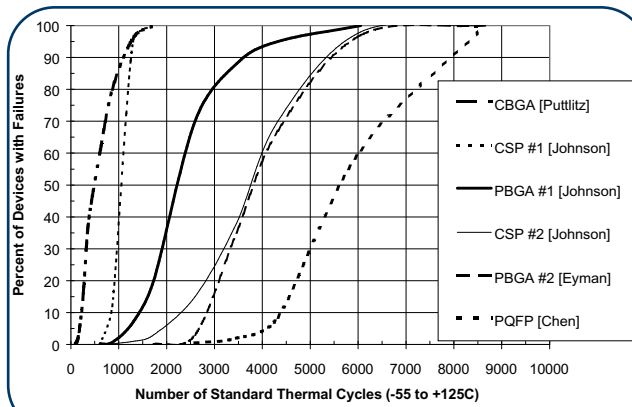
Results from the collaboration will have a definitive impact on the factory floor within a 12-18 month window.

Current projects being investigated include the consolidation and collaboration of part qualification testing for military space applications.

This effort maximizes the benefits of collaboration efficiently and strategically using internal resources provided by ACI and each participating member, and by using company contributions toward technical projects associated with specific areas of collaboration. The activities involved in this industrial collaboration include identifying areas of collaboration, prioritizing and grouping topics, developing project plans, facilitating the execution of projects, and demonstrating and ensuring the transfer of results to the participating industrial members. Collaborating companies include Boeing, Honeywell, ITT, Raytheon and Rockwell Collins. For more information, contact (610) 362-1320.

Technical Applications Guideline (TAG) Handbook

Based on test information collected from the Electronic Miniaturization Missile Applications (EMMA) Program ACI has developed a Technical Applications Guideline (TAG) Handbook. The handbook's benefit to the user is that it provides a user-friendly roadmap to specific COTS components that have been tested and



Example of reliability data found in the TAG handbook

passed (or in some cases not passed) MIL environments. It also provides information in easy to follow format on SMT manufacturing processes and the reliability of these electronics assembly processes. The handbook's focus is to be a source of technical information for individuals interested in implementing Advanced Electronic

continued on p. 10

EMMA

Many advances in microcircuit packaging technologies have enabled revolutionary leaps in the miniaturization of commercial electronics. Electronic packaging, such as Micro Ball Grid Array and Chip Scale Packaging (CSP), are enabling a number of miniaturized electronic technologies to become available to consumers at low cost. Although these commercial-off-the-shelf (COTS) technologies have been shown to be effective in consumer electronics products, these technologies represent a risk for high reliability applications. Very little research has been done to determine the viability of implementing these technologies in military and aerospace systems, where high reliability in harsh operating environments is required.

The Electronic Miniaturization for Missile Applications (EMMA) Program was initiated to introduce commercial advanced electronic packaging to an existing guided missile design. The program's mission was to identify, evaluate, and mitigate the risks associated with the integration of these packaging technologies. The program, sponsored by the United States Navy and Army ManTech programs was initiated in March, 1999, with its completion in December, 2001.

The program's demonstration vehicle was the standard missile (Figure 1). The current Standard Missile Electronics Assembly Unit (EAU) uses twenty year old technology on several of its systems. It requires six 1980 vintage printed through hole (PTH) technology circuit cards. Implementing COTS advanced electronic packaging reduced the space and weight by over 80 percent by integrating state-of-the-art surface mount technology (SMT) into the design. The EAU, developed from data generated by the EMMA program, became a single circuit card employing fine pitch surface mount

technology and advanced packaging technology. This reduced manufacturing costs by 57 percent. By pro-actively implementing COTS technology to the EAU, potential sustainment issues due to component obsolescence were resolved without compromising the design's functionality, the system's reliability or its manufacturability. The new EAU design is interchangeable with its predecessor, an important feature to meet the Standard Missile Program sustainment requirements.

The second EMMA program deliverable is the creation of the Technical Applications Guidelines (TAG) Handbook. Coordinated by the American Competitiveness Institute (ACI), the handbook's objective is to provide government and industry personnel with information concerning the introduction of COTS advanced electronic packaging into a high reliability environment. The handbook's intention is to serve as a technical resource that documents the design, manufacturing, and reliability concerns encountered during the program. The handbook offers suggestions on how to introduce these technologies into environments and provides lessons learned from the program's experience. The handbook is geared towards:

- Program Managers wishing to learn about advanced electronic packaging.
- Design Engineers wishing to introduce advanced electronic packaging into their designs.
- Manufacturing Engineers wishing to build hardware with advanced electronic packaging.

The EMMA program team represents a diverse range of participants within the electronics manufacturing community:

- ACI; Philadelphia, Pennsylvania
- Raytheon; Tucson, Arizona and McKinney, Texas
- Rockwell Collins; Cedar Rapids, Iowa
- Naval Surface Warfare Center-Crane; Crane, Indiana
- Marquette University; Milwaukee, Wisconsin
- Georgia Tech Research Institute; Atlanta, Georgia
- AMCOM; Huntsville, Alabama

The TAG Handbook data was based on research and experiments performed by the EMMA program team. A Design of Experiment (DOE) test vehicle was designed to utilize a wide variety of advanced electronic packaging technologies. The team investigated various issues concerning implementing advanced electronic packaging in high reliability designs.

Component Upgrading Performance

ACI determined if a specific commercially rated component could pass high reliability Environmental Stress Screening (ESS). Component reliability was measured by performing various ESS test procedures, required by the Standard Missile Program. To date, no failures have been found with the components tested.

Design and Manufacturing Development

Raytheon, Rockwell Collins, and ACI designed and built a test vehicle (Figure 2) with the advanced electronic packaging components selected for the program. This test vehicle was made of different board materials and surface finishes, with 42 daisy chain components.

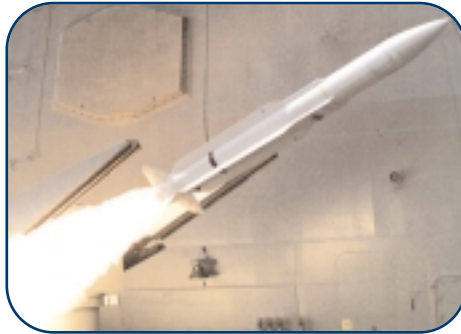


Figure 1. Standard Missile

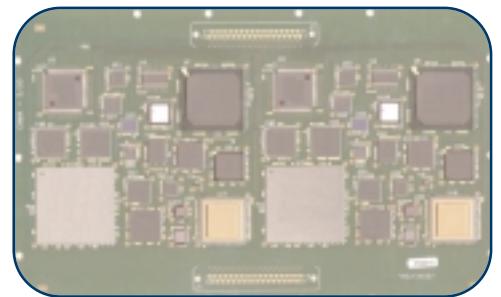


Figure 2. EMMA DOE Test Vehicle

continued on p. 4

Advanced Packaging Assembly Process Overview

Advanced packaging and other emerging technologies are rapidly increasing their presence within the world of interconnect solutions. The assembly process is the bridge between silicon and the electronic system and it is becoming more important to commercialize these technologies successfully. As the standard Integrated Circuit (IC) packaging assembly processes become mature, these processes also have been outgrown vertically and horizontally to accommodate the newer and more sophisticated packages such as micro electromechanical systems (MEMS) devices. Figure 1 is an example of a MEMS device. However, the complication and the miniaturization trend of MEMS devices also introduces many difficult challenges in the assembly processes.

A typical packaging process involves steps such as die-attach/bonding, interconnection, encapsulation/underfill, overmolding, and final testing.

Typically, a silicon wafer is diced to allow the pick and place operation that occurs prior to the die-attach assembly step. The traditional dicing techniques used in the semiconductor industry unfortunately are not satisfactory for several classes of MEMS devices. Currently, there is not a cutting technique that meets all of the desired characteristics for MEMS dicing, however, special dicing techniques have been developed for specific needs.

Once the die is separated from the wafer, it must be attached to the chosen substrate material. This step precedes the interconnection such as wire bonding. Often, this step includes an adhesive bond layer being deposited onto the substrate material prior to placing the die on the substrate. A curing, annealing, or firing step to secure the adhesive bond then follows the placing step. The stress sensitivity of MEMS devices requires some extra considerations regarding the die attachment method and location.

The electrical interconnection for microelectronics includes wire bonding, flip chip or ball bonding, and tape automated bonding technologies. Wire bonding is popular technique to electrically connect the die to the packing. The wire bonding process has two types: thermocompression (heat and pressure) and thermosonic (heat and ultrasonic vibrations).

Both methods provide energy to form the metallurgical bond between the wire and the pad. However, the ultrasonic energy may increase the risk of structure failure during the bonding process due to the structure of MEMS. Flip-chip bonding involves bonding the die, top-face-down, on a package substrate. Electrical contacts are made by means of bumps between bond pads on the die and metal pads on the package substrate. The bump materials can be metals such as solder, aluminum, and gold or conductive adhesive. Flip-chip bonding is attractive to the MEMS industry because of its ability to closely package a number of distinct die on a single package substrate with multiple levels of embedded electrical traces.

The steps following the interconnection include overmolding or encapsulating/underfill. Polymer materials are being used more for packaging MEMS because of their moldability and high temperature tolerance. However, coefficient of thermal expansion (CTE) of the polymer becomes a concern for packaging reliability performance because the CTE mismatch is a source of package stress. While encapsulant isolates interconnects from the harsh environment, underfill adhesive can be used to redistribute the stress between the chip and die and improve the reliability of the package. Effective dispensing of encapsulant materials is a key part of integrating chip-level components into the PCB environment. This may consist of relatively simple glob top dispensing of material to cover the entire component or complex dam & fill operations to build a precise perimeter around the components(s) before filling the cavity with encapsulant.

The final step of the packaging assembly process is the final testing. After the package assembly is completed, a final test that includes electrical, mechanical, and environmental testing is conducted.

The final step of the packaging assembly process is the final testing. After the package assembly is completed, a final test that includes electrical, mechanical, and environmental testing is conducted.

References:

- 1) William D. Brown. "Advanced Electronic Packaging."
- 2) P. Rai-Choudhury. "MEMS and MOEMS Technology and Application."
- 3) Bishnu Gogoi et al. "Challenges in MEMS packaging."
- 4) Rajeshuni Ramesham Ph.D and Reza Ghaffarian. "Interconnection and Packaging Issues of Micro electro mechanical Systems (MEMS) and COTS MEMS."

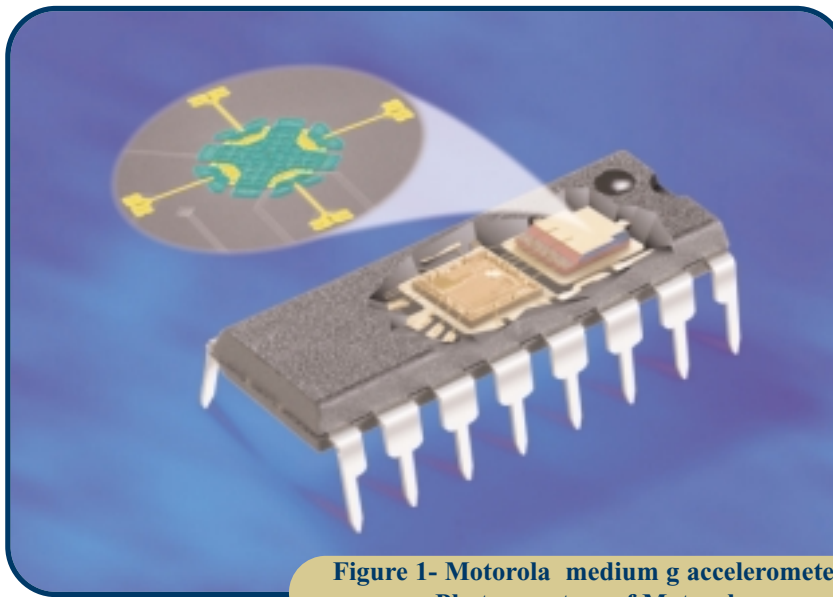


Figure 1- Motorola medium g accelerometer.
Photo courtesy of Motorola

EMMA

(continued from p. 2)

Lessons learned from the design and manufacturing activities provided technical information on the development activities and the production runs. By including these lessons learned in the TAG Handbook, individuals wishing to introduce COTS advanced electronic packaging into a high reliability environment will learn from the EMMA program.

Assembly Environmental Stress Screening

Raytheon, Rockwell Collins, and ACI investigated which combination of components, solders, board material and finish affect assembly reliability. Assembly reliability is determined through thermal cycling and random vibration testing. Naval Surface Warfare Center - Crane is currently performing the tests.

State of the Market Surveys

Georgia Tech Research Institute and Rockwell Collins performed independent industry surveys to determine what the component electronic packaging market offers. The Rockwell Collins' market survey concentrated on microelectronics packaging in high reliability environments. Georgia Tech Research Institute's market survey discusses the background and risks associated with applying COTS advanced electronic packaging.

Raytheon developed a database on component reliability. The purpose of the EMMA reliability database is to provide a common formatted storage location for reliability data on state-of-the-market electronic components with possible applicability to high reliability usage.

Materials Analysis

Marquette University performed a series of experiments to evaluate component underfills and encapsulants material properties, using AC Impedance Spectroscopy. From these experiments, it was determined that it was possible to monitor the quality of underfills and encapsulants, with respect to storage life, pot life, and moisture migration.

Reliability

Raytheon performed a series of experiments which determined the board level reliability of fine pitch area array packages with immersion silver and immersion gold over nickel. For example, through these experiments it was determined that higher concentrations of a gold - tin intermetallic near the board and component interfaces allowed faster crack propagation within the solder joint, which will reduce solder joint reliability. Rockwell

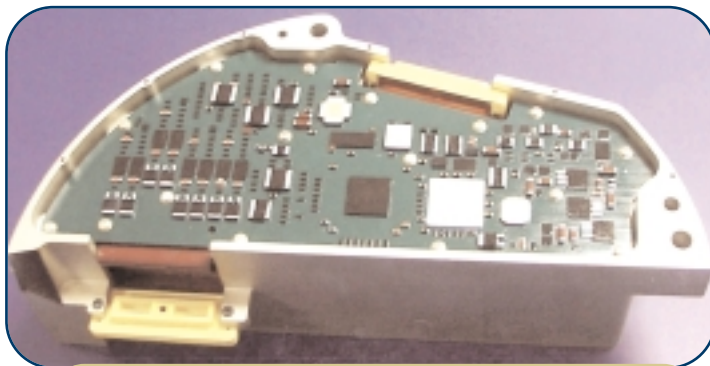


Figure 3. Standard Missile New Electronics Assembly Unit

Collins is performing another series of experiments, determining the manufacturing properties of various underfills. These experiments will show the how underfill properties affect manufacturing process variables with respect to time.

Information gathered for the TAG Handbook was used in upgrading the

The EMMA Program has provided further insight into the challenges of using COTS area array semiconductor packages in high performance military electronics. While this extensive study has found that there are no easy solutions, it has also found that some COTS packaging technologies can successfully be used in high reliability applications. Rockwell Collins and other industries in the military electronics business will continue to be challenged with using COTS components. And thus programs like EMMA must continue to evaluate the impact of these technologies for high performance and high reliability systems.

-- Jim Van Pietersom
Rockwell Collins
EMMA Project Engineer

Standard Missile Electronics Assembly Unit (EAU). Based on data captured by the EMMA program, the EAU was modified. Raytheon has held a series of reviews to assure that the new design met the requirements. Prototype EAU units have been built. The new EAU's single - sided SMT circuit card, which replaced the six double-sided 1980 vintage PTH technology circuit cards, have passed ESS testing. The entire assembly (Figure 3) is currently undergoing ESS testing. The latest information from Raytheon is that the test flight of the Standard Missile, with the new EAU design, is scheduled for October, 2001.

In parallel to the program's objectives, a technology transfer activity was executed. EMMA program members were

The EMMA program has provided a valuable insight into many of the important issues that need to be addressed if commercial production procedures and techniques are to be used for military applications.

-- Dr. Marty Seitz
Marquette University
Director of Materials Science
& Technology Center

continued on p. 5

EMMA (continued from page 4)

encouraged to share technical data with industry. This enabled the EMMA team to provide the electronics industry technical information on data found from EMMA program activities by presenting papers on the program's investigations. At the same time, these conferences gave EMMA

Raytheon's participation on the EMMA team has been very positive. A key to the success of the program has been the diverse technical expertise and experience that the various members bring to the team. The Raytheon team is especially pleased with the results of the EMMA Test Vehicle portion of the project. The Standard Missile Electronics Assembly (EAU) was successfully re-designed and the number of boards was reduced from six (double sided) to one single sided board. The team was able to accomplish this by incorporating some of advanced packaging findings that came out of the EMMA Design of Experiments portion of the project. Significant cost and size reductions were achieved and the project is expected to complete hardware qualification in late September.

**--Juan Silva
Raytheon
EMMA Program Manager**

program team members insight on applying COTS advanced electronic packaging to high reliability applications. Some of the conferences attended include:

- Defense Manufacturer's Conference: November 1999; November 2000
- Military & Aerospace / Avionics COTS Conference: August, 2000; August, 2001 Commercialization of
- Military & Space Electronics Conference: February 2001
- NEPCON East: June 2001

Feedback from such industry participation has been positive. Conference attendees requested the immediate release of the TAG Handbook while it was in development, so it can be concluded that the completed handbook will fill a void in the high reliability electronics environment. Future tasks under consideration include performing follow-up activities continuing the EMMA program mission on other programs, and updating the TAG handbook as new electronic technologies are developed.

At the 2001 Defense Manufacturer's Conference, the TAG Handbook will be released via CD-ROM and a website. At the 2002 Commercialization of Military & Space Electronics Conference, Rockwell Collins will provide additional findings from the EMMA Program.

I feel the EMMA program has made important contributions in drawing together the latest on technology for electronics miniaturization and packaging. It is intended to provide a reference for engineers and managers to use in dealing with this broad, multi-disciplinary subject. It attempts to present terminology and guidelines in a consistent manner across a wide range of package types of importance to both commercial and military electronics.

**--Dr. Ron Bohlander
Georgia Tech Research Institute
GTRI Fellow and Manager**

The EMMA program met the quantitative and qualitative goals defined by the Standard Missile Program, and provided a baseline on how to incorporate COTS advanced electronic packaging to an existing system with high reliability requirements. This baseline and implementation philosophy can be applied to other heritage systems across all services. Raytheon and Rockwell Collins are initiating plans to introduce COTS technology on other high reliability programs, based on the output from the EMMA program.

Through the course of the program, a synergic effect across the team members from government, industry, and academia made the program activities and investigations more productive. The final result of the EMMA Program is the TAG Handbook, which provides technical information to its audience concerning the implementation of COTS advanced electronic packaging in hostile environment.

The EMMA Program represents an excellent example where Government, Industry, and Academia successfully came together to solve a technical applications problem in electronics manufacturing. The output of the program, the deployment of the new EAU for the Standard Missile and the TAG Handbook release, will serve as a "pathfinder" for introducing COTS packaging technologies in high reliability applications.

**--Phil Davis
ACI
EMMA Program Coordinator**

Electronics Manufacturing Learning Center

Course Schedule for Calendar Year 2002

Electronics Manufacturing

Electronics Manufacturing BOOT CAMP A - Week 1

Mar. 4-8
 May 6-10
 Sept. 16-20
 Oct. 28-Nov. 1

Electronics Manufacturing BOOT CAMP B - Week 2

Mar. 11-15
 May 13-17
 Sept. 23-27
 Nov. 4-8

Certifications

IPC J-STD-001 Instructor Certification

Jan. 7-11
 Feb. 4-8
 Mar. 18-22
 Apr. 15-19
 May 20-24
 June 3-7
 July 15-19
 Aug. 5-9
 Sept. 23-27
 Oct. 14-18

IPC J-STD-001 Instructor Recertification

Jan. 28-29
 Mar. 4-5
 May 13-14
 Jul. 8-9
 Sept. 16-17
 Nov. 4-5

EMPF J-STD-001B Instructor Recertification

Jan. 23-24
 Apr. 8-9
 Jul. 29-30

IPC Challenge

Jan.30
 Mar. 6
 May 15
 Jul. 10
 Sept. 18
 Nov. 6

Certifications (continued)

IPC-A-610 Instructor Certification

Jan. 14-18
 Feb. 11-15
 Mar. 25-29
 Apr. 22-26
 Jun. 10-14
 Jul. 22-26
 Aug. 12-16
 Oct. 7-11

IPC-A-610 Instructor Recertification

Jan. 31-Feb. 1
 Mar. 7-8
 May 16-17
 Jul. 11-12
 Sept. 19-20
 Nov. 7-8

IPC-A-600 Acceptability of Printed Boards Instructor Certification

Feb. 27-Mar. 1
 Jun. 26-28

Skills

SMT Manufacturing

Jan. 28-Feb. 1
 Apr. 1-5
 Apr. 29-May 3
 Jun. 17-21
 Aug. 19-23

SMT Soldering/Rework

Feb. 11-15
 May 20-24
 Jul. 15-19
 Nov. 18-22

BGA Manufacturing, Inspection & Rework

Feb. 4-5
 Apr. 8-9
 Jun. 3-4
 Aug. 5-6
 Oct. 7-8

Advanced Packaging Techniques

Feb. 6-8
 Apr. 10-12
 Jun. 5-7
 Aug. 7-9
 Oct. 9-11

Continuing Professional Advancement

Design for Manufacturability

Feb. 25-26
 Apr. 29-30
 Jun. 24-25
 Aug. 19-20
 Oct. 21-22

Failure Analysis and Reliability Testing in Electronics Manufacturing

Jan. 14-16
 Apr. 22-24
 Aug. 12-14
 Nov. 13-15

Characteristic Properties of Materials in Electronics Manufacturing

Jan. 7-9
 Apr. 15-17
 Jul. 22-24
 Oct. 14-16

**For more information,
 or to register for classes,
 please call: (610) 362-1295
 email: registrar@empf.org.
 Visit our web site for more
 course information:**

www.empf.org.

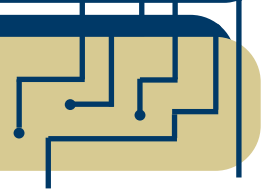
**Course schedule is subject to
 change, please contact our
 Learning Center for the
 most current scheduling
 information.**



Electronics Manufacturing
Productivity Facility

TECH TIPS...

Circuit Board Repair



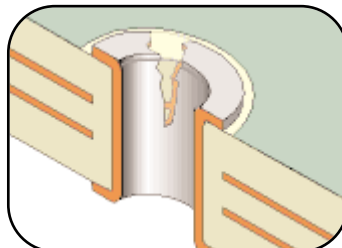
Cut here and save!!

This article is based on and derived from IPC-7721, Repair and Modification of Printed Circuit Boards and Electronic Assemblies, which contains the complete procedures presented here in brief form.

Repair in the electronics industry is defined as the act of restoring the functional capability of a defective article in a manner that precludes compliance of the article with applicable drawings or specifications. If a printed circuit board is deemed to require repair, the first consideration is the cost of the repair as opposed to the value of the board or assembly. The next considerations are the skill level of the repair technician and the availability of the proper tools and supplies. These last considerations are detailed in the repair document.

Plated Hole Repair No Inner Layer Connection

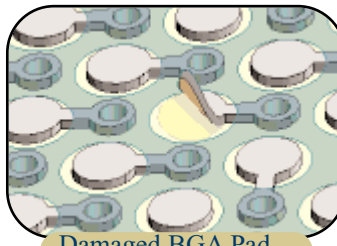
This procedure covers the repair of a damaged hole and is intended only to restore the integrity of the through hole connection. To complete the procedure, the damaged hole is drilled to the proper size to allow the installation of an eyelet. The eyelet is then flared or set, the surrounding circuitry is then cleaned, flux applied and soldered to the circuit.



Damaged Plated Hole

Surface Mount Pad Repair

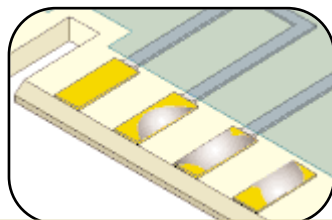
This procedure is used to replaced surface mount pad(s), which have been lifted from the board. After the pad area has been properly prepared, the correct size and shape replacement dry film pad is chosen and bonded in place using a bonding tool and tip similar to a soldering iron. The repair is completed by lap soldering the new pad to the circuitry.



Damaged BGA Pad

Edge Contact Repair

This procedure is used to replace edge contacts or "edge fingers" that have been damaged or worn from insertion in mating connectors. After the contact area has been properly prepared and



Contaminated Gold Edge Contacts

the dry film replacement contact selected, the contact is bonded in place. The contact is then lap soldered to the circuitry, the overhanging contact end is filed and beveled to the board edge and then cleaned.

Land Repair

This procedure is used to replace a lifted or damaged land or pad of a through hole connecting circuitry. After the pad/land area has been properly prepared and the dry film replacement has been selected, the "dry film" is bonded in place. The replace pad/land is lap soldered to existing circuitry and through hole is drilled for the installation of an eyelet, which will be flared or set in place and soldered to the circuitry.



Damaged Land

Lifted Land Repair

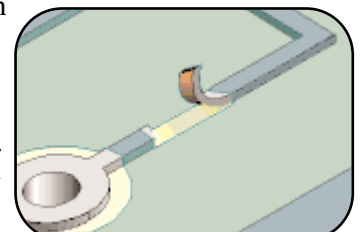
This procedure is used to repair a lifted land. After the lifted land area has been properly prepared, select a piece of dry film adhesive of the correct shape and thickness and bond it in place with the proper bonding tool and tip.



Lifted Land

Conductor Repair

This procedure is used to replace damaged or missing conductors. In this instance, a surface wire or a dry film circuit replacement can be used. After the affected area has been properly prepared from the jumper wire into the circuit pattern, lap solder the wire to the circuitry and adhesive bond the wire to the printed circuit board surface. If dry film circuitry is used, select a shape that conforms to the circuit pattern and bond it into place. Complete the circuit path by lap soldering.



Damaged Conductor

Figures are courtesy of Circuit Technology Corporation. www.circuittechctr.com

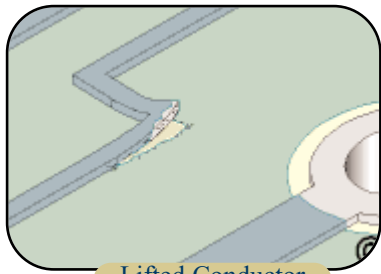
continued on p. 8

Circuit Board Repair

(Continued from p. 7)

Lifted Conductor

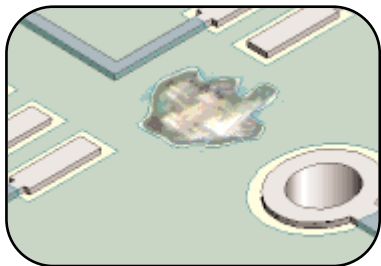
This procedure is used to reattach a lifted conductor pattern. After the affected area has been properly prepared, select a piece of dry film adhesive of the correct shape and thickness and bond the conductor in place using the correct bonding tool and tip.



Lifted Conductor

Base Material Repair

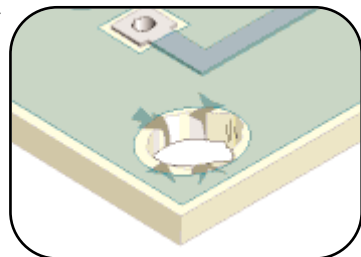
This procedure is used to repair minor surface damage to the printed board surface, commonly cuts and burned areas. The damaged area will be cleaned of any loose material and then the burn or cut area will be drilled with a rotary tool using a ball mill cutter in a manner to create an under-cut cavity, which will enhance mechanical attachment. Liquid epoxy is then applied to the milled area, cured by the proper method. Dress the epoxy to the board surface. Replacement solder mask or conformal coating is then applied to the repaired area.



Damaged Base Material

Hole Repair (Mounting Hole)

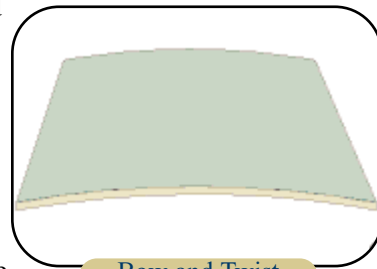
This procedure is used to repair a damaged mounting hole. Drill or mill out the damaged hole area. Clean and then install a dowel made of the same material as the board. Epoxy the dowel into place using high strength epoxy. Cure the epoxy and dress the dowel ends to the board surface. Redrill the hole to the proper size.



Damaged Hole, Non Plated

Bow and Twist Repair

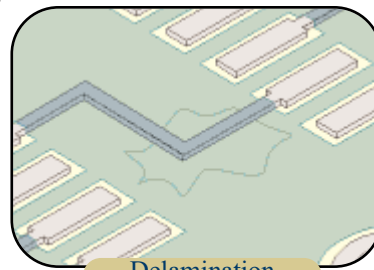
This procedure is used to correct a bow or twist that affects a printed wiring board or assembly. A prime consideration in the use of this repair method is the board material, since the procedure is more appropriate to board materials having a glass transition temperature below 125°C. The procedure involves the placement or clamping of "restraint bars" along the printed board edges of the warp or bow. The assembly is then placed in an oven at a temperature of 125° for one hour. After that time, turn the oven off, leaving the assembly in the oven to cool. After the assembly has cooled, remove it from the oven and measure for any remaining warp or bow.



Bow and Twist

Delamination/Blister Repair

This procedure is used to repair mechanical delamination or blisters resulting from local overheating of a printed wiring board. Using a ball mill or drill, drill holes on opposite sides of the affected area. Bake the board in order to drive off any moisture and inject the pre-mixed low viscosity into one of the holes. Cure the epoxy, dress the repaired area to the original board surface and apply additional coating as may be required.



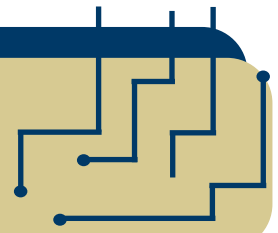
Delamination

As stated in the beginning of this article, the information presented is from IPC-7721 and is not the entire detailed procedure required to complete a given repair. For complete information and repair technician qualification as well as the required tools and supplies, refer to the IPC-7721.

**For more information
on circuit board repair, please call the
EMPF Helpline at (610) 362-1320.**

Manufacturer's Corner

Electrovert Bravo 4050 Reflow Oven



Manufacturing engineers are regularly tasked with performing evaluations and making recommendations for the purchase of SMT equipment. Every piece of equipment in a surface mount assembly line is equally important to produce quality boards and requires an analysis to determine if it will meet both present and future process requirements. The major factors to take into consideration when evaluating a reflow oven must include the following:

Heating Source

Convection heat is the most common heat source used in reflow ovens. Convection heat is generated by blowing air across a heating element that is located in each temperature zone in the oven. Most ovens will have both top and bottom side heaters to stabilize and maintain the temperature settings. The hot air is contained in each zone and it is transferred to the printed circuit board as it passes through the oven on the conveyor. If the temperature of any zone goes out of tolerance, there are alarms to alert the operator that the process is not in control.

Temperature Zones

Reflow ovens will usually have between four and seven temperature zones. The temperature in each of these zones should be independently controlled and must remain stable ($\pm 5^{\circ}\text{C}$) as boards are processed. The advantage of the additional zones is to more precisely control the amount of heat that is transferred to the board as it passes through the oven. Typically a four-zone oven is adequate for most 0.062" and 0.093" FR4 printed circuit boards, even if they are densely populated. When reflowing

large multi-layer boards with ground planes and ceramic parts, or soldering with high temperature alloys, such as lead free solder, additional zones prove to be helpful.

Conveyor

Reflow ovens that are manufactured with a mesh belt conveyor are adequate for reflowing single-sided surface mount boards. Reflow of a double-sided surface mount board will require an oven with adjustable rails. Limitations of the minimum and maximum width openings and a center board support should be considered for both present and future capabilities.

Reflow Profile

The purpose of the solder reflow profile is to activate the flux system in the paste, control the rate of temperature change to the board as it passes through the oven and to reflow the sol-

with the solder alloy and chemistry of the flux used in the solder paste. This profile will always be included in the solder paste specification published by the manufacturer.

To develop a reflow profile for a board, it is necessary to measure the temperature of the board as it passes through the different zones in the oven. The oven manufacturer usually recommends a starting profile, or an existing profile for a similar board can be used. Thermocouples must be attached to various locations on the board to record the temperature of the board as it is run through the oven. The board temperatures are then compared to the recommended profile for the solder paste. The belt speed and temperature of the zones are then adjusted to obtain the targeted profile. Software is available to simulate the change of temperature to the board as the belt speed and

zone temperatures are varied. This helps minimize the time to profile a board and reduces the number of times a board will need to be passed through the oven to determine the profile.

Nitrogen

Some ovens are manufactured with an option for Nitrogen. A Nitrogen atmosphere during reflow prevents oxidation and will improve solderability of the board and components. Nitrogen is also commonly used when soldering with lead free solder

alloys. Consideration for this option should be given at time of the oven purchase, as many times this is not a field upgradable option.



Electrovert Bravo 4050 Reflow Oven

der paste. To avoid damage to the components, the rate at which the board absorbs heat should not exceed 3°C per second. The reflow profile should follow the profile that is recommended by the solder paste manufacturer for that particular paste. Profiles will vary

continued on p. 10

Technical Applications Guideline Handbook (continued from page 1)

Packaging in high reliability environments. The handbook also provides technical data on how to introduce these technologies into high reliability environments. The TAG Handbook provides conclusions and advice based on lessons learned from the EMMA Program's experiences.

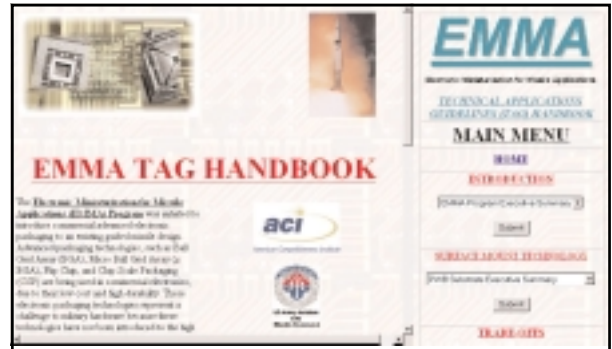
The goal for the handbook is to support the engineering community in developing high reliability electronics hardware utilizing Advanced Electronics Packaging, from a design's concept phases through production. For example, if a design engineer would like to know how a specific electronic package performs via thermal cycling, the design engineer would consult the TAG Handbook. The TAG Handbook provides a manufacturing engineer insight on how to incorporate Chip Scale Packaging components into an existing

production line. Program Management would benefit from the handbook as an information source on advanced electronics packaging that would be integrated into a MIL spec product.

It is anticipated that the TAG Handbook will serve the electronics manufacturing community well. In introducing the handbook's concept at various conferences, conference attendees requested its immediate release while it was in development. The handbook will be offered on hard copy or electronically, via CD-ROM. In addition, access to the handbook will be made available through the American Competitiveness Institute's website.

It is planned that the TAG Handbook will continuously evolve. Future tasks under consideration include performing follow-up activities continuing the EMMA program mission on other programs, and updating the TAG Handbook as new electronic technologies are developed.

EMMA Tag Handbook Website



Manufacturer's Corner (continued from page 9)

Summary

When selecting a reflow oven, determine the current requirement and consider what the future capability of the oven should be. Limitations should be identified and known on the front end rather than after the oven is installed. For example, the application for an oven in a dedicated surface mount line will differ significantly than an oven used by a contract manufacturer who has a need to solder many different board configurations on an ongoing basis.

This month, a PCB manufacturer visited the EMPF to evaluate various reflow ovens and select one that would best meet their needs. After a review of their production requirements, along with board size, throughput, floor space limitations and budget, they

selected the ELECTROVERT Bravo 4050 reflow oven. The manufacturer found that the Bravo 4050 combines the strength and thermal flexibility of high-energy storage with a rod heating element that preheats air at the blower intakes. Increased heater surface area provides optimum, efficient convection heating while accommodating temperatures to of 300°C. High volume blowers located at the top and bottom of each zone provide exceptional volumetric flow to ensure maximum flexibility and heat transfer. The single lower chamber design eliminates separate tunnel and chamber walls to improve performance and reduce maintenance.

The Bravo 4050 is designed for easy programming and operation. Standard software features include onscreen

help, maintenance screens, and system debugging. Software is optionally available for Windows NT™.

This oven easily accommodates substrates to 18" and offers a heated tunnel length of 50 inches. A stainless steel mesh belt is standard and an optional motorized pin rail conveyor is also available. Other options include additional cooling capability, light tower, SMD compatibility, and output photocell.

If you would like to see a demonstration of this oven or any other equipment at the EMPF, please contact Jeff Stong at (610) 362-1200, extension 224 or jstong@aciusa.org.

Ask the EMPF Helpline!

CUSTOMER ISSUE: Recently a customer called the EMPF Helpline inquiring about the electro-static discharge (ESD) protection of Integrated Circuits (ICs) supplied on tape & reel packaging. The customer also asked if the reels had to be placed into ESD bags when moving them short distances.

HELPLINE RESPONSE: Devices are safe if they are packaged in tape & reel format using ESD protective materials.

If the integrity of the reels has not been damaged, then it is not necessary to place the reels into ESD bags. However, if the packaging is damaged, or the components are exposed, then the parts are indeed susceptible to ESD damage during transit over even a short distance. Also, the sensitivity of the part, and the relative humidity of the environment, are two critical factors in determining the necessity for taking further ESD protective measures.



Figure 1 - ESD Protective Tape and Reel Packaging of Components

ESD Component Failures:

Generally, damage to a device is classified as either catastrophic or latent. With catastrophic failures, the device fails to function immediately due to junction breakdown, oxide failure, or metal melting. With latent failures, only partial damage is sustained, and the device may continue to function properly, but experience premature failure. It is usually difficult to detect a latent failure.

The ESD sensitivity of the component can be determined by reviewing the manufacturer's specification sheet. Some devices, such as Junction Field Effect Transistors (JFETs), are more susceptible than others.

ESD Manufacturing Related Products

The following list contains materials and devices that are currently being used in manufacturing areas to minimize ESD problems. For specific ESD prevention applications, these devices and materials should be evaluated and implemented as required.

- ESD bags (Figure 2)
- Conductive foam
- Floor mats
- Static spray
- Anti-static hand lotion
- Conductive storage boxes
- Work-table dissipative mats
- Conductive lab coats (Figure 3)
- Wrist straps and accessories
- Grounding shoe devices
- Conductive storage cabinets



Figure 2 - ESD Protective Bag

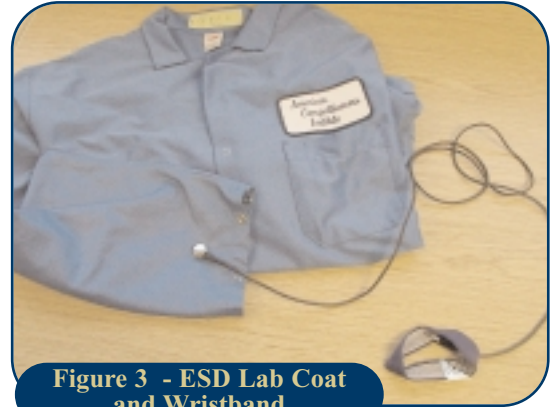


Figure 3 - ESD Lab Coat and Wristband

Summary and Recommendations

Advanced technology includes smaller and more complex geometry, which is in increasing danger of ESD damage. Identify the production areas that need electrostatic control, and define the level of component susceptibility. Eliminate and reduce the generation of static charge where possible, and dissipate or neutralize the charges that do occur. Use proper grounding techniques at workstations and on process equipment to deal with the ESD that does occur by preventing it from discharging directly through the components.

Two informative reference documents (standards) that relate to the subject of ESD are:

- 1) ANSI / ESD S20.20
Development of an ESD control program for - Protection of Electrical and Electronic Parts, Assemblies, and Equipment.
- 2) JESD625-A (revision of EIA - 625) requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.

**If you have an electronics manufacturing problem,
call the EMPF Helpline at (610) 362-1320.**

American Competitiveness Institute - 2001- 2002 EMLC COURSES

November

5th-6th EMPF J-STD-001 Instructor Recertification
 7th IPC Challenge
 8th-9th IPC-A-610 Instructor Recertification
 15th-16th BGA: Manufacturing, Inspection & Rework

December

3rd-7th IPC J-STD-001 Instructor Certification
 10th-14th IPC-A-610 Instructor Certification

January 2002

7th-9th Characteristic Properties of Materials
 7th-11th IPC J-STD-001 Instructor Certification
 14th-16th Failure Analysis and Reliability Testing
 14th-18th IPC-A-610 Instructor Certification
 23rd-24th EMPF J-STD-001B Instructor Recertification
 28th-30th J-STD-001 Instructor Recertification
 30th IPC Challenge
 31st -Feb. 1st IPC-A-610 Instructor Recertification
 28th -Feb. 1st SMT Manufacturing

February 2002

4th-5th BGA: Manufacturing, Inspection and Rework
 4th-8th IPC J-STD-001 Instructor Certification
 6th-8th Advanced Packaging Techniques
 11th-15th IPC-A-610 Instructor Certification
 11th-15th SMT Soldering/Rework
 25th-26th Design for Manufacturability
 27th-Mar. 1st IPC-A-600 Acceptability of Printed Boards Instructor Certification

March 2002

4th-6th J-STD-001 Instructor Recertification
 4th-8th Electronics Manufacturing Boot Camp A
 6th IPC Challenge
 7th-8th IPC-A-610 Instructor Recertification
 11th-15th Electronics Manufacturing Boot Camp B
 18th-22nd IPC J-STD-001 Instructor Certification
 25th-29th IPC-A-610 Instructor Certification

April 2002

1st-5th SMT Manufacturing
 8th-9th BGA: Manufacturing, Inspection and Rework
 8th-9th EMPF J-STD-001B Instructor Recertification
 10th-12th Advanced Packaging Techniques
 15th-17th Characteristic Properties of Materials
 15th-19th IPC J-STD-001 Instructor Certification
 22nd -24th Failure Analysis and Reliability Testing
 22nd-26th IPC-A-610 Instructor Certification
 29th-May 3rd SMT Manufacturing
 29th-30th Design for Manufacturability

**For more information,
 please call the
 EMPF registrar at
 (610) 362-1295 or
 e-mail: registrar@empf.org**

Issue 10-01

Emphasis is a publication of the American Competitiveness Institute and the EMPF. The EMPF is the U.S. Navy's National Center of Excellence dedicated to advancing the state-of-the-art in electronics and increasing domestic productivity in electronics manufacturing.



American Competitiveness Institute
 One International Plaza
 Suite 600
 Philadelphia, PA 19113
 (610) 362-1200 • FAX: (610) 362-1290
 HELPLINE: (610) 362-1320
 WEBSITE: www.empf.org

PRESORTED
 STANDARD
 U.S. POSTAGE PAID
 PHILADELPHIA, PA
 PERMIT NO. 5490