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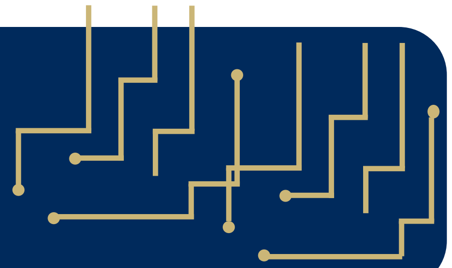

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The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

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Technology Refresh

Rapid evolution of electronics technologies along with the downturn in procurement of new equipment has produced a consolidation of the defense industrial base and has caused DoD suppliers to shift their focus to commercial electronics markets (see Figure 1 and Figure 2 (page 2)). This is one reason why DoD weapon systems will be increasingly comprised of commercial off-the-shelf (COTS) components. Unlike previous custom-built DoD systems, COTS-based systems require a tailored in-service refresh strategy reflecting their different sustainment challenges.

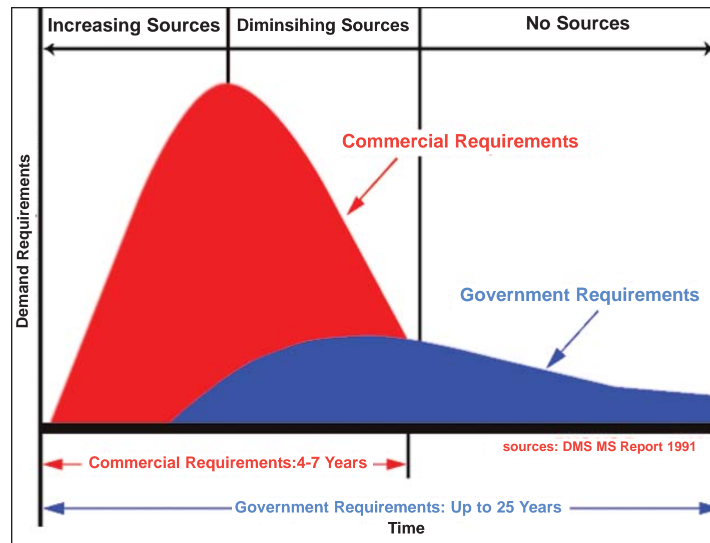

Figure 1 - DoD/NASA needs are not in sync with the commercial Electronic Marketplace. Graph courtesy of DMEA website

Technology refreshment is the only viable means to sustain the capability over the service life of the system. Technology Refresh (TR) is defined as the periodic replacement of both custom-built and (COTS) system components, within a larger DoD weapon system, to assure continued supportability throughout its lifecycle.

Without TR, the DoD will not be able to adequately maintain and sustain its aging weapon systems over a prolonged service life.

To meet DoD transformation objectives, fleet capability must be able to change rapidly to meet evolving threats, but current approaches to TR constrain responsiveness. Upgrading existing systems is slow and expensive. This barrier could be substantially reduced by capability enhancements that are coordinated with obsolescence solutions or if re-designs were better informed by technology roadmaps.

Manufacturers are currently unable to effectively manage TR so that solutions are optimized across issues of capability enhancement, technology roadmaps and obsolescence mitigation for timely improvements in weapon systems capability and flexibility. Capability enhancement and obsolescence management programs are done today, but as disjoint activities by different parts of an organization. Supply chain implications are seldom considered. Current efforts are narrowly focused on solving tactical, local, issues. Managers are often surprised and forced to spend most of their effort reacting to problems because they do not have the information to pro-actively work the issues. Several tools exist to address various aspects of the TR problem but they are fragmented, incomplete and offer little collaboration across the supply chain. No

continued on page 2

Technology Refresh (continued from page 1)

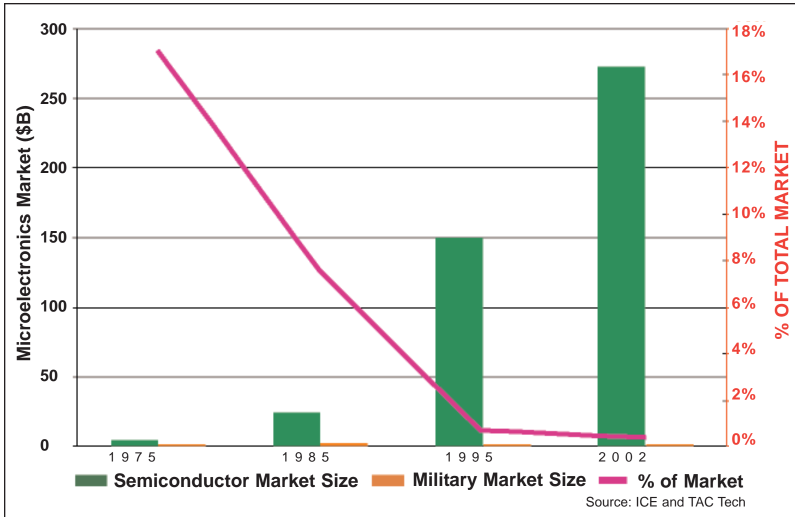

Figure 2 - shows military share of market is at an all time low. Graph courtesy of DMEA website

Figure 3 illustrates the uses for our new TRENT TR tool kit along with the different types of users involved in the TR process. In the lower left is the Systems Engineer who is designing a module to meet requirements. The systems engineer is accessing the design tools necessary for this through the TRENT framework. In the upper right hand corner is the module supplier who is using a roadmapping tool to track new technology and make business decisions on when to stop supporting an older version of the module and start producing newer modules based on the newer technology. In the upper left corner is the TR engineer who is utilizing this information, including the current inventory level of existing modules from the Enterprise Resource Planning (ERP) database, to make better decisions on when and how to perform TR on the system.

infrastructure exists to integrate the processes, information flows, and tools to effectively deal with TR in a comprehensive manner. The development of a planned and organized Technology Refresh program is critical to ensure long-term weapon system availability.

The American Competitiveness Institute (ACI) has partnered with Advanced Technology Institute (ATI), Lockheed Martin Advanced Technology Laboratories and Altarum to develop a new comprehensive Technology Refresh strategy. This new strategy will be a combination of processes, tools, and an information technology (IT) infrastructure that includes all stakeholders, so companies can manage TR as a comprehensive activity. This will enable transformational weapon system products to be produced in a much shorter period of time. This solution will produce an optimized TR for any weapon system. It represents the most timely and cost-effective plan for refreshing a particular weapon system. It facilitates the decision making process of whether to perform technology insertion, technology refresh, or do nothing during the weapon system's planned availabilities. It will facilitate adoption of transformational capabilities. This solution is expected to speed improvements of Navy weapon systems by reducing the cycle time for introducing new technologies and enhanced capabilities by at least 25%. In addition, Operation and Support (O&S) costs should be reduced by at least 10%. These improvements will be achieved by integrating weapons system (WS) improvements and obsolescence resolution into a comprehensive TR process and tool set that can effectively manage the issues at the system to component levels.

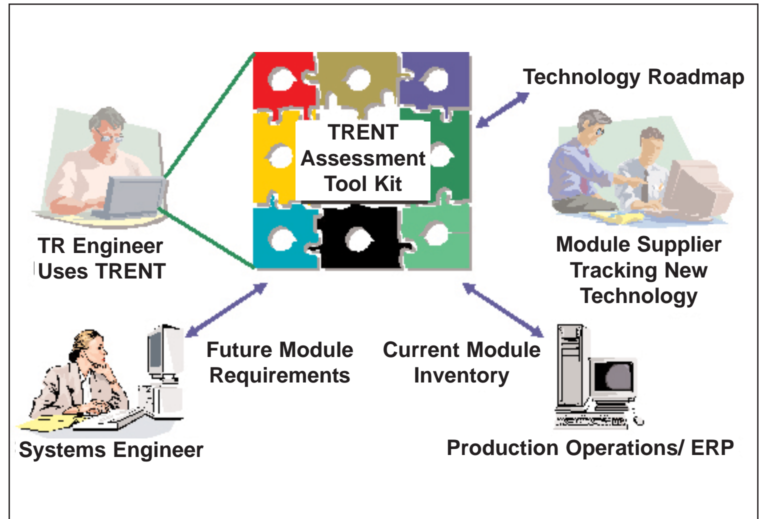

Figure 3 - Courtesy of the TRENT team (Lockheed Martin, ATI, and Altarum) and the SPANS TRENT Program

Technology is very expensive to adopt when it is still considered State-of-the-Art. It would not be cost-effective to insert new technology into the weapon system at this point in its lifecycle unless it is absolutely necessary. However, at some point in the product's lifecycle, the cost of adopting new technology drops as it becomes more state-of-the-practice. This is the ideal point for performing a technology refresh on the weapon system. If you wait longer, the cost will start to rise again because it is now considered obsolete technology and industry is moving towards adopting the next generation technology. Our TR solution will help identify this ideal point in the product lifecycle for doing cost-effective TR on weapon systems.

continued on page 8

Processing Electronic Assemblies using Chip Scale Components

The standard industry definition of a chip scale package is a package that is < 1.5 times larger in total area than the area of the silicon die. For the purposes of this article, which is intended to discuss the various manufacturing techniques and processes involved in using chip scale packages, we will include processing methods for uBGA's, and direct chip attach technologies.

PWB Design Considerations:
Successful processing of PCB's using chip scale component packages begins with the design of the PWB substrate. Issues such as circuit routing, land pattern via design, solder mask and surface finish all play an integral role in the overall success of the assembly process (Figure 1). Routing complexity of circuit traces and associated vias when using area array devices is increased. In order to compensate for the additional routing complexities, additional substrate layers may be required. The selection of land pattern design and solder mask placement is critical to solder joint integrity, reliability and verification. The use of non-solder mask defined land areas imparts less solder joint stress than does the use of solder mask defined lands. Providing a solder mask dam between the land area and any associated vias will prevent solder scavenging or solder flow into the vias during the reflow process.

An additional concern is the PCB surface finish. In most instances, when using uBGA and chip scale component packages, the fine pitch of the components requires coplanarity of the component land areas.

DESIGN ISSUES: LAND PATTERNS

NON-SMD PADS
- **Mast opening larger than copper (Cu)**
- **Pad size tolerance depends on Cu etching**
- **Location stable**
- **No stress concentrations at pad edge**

VIA SIZE AND LOCATION

common design rules for vias...

Land Size	Ball Pitch	Drill Diameter
0.6mm	1.5mm	0.35mm
0.5mm	1.0mm	0.25mm

micro vias...
0.3mm land and 0.1mm drill size
(pushes limit of drilling)

Lazer drilling, plasma etching or photo-imaging for micro vias can be placed in the solder land which saves board real estate

Figure 1 - Non-solder mask defined land patterns impart less stress at the solder joint to land interface.

The use of a standard HASL (hot air solder level) tin/lead surface finish will not provide the required coplanarity for these fine pitch devices. Alternative surface finishes such as OSP (organic solder preservative), immersion silver or ENIG (electroless nickel/gold) may be required.

General Assembly Considerations:
Some of the process considerations that must be addressed in order to successfully manufacture products using chip scale packages include material dispensing, primarily for underfilling and encapsulation, inspection, cleaning and rework. The characteristics of chip scale components may require modifications to these assembly processes in order to compensate for decreased component package dimensions.

Material Dispensing:
Dispensing of underfills and encapsulants requires more sophisticated equipment than may be required for production of assemblies using standard SMT components. The ability of the dispensing equipment to provide underside heating and the ability to program a variety of dispensing patterns is crucial to assembly processes when using chip scale components. Having the underfill material completely fill the entire area under the uBGA or flip chip is crucial for overcoming CTE mismatch between the PCB substrate and the chip scale component, and for adding enhanced mechanical strength to the component.

When processing assemblies incorporating COB (chip on board) components, the dispensing equipment must be capable of encapsulating the COB component without risking damage to the delicate wire bond connections between the component and the PCB substrate.

Cleaning:
Smaller chip scale components have a considerably different component stand-off height from the PCB substrate than do standard SMT components. In some cases, the stand-off height of a flip chip component may be as little as 0.5 mils (0.0005"). When using a no-clean chemistry in your process, stand off height may or may not become an issue. However, when using a process that requires assembly cleaning, the cleaning equipment must be able to penetrate these stand-off distances to ensure effective residue removal underneath the chip scale component packages. In this case, effective residue removal may require specialized cleaning equipment or modifications to the equipment and/or cleaning process currently in use.

Stencil Printing:
When dealing with chip scale packages, the standard process of stencil printing solder paste onto the PCB substrate using a standard 6 mil thick stencil may not necessarily apply. In most instances, when using flip chip and uBGA components, tacky flux is used in place of solder paste and the deposited material is approximately 2 to 4 mils in height. In some cases, depending on the component pitch,

continued on page 6

PC Board Qualification

With increased board density, the use of alternate surface finishes and the need for high product yield board qualification has become a crucial step in the quality control process. A number of circuit board assemblers and manufacturers have recently reported the use of substandard or unspecified materials in the fabrication of substrates, conductors, laminates, and surface finishes. Changes in laminate and substrate manufacturing have resulted in boards that have increased moisture sensitivity, decreased flexural rigidity, poor adhesive properties, and dielectric properties that are below specifications. Failure analysis laboratory testing at ACI's EMPF has revealed an increase in the number of cases involving substandard PWB manufacturing. Those are just some of the reasons that qualification of new and preexisting PWBs has become crucial to quality control for assemblers and their clients.

There are two main questions that must be asked when examining the quality of printed circuit boards:

1. Does the delivered product meet the fabrication requirements specified in the assembly drawings?

2. Does the printed circuit board exhibit good quality and demonstrate good fabrication process control?

To ensure that the PWB meets the drawing specifications and exhibits good quality, qualification tests are performed. The results of these tests are compared to industry-accepted specifications or guidelines. Although most of the qualification tests are performed by the board supplier, the ultimate responsibility for quality control falls on the assembler. This is the reason that many industry leaders now opt for third party board qualification. Qualifications can be performed efficiently and at low cost in external laboratories that have board qualification programs.

The correct approach to outside PWB qualification is to perform the quality control testing on incoming board lots before board related issues arise. Often, manufacturers find themselves scrambling for PWB failure analysis after assembly, burn-in testing, or after experiencing field returns. One recent EMPF customer requested cross-sections of multiple BGA solder joint locations to determine the root cause of an open circuit from a field return. After transmission X-ray imaging and cross-sectioning confirmed continuity of the solder joint to the board, it was suggested that bare boards from the same lot be investigated. Although the bare board manufacturer approved the lot of boards for use, the test samples sent to the EMPF exhibited nodules and areas with thin plating in the barrel. These areas were below specification and proved unreliable.

One of the most common specifications used to assess the quality of rigid circuit boards is IPC-6012A with Amendment 1. This specification produces generic guidelines for performance and quality specifications for rigid circuit boards. J-STD-003A describes not only the test methods but also provides guidelines for assessing bare circuit board solderability. IPC-A-600F is almost always used in conjunction with 6012A and JSTD-003A because it presents a visual representation of the specifications. There are also numerous other industry-accepted guidelines and specifications that pertain to explicit quality areas such as board design, plating, solder mask, metal foil, dielectric films, support drawings and composite materials. The EMPF utilizes IPC 6012A, 600F, J-STD-003, and TM-650 when qualifying rigid printed boards unless other specifications are applicable.

The first and one of the most essential steps in bare board qualification is visual inspection. This inspection is performed with an unaided eye and a low power (5X-90X) optical microscope. Surface imperfections such as burrs, voids, nicks, scratches, and gouges are quickly identified and compared to the standard. Inspection of the solder mask (solder resist) material involves investigating registration, blisters, delamination, bubbles, and thickness. Some subsurface imperfections such as foreign inclusions, measling/crazing, voids and delamination can be detected from the external visual inspection. For example, Figure 1 shows delamination of the composite substrate just beneath the surface of a printed circuit card.

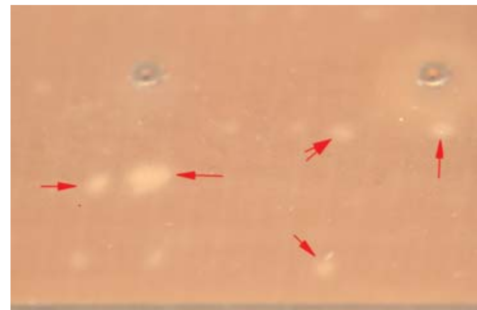

Figure 1. Delaminations beneath the substrate surface are evidenced by color differences. The red arrows highlight the delaminated areas.

Many of the characteristics of the plated through holes are also assessed during external visual inspection. Misregistration, plating or coating defects, diameters and foreign materials are identified and recorded.

Digital imaging enables measurement and assessment of dimensional characteristics such as board thickness, hole size, pattern accuracy, conductor width and spacing, annular ring and registration. These measurements are critical to assessing board quality. For instance, characterizing the annular ring of both supported and unsupported through-holes requires measurement of the hole offset. For high reliability (Class 3) applications, the hole need not be centered in the lands but at least 0.050 mm [0.0020 in] of conductor material must remain between the hole and the edge of the land. Digital imaging is also used before and after adhesion tests are performed on solder resist, surface finishes and metal conductors.

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Tin Whiskers Part II

In the previous edition of Emphasis I introduced Tin (Sn) whiskers as a reliability issue in electronics assembled using Pb - Free solders, as all are essentially based on Sn metallurgy. Along with showing a micrograph of Sn whiskers, several weapons systems were identified which have suffered failures from Sn whiskers in the recent past, e.g. Patriot, F - 15 Radar, Phoenix Missile [1, 2, 3, 4, 5, 6]. Since electronic failure of a deployed system is not an acceptable option, what then is known about predicting failure due to Sn whisker growth?

A study by Dunn in the mid - 80's investigated the length of whiskers formed during room temperature storage, to Sn plated stressed Brass and Steel C - Ring samples [7]. Three different Sn plate types were used: Type I, a "Normal" commercial process; Type II, an "Abnormal" high current density method; and Type III, where "Contamination" by the addition of organics was tested. Analyzing the data obtained from Sn plating on a Brass substrate, we find the activation energy, Q (the thermodynamic force to be over-

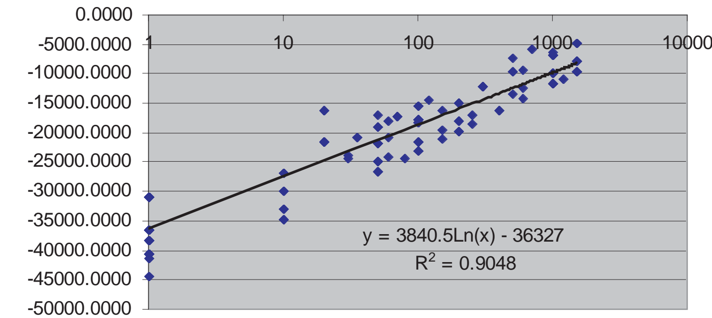

Figure 1: Diffusion, by Arrhenius, Activation Energy vs. Whisker Length

come for growth to occur), varies with whisker length, Figure 1. Therefore, we can directly conclude that the growth of Sn whiskers is not a simple diffusion problem. Closer inspection of the data shows some interesting relationships, Table1.

What is observed is that the plating conditions have a large effect on Q, which is again the activation energy for whisker growth. Additionally, the value of Q found in these experiments is in reasonable agreement with the value given for the self-diffusion of Sn, 25.3 Kcal/Mole [8]. Also, since the activation energy is lowest for Normal plating, one would expect that this coating should be the least susceptible to whisker growth.

Sn Plating	Type 1, Normal	Type II, High Current	Type III, Contaminated
avg Q Kcal/mole	-35.8	-25.6	-12.4
stdev of Q Kcal/mole	3.8	7.8	4.8
A Stress	0.00	3.50	25.00
avg Q Kcal/mole	-29.3	-22.7	-22.0
stdev of Q Kcal/mole	8.7	11.0	12.3

Table 1: Average Activation Energy and Standard Deviations for Sn Plating Type and Imposed Stress in C - Ring Sample

Inspection of the data in Table 1 also shows that plating conditions may have a greater effect on whisker formation than imposed mechanical loads. This is not surprising as electro and/or electroless deposition are atomic transport processes that can develop high internal stress due to dislocations, contaminates, crystal structure selection and epitaxial issues. Since mechanical loading is not atomic in nature but essentially a macro-continuum, loading stress that develops is usually much lower in magnitude.

Work on-going here at ACI is to mitigate the effect of Sn whisker in high reliability systems required by the military. "Even though at the present time no definitive failure model exist for Sn whiskers maintenance and rebuild schedules can be developed from published experimental data." With the Kolmogorov - Johnson - Mehl - Avrami construct [9] ACI has developed a time-based failure criteria for Sn whisker growth in which the Growth coefficients for a specific alloy system is being determined empirically for presently available data, Equation 1:

Equation 1:
$f = 1 - \exp(Kt^n)$ = fraction of material transformed to a whisker
K = constant proportional to self - diffusion and mechanical strain
n = Growth Exponent
t = Time

Exercising this simple model we can mimic the experimental data.

One result obtained using MatLab is shown in Figure 2, where we compare the different activation energies found in

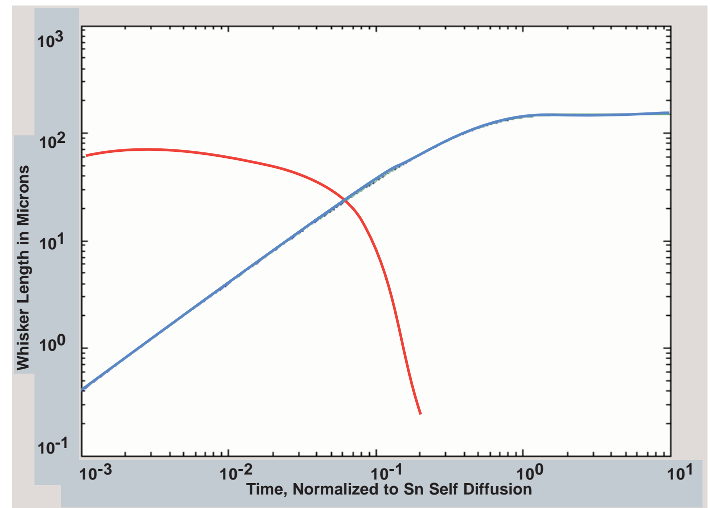

Figure 2: Kolmogorov - Johnson - Mehl - Avrami Analysis for Sn Whisker Growth

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Chip Scale Components (Continued from page 3)

uBGA components can be placed into solder paste; however, the standard height of the deposit will be less than the usual 6 mils customarily used on standard SMT components. When dealing with CSP components, a chemically etched stencil will not yield the precision required and therefore, a laser etching or electroforming stencil manufacturing process will be necessary. On PCB assemblies that incorporate both standard SMT and chip scale packages, step etching the stencil to provide for smaller material deposits on CSP component lands will be necessary. This means a more flexible squeegee blade, usually rubber or urethane, will be needed. Depending on the pitch of the components used on the assembly, it may be necessary to deviate from the standard mesh #3 solder paste and use a mesh size of #5 or #6. The fine mesh solder paste allows for better paste transfer through the stencil apertures and better release from the stencil apertures in fine pitch applications.

Reflow Soldering:
The reflow process for assemblies incorporating chip scale packages will be similar to that used for PCB assemblies using standard SMT components. There may be a need however to lower the volume of the convective air currents inside the reflow chamber when processing assemblies with extremely light weight components such as uBGA and flip chip components.

Summation:
As we have noticed, there are differences in process parameters that must be considered when processing electronic assemblies that require the use of chip scale packages. When these differences are understood and incorporated into the manufacturing processes, overall product yields should be compatible with assemblies using standard SMT components. The incorporation of wire bonding is necessary when using COB (Chip on Board) components, although, the use of chip scale packages on an electronic assembly should be as straightforward as processing with standard SMT components.

If you are faced with incorporating chip scale component packages into your assembly processes, the EMPF offers a highly specialized three day curriculum specific to these needs.

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Tin Whiskers (Continued from page 5)

analyzing the data presented by Dunn.

This analysis is useful as the sensitivity of whisker growth to diffusion temperature and the value of the growth exponent, all well known, can be used to predict whisker length and therefore time to failure due to shorting. "Simply the spacing of the interconnects using Sn based material in microns is locate on the vertical axis of Figure 2. Moving across the diagram when the interconnection pitch distance value intercepts the line we drop down to the X - axis to find the time necessary to grow a whisker of that length. If the interconnection pitch distance is always above the line one would not expect electrical shorts due to whiskers." Therefore, some predictions can be made as to the expected length of service of Pb - free components can be made.

In the final installment of the EMPF's expose' on Sn whiskers the implications of this work on the reliability testing methods and assembly processes will be discussed. Along with a roadmap of the EMPF's future work in the Sn whisker arena.

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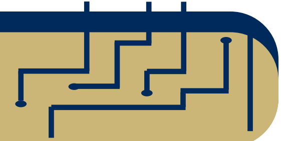

TECH TIPS... REBALLING BGA

It may not be a sound economic decision to reball and reuse a BGA component that has a low initial cost. However, many custom ASIC's and even some "off the shelf" BGA components, because of their complexity, can be very expensive with limited availability and excessively long lead times. For these types of components it can be cost effective to have the ability to reuse components that have failed due to soldering defects. In this article we will discuss some considerations that must be addressed in order to successfully perform reballing of BGA components.

Package Specifications:
It is important to know the component package specifications before attempting a reballing process. These specifications include maximum thermal limits for the component materials, alloy type (either eutectic or high temperature), ball size, moisture sensitivity level and most importantly the manufacturer's recommendations for the maximum number of reflow cycles the component can withstand. This information can be obtained from the component data sheets or directly from the component manufacturer.

Component Substrate Preparation:
Before attaching the new component interconnects the component substrate must be carefully prepped by removing all residual solder. The most efficient method is to use solder braid and a wide blade soldering iron tip. The use of flux during this process will increase the effectiveness of the solder braid in wicking the residual solder from the component substrate. Because of the increased risk of component substrate damage, care must be taken to avoid “scrubbing” the substrate surface with the solder braid and iron tip during this process.

Once all of the residual solder has been removed from the component substrate, it should be thoroughly cleaned using isopropanol alcohol (IPA) to remove any remaining flux residues. The component substrate should then be inspected for any evidence of component substrate damage.

Reballing Process Options For Eutectic Interconnects:
Once the component has been properly prepared for attachment of the new interconnects (balls), a process for accomplishing this task must be selected. The three main options available (see figures 1, 2 and 3) when reballing with eutectic balls are either the preform method, the screen method or a relatively new method based on the screen method which employs a vacuum pick-up for holding the alloy spheres in place. The screen method requires specialized fixturing to place individual solder balls over the corresponding component substrate land pattern. Once all of the lands have a new ball in place, the entire fixture is sent through the reflow process to melt the solder balls onto the component. An alternate method is to use solder preforms in conjunction with a simple frame sized to match the outside dimensions of the component. This method has proven more efficient and reliable than the screen method. The solder ball preforms are available in literally thousands of package configurations and are very easy to use. The preform consists of precisely spaced balls sandwiched between a lamination of cardboard that has been impregnated with a water-soluble flux. Simply apply a water-soluble tacky flux to the component substrate, place the preform onto the component and then place the component into the frame. Reflow the component in the frame to melt the solder balls onto the component substrate. Once the solder preform balls have wetted to the component substrate and resolidified the cardboard can simply be peeled away from the component and cleaned using DI water. This method, although more efficient, does require a bake out cycle of the rebailed components for approximately 24 hours prior to placement of the components onto an assembly.

Figure 1 - Solder reballing screen and fixture. Figure 2 - Vacuum Head and Reballing Fixture. Figure 3 -Solder preform material and fixture

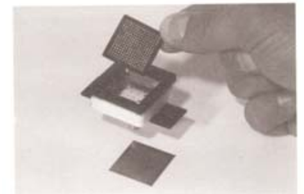

figure 1

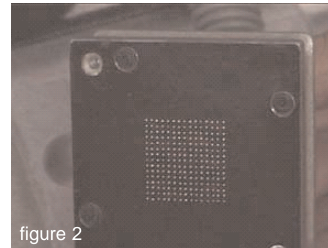

figure 2

figure 3

Reballing Options For High Temperature Interconnects:
When attaching high temperature interconnects to a component, the only viable option is to first screen solder paste onto the component substrate using a solder paste stencil and then placing the high temperature preform into the screened solder paste. The use of a split

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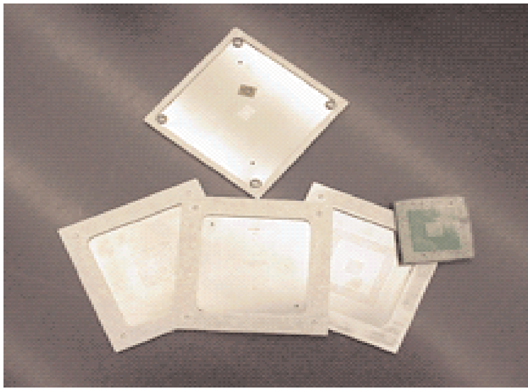
Reballing BGA (continued from pg 7)

vision rework station helps in alignment of the preform to the component. The thermal profile requirements for reflow are also more critical when working with high temperature interconnects as opposed to eutectic. It is critical that the thermal profile be of sufficient heat to fully reflow the eutectic solder paste without reflowing the high temperature interconnect and remain within the maximum component temperature rating.



Solder paste stencil required for High Temperature attachment

Cleaning per flux chemistry:
The cleaning process of the reballed component will depend upon the type of flux chemistry used during the reballing process. If using a no-clean or rosin based flux chemistry, isopropanol alcohol will do a very good job of removing flux residue. When using the solder preform method, which requires the use of water-soluble flux, cleaning in DI water is necessary. Because of possible water absorption by the component during the DI water cleaning process, it is necessary to preform an additional process step of a bake-out cycle of the component prior to use. The recommended bake-out for standard PBGA packages is 24 hours at 125 degrees Celsius. Other component configurations may have different recommendations, which can be obtained from the component data sheet.

When properly performed, the reuse of BGA components is possible and can be very cost effective. Understanding and adherence to the component and process specifications is critical to success. With experience, reballing and reuse of BGA components can be achieved rather easily. The EMPF offers a two-day curriculum on BGA processing and rework which covers all aspects of BGA reballing methods. If you would like additional information please contact the EMPF helpline at 610-362-1320 or log onto the EMPF website at empf.org.

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Technology Refresh (continues from pg 2)

Figure 4 is a solution, that will be implemented as a web-based environment, integrating all of the required tools within a single framework that permits collaborative TR. The tools themselves do not have to be physically located at the same site as the users.

Examples of tools that will be used within our new solution include design tools, roadmapping tools, reliability analysis tools, decision support and optimization tools, as well as any new tools that need to be developed. The users will be able to access the tools and share data across the distributed enterprise using commercial internet capabilities and technology.

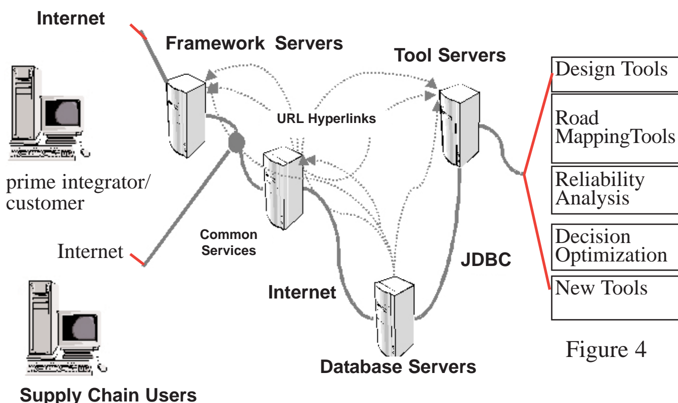

Figure 4

This effort is being jointly supported by SPANS (Supply Chain Practices for Affordable Navy Systems) and Navy ManTech which will combine "best of class" supply chain management with world class manufacturing sustainment and obsolescence mitigation practices.

If you are interested in additional information about TRENT Technology Refresh program, please contact the EMPF Helpline at 610-362-1320.

Author of Article: Mike Guiher
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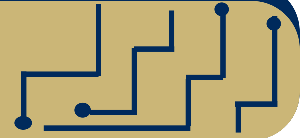
Cut here and save!

MANUFACTURER'S CORNER
McDry Cabinet



At the EMPF, all military and commercial-built PCB assemblies are treated with special care. Moisture build-up in components can have a detrimental effect when reflow temperatures are applied. The proper storage of components and PCB's is essential to any assembly house. The EMPF utilizes a McDry Air Drying Cabinet by Seika Machinery, Inc.

With the increased sophistication of electronic products, moisture sensitive devices (MSD) have become widely used. MSDs present a number of challenges when used in surface mount assemblies as they may suffer internal damage during the manufacturing process if they are not handled and stored according to industry standards.

McDry Cabinet

In surface mount assembly, solder paste is printed onto a PCB. Components are then mounted, and the entire board is sent through a reflow oven. In the reflow process, the entire PCB and component packages are heated along with the solder and component leads. The high reflow temperatures can cause a package containing moisture to swell and crack, affecting the performance and reliability of the component. These problems are normally the result of poor handling and storage of MSDs.

While most of the damaged components may be detected prior to shipment of the final product, many make it to the market place only to fail in the field. Although a component with external cracks may pass pre-shipment functional tests, subsequent high temperature and moisture exposure can induce the transport of ionic contaminants through these openings to the die surface, increasing the potential for failure due to corrosion. Furthermore, internal cracking and delamination can be present even if there is no evidence of external cracks. Ball grid arrays (BGAs) and chip scale packaging (CSPs) are especially sensitive to moisture and damage to these components can be very difficult to detect.

Manufacturers must pay close attention to their handling and storage of MSDs to maximize yields and to ensure the quality of their finished products.

Why do components require low humidity storage?
The plastic packaging used to manufacture surface mount devices (SMD) will absorb moisture from the atmosphere. The high temperatures involved in the vapor phase of reflow soldering can cause the absorbed moisture to expand rapidly, producting internal stress known as "Popcorning." Surface delamination is likely and this delamination results in strain on the bond wires and wire loop. Microcracking may also extend to the outside of the package.

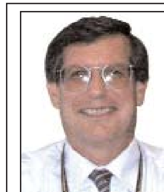
The SMT reflow process exposes devices to higher temperatures (220°C to 245°C) than through-hole devices (135°C to 150° C). The solder reflow processes of concern are convection, Convection/IR, Infrared (IR), vapor phase and hot air rework machines.

Integrated components (ICs) are comprised of dies typically made of silicon, a die pad, which the silicon die rests on, gold or aluminum wire for the electrical connection to the leads and various plastic materials that make up the body of the component. The materials that comprise an integrated component have different thermal expansion ratios, adhesive strengths and material strength characteristics. Moisture absorbed by components vaporizes during the reflow process. The vapor pressure causes delamination and cracking in the plastic component packages. External cracking may appear on the side, top and/or the bottom of the components. As the package wall is often thinnest below the die pad, bottom side cracking is the most common and is very difficult to detect visually. External cracked components can suffer additional damage due to moisture, heat and vibration in the market place. Internally, the vapor pressure can create a void that allows the die paddle to move during temperature cycling. Surface delamination resulting from strain and breakage of the bond wires is likely.

The use of air-dry cabinets is one way of reducing moisture absorption by components. Air drying cabinets, which utilize a strong desiccant, are popular in Asia due to the extreme humidity in the region. Normally, with an air-dry cabinet, the desiccant is recycled automatically with a heating system and does not require replacement. Performance of air-dry cabinets is based on the type and the amount of desiccant used, efficiency of the desiccant recycling system and sealing of the cabinet. Two types of desiccant, silica gel and zeolite, are commonly used. Of the two, zeolite is more efficient at lower Relative Humidity (RH) levels. At 25 °C, 5% RH, zeolite can hold 20% of its weight in water compared to approximately 5.5% for silica gel.

When using an air-dry cabinet, caution must be taken to ensure that the cabinet doors are not opened too frequently or for an extended time. This will cause the RH level within the dry box to become unstable.

Improper storage of moisture sensitive components can lead to low yields and product failures in the market place. With proper handling, packaging and utilization of air-dry cabinets, manufacturers can effectively and efficiently implement proper handling procedures based on IPC/JEDEC specifications. (Reference IPC/JEDEC Standard J-STD-033). Air-drying cabinets are a good option for components that require short term storage at low RH levels. MSDs which must be used shortly after baking, can be easily staged in an air-dry cabinet. Air-dry cabinets are also convenient storage for MSDs to be used for rework. Rework technicians are able to remove the required number of components from the air-dry cabinet and are relieved from constantly having to reseal the remaining MSDs.



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PC Board Qualification (Continued from page 4)

Cross-sections of the circuit board are performed to assess internally observable characteristics. Much of the information about the quality of the fabrication of the circuit board can come from a cross-section of the area in and around a through-hole. The laminate material immediately surrounding the through-hole is divided into zones. Each zone is permitted a certain type of defect such as voids, blisters, or resin recession. Low magnification views of the through-hole cross-section provide information regarding internal through-hole dimensions and foil thickness. These dimensions are compared to the assembly drawings and the industry guidelines.

Plated through-hole cross-sections also yield an abundance of information regarding the bare board manufacturer's process controls. The EMPF examines cross-sections using both low magnification optical microscopy and high magnification scanning electron microcopy (SEM). The target condition for plated through-hole is plating that is uniform and meets the minimum thickness requirements. Quite often some small defects are observed and used as process indicators. These defects could be small nodules, slightly non-uniform plating, nailheading, or burrs that pass acceptability guidelines but indicate improvements may be warranted in the drilling, cleaning, or plating processes. Defects and anomalies such as cracks, lifted lands, or separations are not allowed and indicate poor product quality and reliability concerns. Figure 2 shows a separation between a trace and barrel of a through-hole that would not only fail visual inspection but would also fail electrical continuity tests. Cross-sections should also be performed on bare PWBs after thermal stress. This thermal stress may include thermal cycling or solder pot exposure if specified.

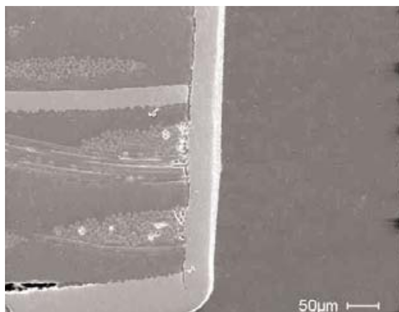

Figure 2. SEM image of trace/barrel separation. Land lift and barrel cracking was also observed.

Bare boards must exhibit acceptable solderability. Circuit board solderability assessment is performed to ensure that fabrication and storage processes do not inhibit solder joint quality. J-STD-003 specifies five specific tests with established accept/reject criteria. Of these the EMPF utilizes Test A (Edge Dip Test), Test C (Solder Float Test), and Test E (Surface Mount Process Simulation Test). Samples used for solder float testing can also be evaluated for plated through-hole integrity after stress. The wetting balance test for bare boards does not have established accept/reject criteria but when coupled with an optical assessment after testing (dip and look) reliable conclusions about board solderability can be made.

PWB cleanliness is a commonly tested quality indicator. When ionic cleanliness is assessed by Resistivity of Solvent Extract (ROSE) methods, the IPC recommends a maximum of 1.56µg of NaCl /cm2. Ion Chromatography (IC) is often coupled with ROSE techniques to help identify individual ionic species.

There are also many tests that are not commonly performed including outgassing, thermal expansion measurement, organic contamination, fungus resistance, and impedance. These tests may be requested by the PWB assembler but are generally reserved for special circumstances. For quality assurance purposes, solderability testing, construction integrity analysis, electrical measurements, environmental testing and visual inspection provide a comprehensive appraisal of the quality of incoming bare printed circuit boards. A program that includes these tests should be an integral part of a good quality assurance plan. A full table of IPC recommended guidelines for rigid circuit boards is available as Appendix A of IPC-6012A.

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CERTIFICATIONS
at the National Center of Excellence for Electronics Manufacturing

IPC-J-STD-001 Instructor Recertification
December 8-9

IPC Challenge
December 10

IPC-A-610 Instructor Recertification
December 11-12

Contact the Registrar for details and registration
610-362-1320 or registrar@empf.org

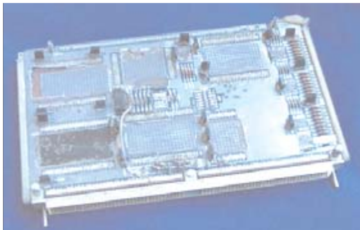
Ask the EMPF Helpline!

Customer Issue: The helpline received a call from Naval Supply Systems Command to provide assistance in removing 300 pin edge connectors from PWB's. "I am looking for an assist in the removal of some connectors from 12 NON-RFI CCA's. I need the connectors to be able to be re-used. The current contractor lacks the skills, materials, and processes to remove the connectors without damaging them. Can you help?"

Initial Inspection

Initial inspection of the circuit card assembly highlighted several challenges involved in removing the flex to rigid edge connector.

1. The connector mates to the board on both sides with flex ribbon style routing.
2. The board is covered with conformal coating, including the edge fingers and flex cable terminations mounted to the board.
3. The flex cable terminations are fragile and easily damaged.
4. The rigid portion of the connector is riveted to the circuit board assembly in three places.
5. Adjacent components interfere with access to some of the flex termination pins.
6. The board has heavy ground planes on both sides.



Step 1
The first step was removing the conformal coating from the flex connection terminations. IPC-7721 procedure 2.3.1 was used to determine the type of coating and the best method for removal. The flex cable was tested to ensure it would not have a negative reaction to using solvents for coating removal. Acetone (solvent method 2.3.2) was used to remove the bulk of the coating. The connector was immersed in the solvent while the flex terminations were scrubbed with an acid brush. Any residual coating was removed using the thermal method (2.3.4). After the conformal coating was successfully removed, the board was thoroughly cleaned with isopropyl alcohol.

Step 2
Any components interfering with access to the connector flex terminations were removed and saved. These components were not required to be "salvaged" or re-used, but our customer did want all components and wiring removed from the CCA to be saved and returned upon project completion.

Step 3
Once the coating and adjacent components were removed, the next step was to remove the solder from the flex terminations and board edge fingers. IPC-7711 procedure 4.1.3 was used as a guideline. RMA flux was liberally applied to the termination area to aid in heat transfer. Solder wick impregnated with RMA flux was selected to ensure compatibility with the external RMA flux already applied. Additional flux was applied to the wick as needed to ensure fast and complete solder removal from each land site.

Step 4
After all excess solder had been removed from the flex termination/CCA land site, the connector was ready for step 5. A small solder fillet was evident between the flex termination and the CCA land. In this step each flex "finger" is heated while a sharp probe is used to lift the finger off the land site. As soon as the "finger" or termination is lifted the soldering iron is moved to the next site. This action was repeated until the entire row of fingers had been lifted from the board land sites.

Step 5
The connector was now completely de-soldered but still hard mounted to the CCA with three rivets. These rivets were removed by drilling out the swagged rivet flange using a mini drill press.

Step 6
The next step was separation. Once the flex was de-soldered and the rivets drilled out, the connector was ready to fall off the CCA. The board was placed on a flat surface and the connector was pulled from the CCA taking care not to damage any of the now free flex connector terminations.

Step 7
The connectors were then thoroughly inspected. A few fingers had exposed copper which occurred during the conformal coating removal process. A solder coating was re-applied to all the connector fingers using the solder pot dip method. This restored the connector to its original condition and provided insurance against future solderability issues.

Conclusion
Upon receipt of the connectors, the NSSC responded, indicating that the EMPF was able to fulfill their requirements, saving them valuable time and avoiding unnecessary expense. Since the connectors were removed from the circuit boards without damaging any of the components, the NSSC was not required to prepare new test modules for bench/flight testing. New test modules would have taken three months to develop, and would have cost approximately $40,000.

Sometimes a call to the EMPF Helpline can make all the difference. If you find yourself in a jam and you do not know which way to turn, call the EMPF Helpline at 610-362-1320. We are always ready to put our team of Engineers and Technicians on your problem, no matter how big or small.

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American Competitiveness Institute - 2004 Course Schedule

Skills

SMT Manufacturing
February 23-27
May 24-28
August 23-27

BGA Manufacturing, Inspection & Rework
January 26-27
April 12-13
July 19-20
November 30 - December 1

Chip Scale Manufacturing
January 21-23
June 21-23
November 15-17

Electronics Manufacturing

Boot Camp A - Week 1
February 2-6
May 10-14
July 26-30
October 4-8

Boot Camp B - Week 2
February 9-13
May 17-21

Certifications

IPC J-STD-001 Instructor Certification
January 5-9
March 1-5
April 19-23
June 7-11
August 9-13
September 13-17
October 18-22

IPC-A-610 Instructor Certification
January 12-16
March 8-12
April 26-30
June 14-18
August 16-20
September 20-24
October 25-29

IPC Challenge
January 28
March 24
May 5
September 1
December 8

WHMA-A-620 Wire Harness Manufacturing (Operator)
January 21-23
June 21-23
November 15-17

J-STD-001 Instructor Recertification
January 26-27
March 22-23
May 3-4
August 30-31
December 6-7

IPC-A-610 Instructor Recertification
January 29-30
March 25-26
May 6-7
September 2-3
December 9-10

IPC-7711/7721 Rework, Repair and Modification of Printed Boards and Electronic Assemblies (Operator)
March 15-26
July 12-23

Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing
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March 8-9
June 17-18
November 1-2

Design for Manufacturability
February 19-20
May 3-4
August 30-31
December 6-7

Failure Analysis and Reliability Testing
March 15-17
November 29-December 1

Characteristic Properties of Materials
March 29-31
October 25-27

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For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

issue:10-03

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