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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

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Electronics Manufacturing Improvements For Precision Guided Weapons

Precision guided weapons have made a significant impact during recent armed conflicts in the war on terrorism. These weapons offer increased accuracy resulting in a greater percentage of enemy targets destroyed with less chance of collateral damage. It is estimated that 70% of the bombs used in the recent war in Iraq (Operation Iraqi Freedom) were guided. Precision guided weapons utilize internal advanced electronics packages such as an inertial measurement unit (IMU) in conjunction with a global positioning system (GPS) to home in on a target. These guided munitions are presently the weapon of choice, and ongoing DOD funding efforts indicate a trend toward the production of smaller guided weapons with enhanced accuracy. The increased use of smaller, more accurate precision guided weapons will rely on electronics manufacturing improvements that enable high-g survivability at a reasonable cost. The EMPF, in conjunction with its industry partners, is actively pursuing manufacturing improvements to produce low-cost IMUs (Figure 1-1) for precision guided munitions applications as part of an ongoing Navy ManTech project.



Figure 1-1

Some of the most widely used guided weapons include the Joint Direct Attack Munition (JDAM), the Paveway laser guided bomb, the Joint Stand-off

Weapon (JSOW) and the Tomahawk missile. Of these, the JDAM weapons have been some of the most widely used. The JDAM is a free-falling bomb (1,000 or 2,000 pounds typically) that has a strap-on guidance kit. The kit includes both GPS and inertial capabilities (functions without external reference or communication) and provides guidance to the otherwise "dumb" bomb. JDAMs can be equipped on the Navy F/A-18 fighter aircraft as well as several Air Force fighters and bomber aircraft. Recent JDAMs have had a publicly reported circular error probable (CEP) accuracy of approximately 10 meters. CEP indicates the radius of a circle that encompasses 50% of the impacts from fired weapons. Recent JDAM accuracy improvement offers the potential for CEPs of around 3 meters.

Efforts are underway to produce a new class of precision guided munitions (PGMs). Examples include the Army's Excalibur and the Navy's Extended Range Guided Munition (ERGM) (Figure 1-2). Extending the precision guidance capability to munitions fired from Navy ships would allow precision strikes on enemy targets that are within range of the shoreline. The ERGM round will be fired from a gun barrel on a Navy ship, have the ability to travel a distance of around 50 miles, and impact within meters of its target. The ERGM round is approximately 5 feet long and includes a rocket motor that fires briefly after leaving the gun barrel. The round will be guided by GPS, but will also have a form of inertial guidance known as an Inertial Measuring Unit (IMU). IMUs are units containing both accelerometers to measure linear acceleration, as well as gyroscopes which measure angular rates. The IMU is used initially after launch for guidance prior to the activation of the GPS and can also be critical during the

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Electronics Manufacturing Improvements for Precision Guided Weapons (continued from page 1)

final stages of the mission. For example, during the final approach to the target the GPS signal can be lost or jammed by the enemy. In this scenario, the IMU can complete the mission by leading the round to the target. Guidance information is processed and used to adjust aerodynamic fins on the side of the round in order to change its flight course.



Figure 1-2

One enabling path to producing precision guided weapons such as ERGMs is to produce functional, gun-hardened IMUs at a reasonable cost. IMUs based on micro electro-mechanical system (MEMS) technology are being considered due to their small size, low-cost and expected long-term reliability. MEMS technology typically refers to small mechanical elements micro-machined into a silicon substrate which also contains circuitry. The U.S. Navy, Army and Air Force are currently committing funds to develop low-cost MEMS IMUs for precision guided munitions.

One of the main technical challenges associated with precision guided munitions is the need for the electronic hardware to operate after withstanding the high g forces (g's) associated with gun firing. Munitions of this type typically experience gun shocks of 10,000 to 20,000 g's. Future applications for the Advanced Gun System [AGS] and the 105mm & 120mm rounds for the Future Combat System [FCS] will encounter environments producing a pull in excess of 20,000 g's.

In addition to high-g survivability, reduced size packaging will enable the production of next generation guidance electronics such as the Deeply Integrated Guidance/ Navigation Unit (DIGNU), which combines the IMU and the GPS receiver into a four to five cubic inch unit. The achievement of smaller, gun-hardened electronic systems may enable new classes of guided weapons such as helicopter fired missiles. Beyond control electronics lies the DOD need for micro-electronic packaging that can be utilized in new fuze programs [MOFA, MFF, HTSF to name a few], seekers and sensors for missiles. The need for high-g survivability, along with the ever increasing demand for higher performance and smaller electronic systems in PGMs, presents the need to establish and demonstrate electronics packaging guidelines for gun-hardened applications.

As part of the effort to manufacture gun-hardened IMUs and related PGM electronics, the EMPF has proposed to develop a set of gun-hardened packaging guidelines based on high-g test data. This guide could be used by numerous DOD manufacturers that make subsystems such as IMUs, GPS receivers, Selective Availability Anti-Spoofing Modules (SAASMs), fuzes and control electronics. The EMPF would select, assemble and test unproven packaging and interconnection approaches in high-g applications. These approaches would provide a definable benefit in terms of high-g survivability, size reduction and cost. The EMPF can leverage its current involvement in the MEMS IMU area as well as its internal packaging capability, knowledge and industry partners. The work performed would establish failure mechanisms for packaging currently being tested in high-g electronics such as wire bonding and flip-chips. Further investigation could include the consideration of more advanced packaging approaches that would enable size reduction techniques such as 3-D chip stacking, stud-bumping of MEMS or the use of folded flex-rigid circuit boards.

The selected packages would be assembled into test articles on the EMPF's demonstration factory floor. The test articles would then be tested at an off-site, established high-g testing facility. The EMPF would use its in-house testing and analysis equipment to perform functional checks and any associated failure analysis. In addition to the high-g survivability data, the EMPF could include the corresponding manufacturing guidelines for package assembly.

Establishing guidelines for gun-hardened electronics would allow all manufacturers of high-g systems and subsystems to draw from a single source for packaging information. The intent would not be to completely mimic the gun-environment, but instead provide high-g test data to enable improved electronic design, component and material decisions for military applications. As next generation products are developed, the high-g test data for packaging would provide a foundation of confidence that certain packaging approaches have merit and should be investigated further. This would not only contribute to the fielding of current and next generation PGMs, but would do so with an emphasis on inexpensive manufacturable packaging solutions.

The level of investment from multiple DOD branches demonstrates the current interest in precision guided munitions. Through the efforts of the Navy ManTech program, the manufacturing technology needed to expand and enhance the attributes of electronics packaging for precision guided munitions can lead to their increased availability and affordability, thus meeting the battlefield needs of today and tomorrow.



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Characteristic Properties of Materials Used in Electronic Assemblies

An important factor in ensuring the reliability of an electronic assembly is understanding the raw material properties and characteristics from which electronic components and assemblies are made. As part of its comprehensive line-up of electronics manufacturing training, the EMPF Training Center offers a three-day course entitled "Characteristic Properties of Materials Used in Electronics Manufacturing" that deals exclusively with the selection, use and compatibility of materials used in electronic assemblies. The course focuses on the correlation of material properties and characteristics to product development, manufacturability and quality.

The objective is to prepare participants to make informed decisions about the materials used in their components and assemblies, and to identify how material properties influence the performance and reliability of the end product. Engineers, quality managers, technicians and designers will benefit by gaining an understanding of the fundamentals of material properties with a focus on translating complicated concepts into practical applications for design and production related scenarios. A wide range of topics are covered including:

- ◆Ceramic and composite substrates
- ◆Fluxes
- ◆Semiconductors
- ◆Tin-lead and lead-free solder alloys
- ◆Plastic packaging
- ◆Wire bonds
- ◆Underfills and adhesives
- ◆Solderability
- ◆Contamination
- ◆Advanced packaging materials
- ◆Board finishes
- ◆Viscosity
- ◆Electrical properties
- ◆Corrosion
- ◆Solderability and wetting
- ◆Diffusion
- ◆Lead materials
- ◆Coatings
- ◆Thermal expansion
- ◆Mechanical properties
- ◆Thermal and chemical properties

Curriculum

1) Selection

Material selection is fundamental for effective design engineering. The ability to interpret data sheets and assess the material's impact on the performance of a product is crucial for reliable performance. Successful participants in the course will attain the technical knowledge required to make informed decisions regarding the selection of fluxes, paste, adhesives, substrates, cleaning materials, conformal coatings and other common interconnect materials.

2) Behavior

The actual behavior of a material can vary from the theoretical or expected performance of the material in various situations. Because of this, the factors that affect material behavior such as temperature, humidity, contamination, processing and additives are covered in depth in order to pre-

pare the participants to effectively troubleshoot and correct variations in material behavior.

3) Testing

The testing of material properties and the associated collection of test data is widely understood to be the key to understanding material interactions. Material testing serves as the basis for performing failure analysis and also provides information on the quality of incoming and outgoing products. Inspection test equipment and the associated inspection techniques are demonstrated for a wide range of materials and assemblies. This provides the participants with both knowledge of the common failure modes observed in electronics manufacturing and the proper techniques for evaluating them.

Participants are first exposed to the definitions of material properties. These material properties are then linked to the chemistry and physics that influence product yield, reliability and quality. Throughout the course there are a number of hands-on laboratory exercises and demonstrations to further enhance the understanding of the topics and relate them to actual manufacturing situations. Several of the laboratory exercises include:

- ◆Metallography of intermetallics and solders using scanning electron microscopy (SEM)
- ◆Glass transition temperature measurement of polymer materials using differential scanning calorimetry (DSC)
- ◆Characterization of halide content of fluxes and circuit boards
- ◆Wire bonding
- ◆Oxide characterization and quantification

Course participants are encouraged to bring sample products to use in the hands-on laboratory exercises. This will assist in relating the comprehensive course material to each participant's specific manufacturing applications. Successful completion of the three day course will ensure that each attendee will leave with a better understanding of material properties and prepare them to use the information to improve product reliability and manufacturability in their respective organizations.



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Solderability Testing and the Transition from Lead to Lead Free Solders

Lead has been linked to various medical disorders and physical development problems, especially in children. Historically, contamination has been a consequence of improper disposal of leaded waste, residues left over from internal combustion engines or the direct leaching of lead into potable water sources. The regulatory agencies within the United States have begun to act in accord with the Environmental Protection Agency's (EPA) 1973 proclamation to gradually reduce lead in gasoline. In addition, the Consumer Product Safety Commission banned the sale of paint with greater than 0.06% lead in 1978. Within the electronics industry, the EPA's Toxic Release Inventory implemented a reduction in reporting thresholds for lead amounts from 10,000 lbs to 100 lbs per year starting in 1999. Outside the US, the European Council and European Parliament have set July 1, 2006 as a target date for a ban on hazardous materials such as lead as per the Waste Electrical and Electronic Equipment (WEEE) Directive and the Restriction of Hazardous Substances (RoHS) Directive. The Japanese Ministry of Industry and Trade proclaimed that lead usage will be reduced 67% by 2005. As a result, the shift in PWA manufacturing overseas will impact domestic customers [1].

The effects of Lead regulatory changes on the Electronics Manufacturing Industry

Solder consisting of tin/lead (63/37 wt %, also known as SN63) is considered a eutectic. In metallurgical terms eutectic refers to the lowest melting mixture of the two metals (183°C). Historically, this ratio of tin to lead solder has dictated the types of materials which could be used in PWB base material and component packages.

In combinations other than that of eutectic, solder does not melt or become liquid at a specific temperature but has a melting range. As a result, the use of non-eutectic combinations would influence the soldering process since partial melting would occur. The alloys shown in Table 2-1 are being evaluated by many manufacturers for future production applications and in some selected cases, are being used in the production process.

Alloy	Melting Temperature
SnBi	138°C
SnAgCuBi	215°C
*SnAgCu	218°C
SnAg	221°C
SnAgCuSb	222°C
SnCu	227°C
SnSb	240°C

Table 2-1

* This alloy has been identified as a primary combination with two specific variations coming from Japan (96.5% tin/3.0% silver/0.5% copper) and North American Electronics Manufacturing Initiative (NEMI) (95.5% tin/3.9% silver/0.6 % copper). [3]

However, it is critical to the electronics manufacturing industry that there be a consensus for the metallurgical makeup of solder as well as a recognized Design for Manufacturing (DFM). The DFM must include solderability testing, as acceptable wetting will be affected by the solder alloy. The current specifications for solderability testing within the US are IPC J-STD-002B "Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires" and IPC J-STD-003A "Solderability Tests for Printed Boards".

There are a number of tests for evaluation of solderability. Dip & Look and Wetting Balance analysis are the most common and the focus of this article. According to Wassink [7] there are two groups of tests: Those that evaluate the parameters which create good wetting (i.e. rate of wetting and wetting angle) and those that evaluate the results of these parameters. Acceptable visual solderability is indicated by a "continuous solder coating free from defects for a minimum of 95% of the critical area. Anomalies other than de-wetting, non-wetting and pin holes are not cause for rejection." [7] Another trait of acceptable solderability is a shiny appearance, as newly flowed eutectic tin/lead solder gleams in light. In contrast, lead free solder is often dull in appearance due to the fact that tin is often the major component and the oxides of tin are more stable than those of lead (i.e. lower heat of formation- ΔH_f [4]) (SnO -69 cal/mol, SnO₂ -143cal/mol, PbO -53cal/mol, PbO₂-67cal/mol).

Quantitative solderability testing (Wetting Balance testing) measures the wetting force (Figure 3-1) which is dependent upon the density and surface tension of the solder. This test does not have established accept/reject criteria but does provide suggested evaluation criteria (Table 2-2).

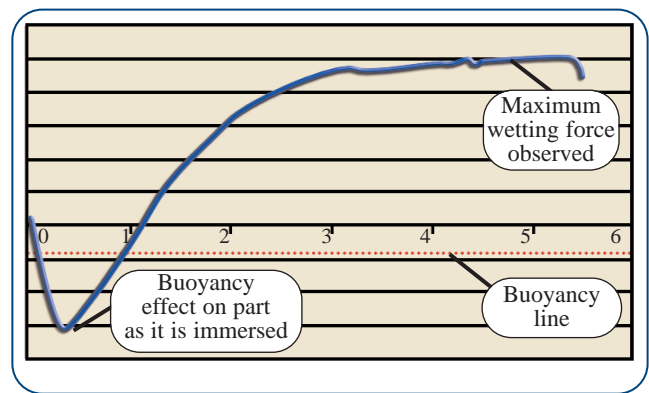


Figure 3-1**

**Note: This graph is from an actual wetting balance analysis and is portrayed opposite of the direction of the actual forces involved. (Buoyancy is an upward force while solder wetting is a downward force).

The time to reach the maximum wetting force along with the absolute value of the force are of great importance as both will be impacted by the ability of the flux to remove oxide layers common in lead free solder.

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Solderability Testing and the Transition from Lead to Lead Free Solders (continued from page 4)

Parameter	Description	Acceptability Set A	Acceptability Set B
T ₀	Time to buoyancy corrected zero	≤ 1 second	≤ 2 seconds
F ₂	Wetting force at 2 seconds	50% of maximum theoretical wetting force at or before two seconds	Positive value at or below two seconds
F ₅	Wetting force at 5 seconds	At or above the positive value at F ₂	At or above the value of F ₂
AA	Integrated value of area of the wetting curve from start of test	Area calculated using sample buoyancy and 50% maximum theoretical force.	> zero

Table 2-2 (courtesy of IPC)

Considerations for Lead Free Testing

In addition to evaluation criteria, test requirements could be affected by lead regulation. Currently the two standards mentioned earlier utilize an RMA type flux. Since surface oxides are more likely with the lead free systems, higher activity fluxes, which leave residues that require more aggressive cleaning, may be required. Additionally, performing the testing in a blanket of nitrogen may be necessary since dross removal is more frequently needed with lead free solders.

The current pot temperature for eutectic tin/lead solder is 245 ± 5°C (62 degrees above the melting point). Referencing the melting temperatures of the various solders listed in Table 2-1, the necessary pot temperatures would average 272 °C. As a result, contamination from some of the substrate materials shown below in Table 2-3 could occur as these materials may be susceptible to thermal degradation despite the short contact times.

Glass Transition Temperature	
Material	T _g
FR-4 epoxy	125°C
FR-4 with phenolic	170°C
Thermount	240°C
Polyimide	250°C

Table 2-3

The requirement to steam age parts has been designated for those components and connectors that experience extended time periods between testing and soldering (>6 months) and have either limited thermal exposure or multiple thermal exposures before soldering. This current requirement assumes that "properly applied tin and tin/lead coatings can withstand the steam conditioning environment well beyond the eight hours specified and may survive natural aging well beyond 12 months". [5], [6] Steam aging samples prior to testing may become more critical as the shelf-life of components and boards is reduced.

During the transition from lead-based to lead free solders, vendors will also find themselves maintaining multiple solder baths to avoid cross-contamination.

What has been done so far to answer these questions?

In 2000, the Lead Free Component Focus Group (an industry consortium) compared the component solderability of tin, tin/copper, nickel/palladium, and nickel/palladium/gold finishes and the PWB solderability of Hot Air Solder Leveling (HASAL), Organic Solder Preserve (OSP) and Electro less Nickel Immersion Gold (ENIG) finishes. Standard RMA flux and three solder systems (Sn63 / Pb37, Sn95.5 / Ag4.0 / Cu0.5, Sn99.3 / Cu0.7) were used in the study. The results are as follows:

- ◆ The four component finishes are suitable for lead free systems.
- ◆ The "Dip and Look" test lacks the robustness to accurately predict board level solderability.
- ◆ Wetting times and wetting forces were degraded for various leaded packages using Sn/Ag/Cu solder vs. Sn/Pb at 235 °C.
- ◆ ENIG and OSP are acceptable as lead-free finishes.
- ◆ Temperature has a direct influence over solderability as wetting times improved with all the alloys in comparison to SN63 (Figures 3-2, 3-3 & 3-4).

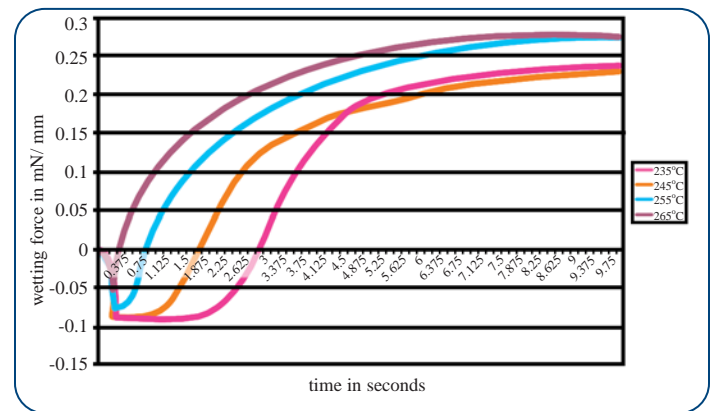


Figure 3-2: Hasal finish with Sn/Ag/Cu solder

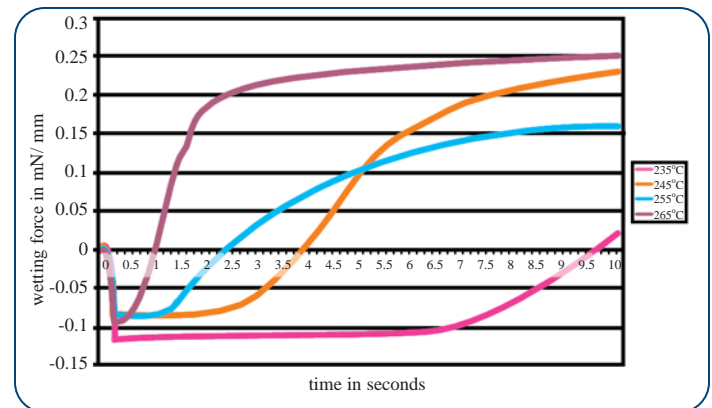


Figure 3-3: Hasal finish with Sn/Cu solder
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Since the inception of Chip Scale Packages (CSPs) and Flip Chips (FCs), the increasing demand for smaller electronic component packages has intensified the focus on related manufacturing processes to find methods to increase their reliability. The capillary underfill process was developed to provide the necessary thermo-mechanical reinforcement to mitigate the coefficient of thermal expansion (CTE) mismatch, thus preventing early failure. The CTE is the difference in expansion and contraction between the board and the component, which weakens the solder joints. Flip Chips and CSP devices, such as Micro BGAs, require the underfill epoxy to absorb the stress induced by the CTE mismatch.

The capillary underfill process has become a time consuming and costly part of the manufacturing process. The process requires labor intensive steps such as the application of tacky flux material (used to solder the eutectic bump to the pad), cleaning the assembly, dispensing the capillary underfill (typically in an L shaped pattern around the device- allowing capillary flow) and curing the capillary underfill in a batch or re-flow oven.

The development of re-flow encapsulants, which are also known as no-flow underfills, has helped to reduce manufacturing costs. The use of these materials involves a one-component system that combines both tacky flux and underfill encapsulants. This combination reduces equipment requirements, increases throughput and decreases the labor costs by eliminating over half of the assembly steps required by the standard encapsulant process (Figure 2-1). Additionally, only a single re-flow is required using a standard SnPb profile to solder the eutectic bumps and cure the encapsulant.

The following Tech Tips focus on some of the dispensing parameters and patterns, die placement settings, re-flow profile settings and storage and handling steps used in the processing of FC or CSP components with a re-flow encapsulant.

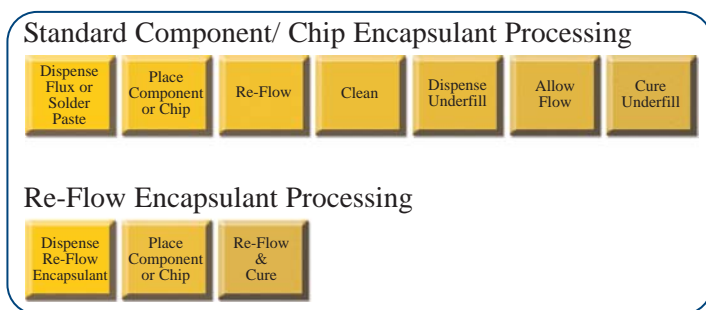


Figure 2-1*

Dispensing

Unlike traditional capillary underfills, most re-flow encapsulants do not require the substrate or the needle to be heated. As is typical in many dispensing applications, the size of the needle is based on the size of the component. A 23-gauge needle is recommended for most FC processes.

The size of the component also determines the dispense quantity of re-flow encapsulant that is required. Table 1-1 shows examples of typical FC body sizes and the dispense quantity required.

Die Size (mil x mil)	Die Size (mm x mm)	Dispense Pattern	Dispense Quantity
250 x 250	6.4 x 6.4	Dot	6 mg
500 x 500	12.7 x 12.7	Dot or Asterisk	25 mg
700 x 700	17.8 x 17.8	Asterisk (cross)	50 mg

Table 1-1

Table 1-1 also delineates the recommended dispense patterns based on the component's size. The dot and asterisk (cross) patterns are common to compression flow processes. These patterns allow for domed deposits, minimizing the probability of voiding that could be caused by the placement of FCs or CSPs. A dot pattern is typically dispensed for smaller dies, whereas the asterisk pattern applies to larger dies. Figure 2-2 shows an example of how these geometries appear from both a top and side view.

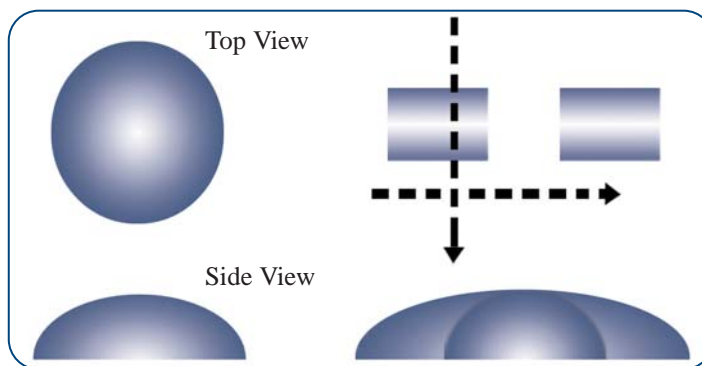


Figure 2-2*

Die placement settings

Die placement settings are important to the re-flow encapsulant process because they facilitate the compression flow of the material. Table 1-2 lists the recommended parameters when placing an FC or CSP package. Placement dwell times may vary depending on component size.

Component Size (mil x mil)	Component Placement Speed	Component Placement Force	Placement Dwell Time
250 x 250	15mm/s	250 grams	0.1 - 1.0 seconds
500 x 500	15mm/s	800 grams	0.1 - 1.0 seconds

Table 1-2

continued on page 7



Figure 2-3 shows an illustration of how a die component would be placed on top of an asterisk (cross) pattern.

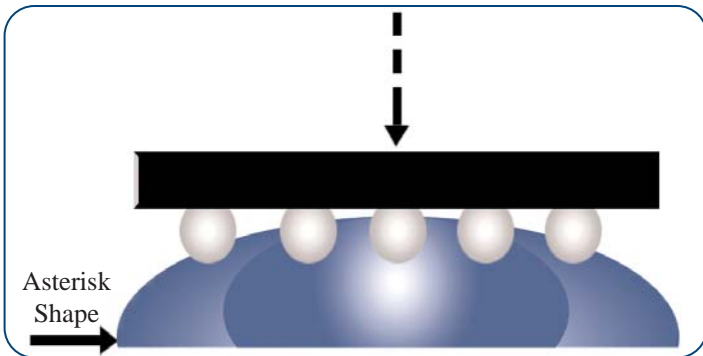


Figure 2-3*

Re-flow profile settings

The latest developed re-flow encapsulants are engineered to facilitate a single pass re-flow process using a standard Sn63Pb37 re-flow profile. This profile (Figure 2-4) will have the bumps soldered to the pads as well as encapsulate the component. This works in conjunction with other SMD components that are populated and soldered with standard Sn63Pb37 solder paste.

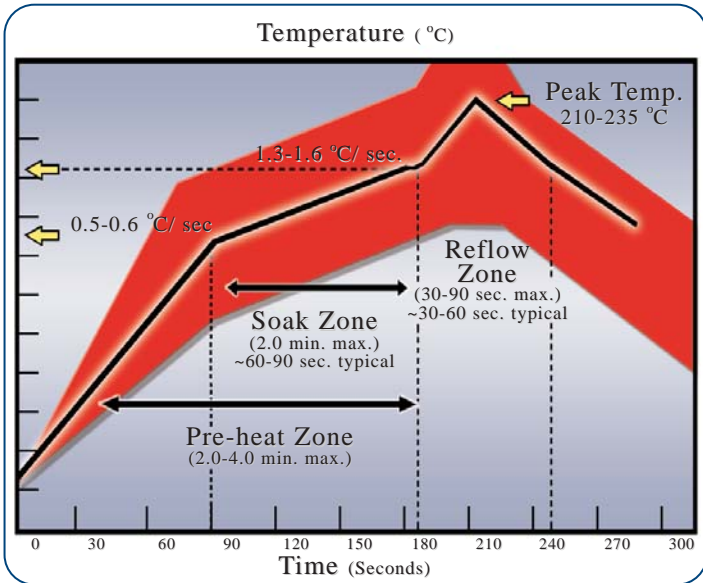


Figure 2-4*

Storage and Handling

The storage of re-flow encapsulants is similar to other encapsulating materials in that they must be stored below -40°C until the expiration date or time of use. The "pot life" is defined as the time of use at ambient conditions, which for most reflow encapsulants is 24 hours.

The material should also be thawed according to the manufacturer's recommendations. Table 1-3 shows a "time to thaw" example of Kester's SECURE® 9126 Re-flow Encapsulant. Most of these times are standard. However,

checking the thaw specifications of your manufacturer is advised. It is also recommended that the material be used completely or discarded, and not re-frozen in storage.

Packaging	Time to Thaw
10 cc syringe	60 minutes
30 cc syringe	90 minutes
6 oz cartridge	2 hours
12 oz cartridge	2 hours

Table 1-3

*Images courtesy of Kester



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Contact the EMPF Helpline @
610-362-1320 for information
on any of the following
Laboratory Services

Environmental Laboratory Capabilities:

- ◆ Thermal cycling: -65 to +155C, ramp rate 10C/minute maximum
- ◆ Thermal shock: -75 to +160C, <5 seconds switching time
- ◆ High temperature exposure, to +160C
- ◆ Low temperature exposure, to -75C
- ◆ Highly accelerated stress testing (HAST) (temp/humidity/pressure),
- ◆ Temperatures to 143C max, Humidity 75 to 98% RH, Pressure .02 to .2 MPa (maximum similar to 2 atmospheres)
- ◆ Vibration, to 1 pound-weight UUT, sine, sine-sweep, and random
- ◆ Humidity/heat, typically 85% RH/85°C, capable to 95%/-15 to +90°C
- ◆ Salt fog
- ◆ Rain

Materials Laboratory/ Failure Analysis Capabilities:

- ◆ Optical microscopy with digital imaging
- ◆ Micro-sectioning
- ◆ SEM (scanning electron microscope) analysis
- ◆ Fourier transform infrared spectroscopy
- ◆ Ion Chromatography
- ◆ Wetting balance
- ◆ Transmission X-ray imaging
- ◆ Shear testing
- ◆ Reduced oxide solderability activation (ROSA)
- ◆ Ultra-violet visible (UV-Vis) spectroscopy
- ◆ Sequential electrochemical reduction analysis (SERA)
- ◆ 'Level 1' component analysis

Use of COTS Components in DoD Applications

The use of commercial parts in electronics military systems is certainly not a new concept and has been in use for many years. However, there is an increasing trend of the reduced availability of military specified component parts in many military applications due to the fact that the manufacturers of the military versions ("Mil Spec") either no longer exist or are no longer interested in such cost expenditures for so little return. The military customer represents less than 1% of the semiconductor market today.

The need to use COTS (commercial-off-the-shelf) components in military systems has not reduced the requirement for reliable operation in harsh environments. It is the EMPF's challenge to make use of COTS components either through the determination of methods for upgrading them or by determining if the characteristics of the "commercial" parts reliably meet or exceed those listed in the specifications.

The question of how to validate the use of these components must be addressed with every new design. At the component level, up-screening is an effective way to ensure that commercial parts will meet the electrical and environmental parameters required by the intended system. Extended, or life-cycle, screening will provide some assurance that the parts will have long-term reliability. The practice of such testing is known as Ruggedization.

Testing

Some of the tests that apply are often referred to as environmental stress screening (ESS) and are performed at the EMPF. These include thermal cycling, high and low temperature exposure, highly accelerated stress testing or screening (HAST or HASS), highly accelerated life testing (HALT), vibration, shock, humidity, salt fog, rain, explosive atmosphere, low pressure (altitude) and fungus testing. Excluding HAST/HASS and HALT, those listed would be typical of environmental testing for a military contract design of a printed circuit board or electronic unit, and are therefore a part of the COTS qualification process at the EMPF.

Accelerated test methods such as HAST allow exposure for the purpose of simulating the advanced aging of the device under test (DUT). HAST includes relative humidity (RH) up to 98% and temperatures up to 120°C with simultaneous pressure (versus simply 80°C temperature and 85% RH in a normal thermal chamber).

Testing is necessary since MTBF calculated from MIL-HDBK-217 falls short. This is mostly due to the fact that new component models have not been updated in the MIL-HDBK and therefore it is not always possible to calculate a valid MTBF.

Finite Element Analysis (FEA) is utilized to determine the reliability (the stresses, strains, structural integrity, and fatigue life) of components, and is advisable as an accompaniment to testing.

Analysis of Failures

Any failures found during testing (exposure to environmental conditions) may be subject to failure mode analysis. This typically includes both optical inspection and micro-sectioning of the part for SEM (scanning electron microscope) analysis in order to find the cause of failure.

One example of a failure is a printed circuit board fracture with the failure mode occurring 1) when the heavy heat sink is residing on the outer two inch perimeter of the board, 2) at temperatures below -20°C, and 3) when subject to 20g shock. Another example of a failure is when an integrated circuit produces internal open or short circuiting over extended periods of time. Here, methods such as HALT will assist in mimicking those conditions. SEM analysis may then reveal that an overlay of dissimilar metals has caused intermetallic layer growth and fractures to form an open circuit, or tin whisker growth to form a short circuit.

EMPF Testing and Failure Analysis

The EMPF's environmental and materials labs allow for exposure testing and failure analysis required of COTS parts used in military applications. A list of the testing services available can be found on page 5.

Example of COTS Components Ruggedization For a DoD Application

Assisting the Standard Missile program, the EMPF up-screened components associated with the EMMA (Electronic Miniaturization for Missiles Application) program for the Autopilot system. The usage of COTS components reduced manufacturing costs by 66% and reduced system volume by 80% over the 20 year old previous design using Mil Spec Parts. The remaining volume was then able to be used for the Flight Termination System (FTS).

Vibration and thermal cycling (-55 to +125°C) was performed for components with various packaging types that included SOT, TQFP, PBGA, TBGA, flip chip, and LFCSP while mounted on three different substrates. Other devices including amplifiers, A/D converters, power MOSFETs and memory components were subjected to environmental exposure followed by functional testing and analysis.

Limiting the Testing Required

The comparison of a MIL-STD-883 specified part with its commercial equivalent may reveal the limited nature of the commercial part's intended use. However, the full military specified version may not be required either. Depending on the circuit, military platform and intended environment, the specifications for testing must be decided specific to the application.

By determining if "Mil Spec" parts are absolutely necessary for the system's performance requirements, the ruggedization testing can be limited in scope. The particular application in the circuit, physical position with respect to thermal dissipation and mission duration further limit or add to the testing required for any given part. Thermal cycling is a typ-

continued on page 9

Use of COTS Components in DoD Applications (continued from page 8)

ical starting point for testing, as real aging includes exposure to daily changes in temperature. A second choice is often vibration, as it will reveal the mechanical fragility of an item, particularly in regard to its packaging.

The electrical requirements of a COTS part may fall short of those of its military predecessor. However, if the part is intended as a portion of a redesign, it may be specified less critically while associated new circuitry makes up the balance of tolerances. These tolerances may have actually been required of the circuit instead of the part. The compromises involved in choosing similar rather than identical replacements can be discovered in SMT magazine, November 2000: "The Use Of Commercial Components in a High Reliability Environment".

Conclusion

Up-screening components before assembly and age-simulation for failure rate prediction provides the reassurance of risk reduction. The key to reducing the scope of reliability testing for COTS parts in a military system is to determine what specifications truly must be "Mil-Spec" to meet the performance requirements of the application. Secondly, the re-design of associated circuitry to alleviate the critical nature of a single part may be an option should a drop-in COTS item be unavailable. This maintains the integrity of the next higher assembly. When the COTS part itself must adhere to certain specifications, the performance parameters under harsh operating conditions must be verified.



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Solderability Testing and the Transition from Lead to Lead Free Solders (continued from page 5)

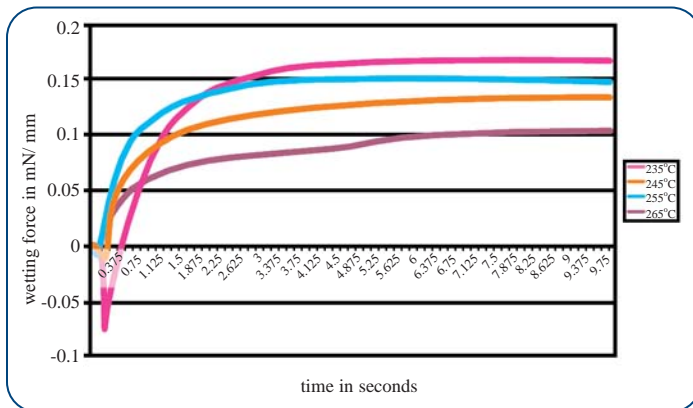


Figure 3-4: Hasal finish with SN63 solder

The affect of temperature on board solderability was also confirmed by NSF Center for Advanced Vehicle Electronics, Auburn Univ. [9]. The push for VOC free fluxes and their influence in lead-free systems was investigated [10]. This study showed that the lead-free systems did not perform as well as the incumbent eutectic tin/lead control. It was observed that better wetting was observed in systems which contained less Cu, confirming the consensus that the addition of copper degrades wet-ability.

As mentioned earlier, the consensus of the NEMI and JAPAN is a solder of composition Sn/Ag/Cu. Their recent study examined how subtle variations of silver content (3 to 4%) may influence solderability testing. The findings of the IPC study showed no significant difference in wetting balance parameters for the variations.

What does this mean for the future of electronic assemblies?

The technical staff at the EMPF has researched the manufacturing challenges associated with lead-free soldering for several years and has developed a considerable level of

expertise in lead-free solder alternatives, with an emphasis on military applications. A technical core competency focus at the EMPF will continue to be working with and finding solutions for the difficulties associated with the inevitable transition to lead free solders. The need to establish a consensus on the composition of a lead free solder is critical, as this will determine solderability test requirements (i.e. flux & temperature). Criteria for accepting/ rejecting components must also be determined.

There is a likelihood that Class I applications will switch readily over to lead free solders in the near-term, as the reliability requirements are not as stringent as that of Class II and Class III applications. The EMPF will remain actively involved in representing the specific needs of military applications at the board level (Class III) during the development of solderability standards. Overseas, the commercial industry appears to be ahead of its domestic counter parts as approved lead free solders have already appeared on the market.

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Manufacturers' Corner... BTU Oven



Surface Mount re-flow soldering is the most widely accepted method of attaching electronic components to a printed circuit board. Applications vary depending on the components, atmosphere and solder type, all of which dictate the process profile. Finer pitches and challenging materials, particularly lead-free solders, continue to reduce the process window and require optimum thermal re-flow performance. The resulting solder joint forms a mechanical and electrical connection to the surface of a conductive land pattern that does not utilize through-holes or terminals.

The EMPF is utilizing the BTU Pyramax 98 oven (Figure 4-1) in a wide variety of applications such as SMT Boot Camp training (helping SMT students develop solder re-flow profiles), testing lead-free processes, wafer bump re-flow for lead-based or lead-free solders, nitrogen process development, high temperature applications for military projects and lead-free process development to assist manufacturers with their specific process challenges. Most recently, the EMPF utilized the BTU Pyramax 98 for a lead-free workshop.



Figure 4-1

SMT re-flow is typically performed using forced air, convection dominant ovens utilizing either air or nitrogen as the process gas. The typical lead-free process profiles consist of four phases: preheat, soak, reflow and cool down. For thermal profiles, the following parameters for air temperature settings must be considered for each zone to achieve satisfactory results: Nitrogen flow rate (to achieve the appropriate reduction of the oxygen levels required by the paste manufacturer), conveyor speed, cooling rate and fan speed (optional on some ovens). Lead-free processing presents additional challenges. For example, since re-flow temperatures are higher than that of Eutectic solder, the difference between re-flow temperature and maximum component temperature ratings is smaller. This results in a significantly reduced process window.

The central component of any solder re-flow system is its heat transfer technology. The BTU oven uses jet impingement convection, which is an efficient means of transferring heat to a relatively flat surface such as a printed circuit board (PCB). A small, singular jet of high-speed gas can transfer its temperature to a surface very effectively at the spot where it impinges on the surface. An array of such jets is able to extend that high heat transfer coefficient across the surface, so long as the impinging gases have clearance to escape between the jets. In the BTU furnace design, the size and velocity of the jets, and the spacing of the arrays have been optimized using Computational Fluid Dynamics (CFD) computer modeling.

The benefits of the very high heat transfer coefficients available with jet impingement are that both small and heavy components heat up quickly, and the oven zone temperature set points can be closer to the desired product temperatures. As a result, small components do not overheat while large components are heating up. All of the components on a board go through the same narrow process window, which is a necessity for a Lead-free PCB assembly. In less effective, convection dominant and radiantly heated ovens, the zone temperature set points are higher in order to achieve the same profile for the heavy components. This leads to larger temperature differences across the PCB assembly and a less controlled process.

The Pyramax 98 has the process capability and flexibility to accommodate all thermal profile recipes developed at the EMPF. If you would like to see a demonstration of this oven at the EMPF, please call Jeff Stong at 610-362-1200 x-224.



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Customer issue: The customer wanted to obtain wire bond pull data on immersed silver substrates. The substrates were to be baked at varying lengths of time (0, 2, 4 and 8 hours at 125 degrees Celsius) prior to processing and testing.

Investigation Technique

Each substrate was labeled on the back side as to the length of time for baking prior to performing the wire bonding.

Wire Bonding

- ◆ The boards to be tested were 6.1 cm [2 7/16 in.] by 3.8 cm [1.5 in.].
- ◆ Wire bonds were made using a FEK Delvotec 5430 at 102kHz, and a bond weight of 15.
- ◆ 200 bonds using 1.25 mil diameter aluminum wire with a loop height of 3.50 mil were tested.

Pull Testing

Wire bond pull tests were performed on a Dage model 4000 at K&S in Horsham, PA using the following parameters:

- ◆ 100g cartridge (2013480)
- ◆ Test speed of 700m/sec
- ◆ Test load of 20g
- ◆ Fall back of 30%

Results

A summary of the wire bond pull testing results is displayed in Table 3-1.

Bake Time (Hrs.)	0	2	4	8
Mean Pull Force (g)	5.051	4.848	4.176	4.770
Standard Deviation	2.525	2.080	2.066	2.228
Total Measurements	45	47	48	54

Table 3-1

Wire Bond Fracture Locations

Each test board possessed four wire bonds for a total of 8 contact bonds per board. All 8 of these locations were examined under a 400X optical microscope on three boards from each aging time. In addition, a scanning electron microscope (SEM) was used to examine the fractured areas on two of the boards.

- ◆ After wire bond pull testing, the fractures were noted to occur within the wire at all locations except for about 40% of the wire bond source sites where the fractures occurred at the wire/pad interface.
- ◆ When pull testing a strong wire bond, the break should occur in the wire, leaving behind a remnant from the wire-to-pad bond (Figure 5-1). This situation was observed to occur on 47 out of the 48 destination bond sites which were inspected from various aging times. Inspection of the wire bond source sites (Figure 5-2) revealed that 20 out of 48 wire bond sites inspected did not show any wire remnant, indicating that the separation

occurred at the wire/pad interface. Table 3-2 lists the inspection results per aging time. Listed are the number of bond sites that visibly exhibited failure at the pad surface.

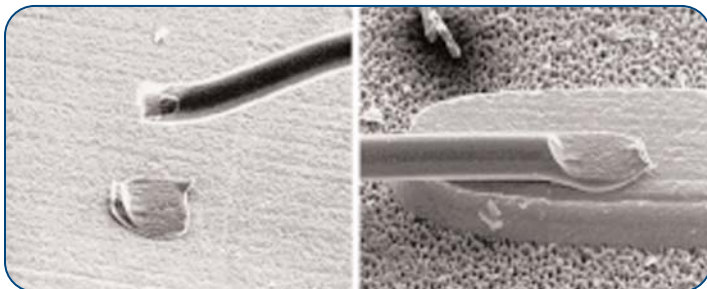


Figure 5-1

Figure 5-2

Aging Time	Destination Sites	Source Sites
0 hours	0 of 12	7 of 12
2 hours	1 of 12	7 of 12
4 hours	0 of 12	2 of 12
8 hours	0 of 12	5 of 12
<i>Totals</i>	<i>1 of 48</i>	<i>20 of 48</i>

Table 3-2

Conclusions

The fracture mechanism was not influenced by the aging time, but was affected by bond location. The destination sites exhibited failure within the wire in nearly every instance. One possible reason for this could be that the wire near the destination site was crimped and positioned at a greater angle than the wire at the source site. This created a stress concentration point that could have made the wire more susceptible to fracture.

Recommendations

To ensure the bondability and reliability of wire bonds, the bonding surface must be free of any contaminants. Cleaning is the fundamental process needed prior to wire bonding. Optimum bonding parameters are the key for reliability and maintaining high yields.

The key variables that affect bonding include:

- ◆ Bonding force and pressure uniformity
- ◆ Specified bonding temperature
- ◆ Bonding time
- ◆ Ultrasonic frequency and power



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