

American Competitiveness Institute

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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

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Use of Commercial Technology in DoD RF Modules

The current movement in the commercial RF electronics industry is toward plastic packages and assemblies that are lighter and cost less than traditional hermetic ceramic module packages. Since commercial applications account for 98% of the electronic components market share, market trends are not heavily influenced by the needs of Department of Defense (DoD) applications.

Specifically, the recent use of plastic materials to encapsulate the Laterally Diffused Metal Oxide Semiconductor (LDMOS) Monolithic Microwave Integrated Circuit (MMIC) radio frequency (RF) power amplifier chips for electro-optical power amplifiers is typical of the industry trend towards the wide-spread use of plastic packages to lower costs. Additionally, the movement to position RF hardware on commercial cellular towers close to the antennae to avoid costly and performance limiting amplification at a remote (ground level) site supports the trend from a performance standpoint. Both examples support the goal of many commercial competitors of all plastic electronics for RF and RF power applications. Once again, commercial applications are driving electronics technology trends.

It is interesting to note that these commercial applications of plastic packaging for RF electronics have DoD analogies. The LDMOS RF amplifier noted could easily have application on the digital battlefield, and the cell tower application is roughly analogous to Naval ship mast-head located radars and communications gear.

The EMPF is helping to define where the DoD can take advantage of this commercial trend in RF packaging. The potential cost and weight benefits that the commercial world currently enjoys could then become available to the DoD.

One commercial method towards all-plastic RF electronic packaging is to utilize the concept of "Near Hermeticity." This concept allows the use of high performance organic materials for encapsulation to provide the required amount of hermeticity, as measured by the Highly Accelerated Stress Test (HAST) for the particular application. Hermeticity has a range of values as evidenced by the graph in Figure 1-1, which shows a progression from simple plastic packages up to a true hermetic DIP response, and then to HAST testing.

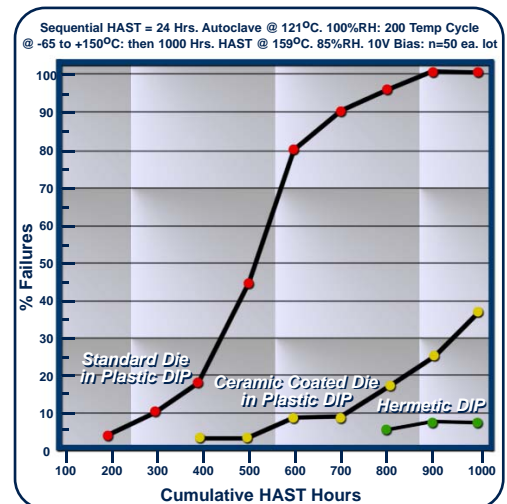


Figure 1-1

This continuum of hermeticity, from simple consumer item plastic packaging (inadequate for high reliability military applications) to the extremely high reliability of the hermetic DIP (Dual Inline Package), has been exploited by Dow Corning in their Chip Seal process (See Figure 1-1 for generalized Highly Accelerated Stress Testing (HAST) testing results). HAST is a measure of the degree of hermeticity exhibited by a test specimen). Chip Seal is a process of multi-level passivation applied at the wafer level to impart some level of her-

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meticity to each of the chips on the wafer. The results of HAST testing for some representative examples are shown in Figure 1-2. Commercial alternatives to the Dow Corning wafer level hermetic coating are now available as less expensive, near-hermetic alternatives for RF packaging applications.

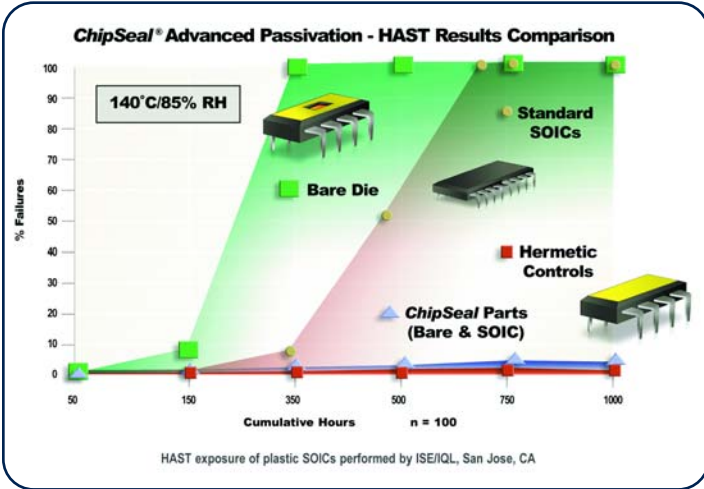


Figure 1-2

This technique, applying such a multi-stage hermetic coating to the RF die in the wafer form, represents significant cost and weight advantages over traditional ceramic packaging and is actively being pursued by some major defense contractors. However, this technique does require that all chips in a several-chip assembly be coated while they are still in wafer form, thus raising a significant logistical issue.

To further lower the cost of RF electronic modules, and also allow the application of a hermetic coating to a multi-chip assembly, the commercial industry, as well as the EMPF and some major defense contractors, are actively pursuing the introduction of all-organic, near-hermetic solutions. Unlike the wafer level chipseal type chip coating, these can be applied at the modular level to any and all kinds of chips used in the RF module, providing much greater flexibility to the module assembler.

A relatively new plastic material is now in the process of becoming a commercially available alternative to heavy, costly ceramics. It is called Liquid Crystal Polymer (LCP). LCP refers to the broad class of thermoplastic polymers that typically have long, rigid backbones with flexible ends. Polyester is the most common polymer backbone used in LCPs. When extruded, the rigid rods align in the flow direction and the polymer takes on some crystalline properties. Because of these crystalline properties and the excellent dielectric properties of the base (polyester-like resin), the properties of LCP are proving to be ideal for RF applications.

A comparison of the prosperities of the presently employed ceramic packages and the LCP plastic alternative that is becoming available is shown in Table 1-1.

Property	Typical Ceramic	Liquid Crystal Polymer
Dielectric Constant	9.7	2.9
Dielectric Loss Tangent	0.009	0.002
Heat Deflection Temperature, °C	>1000 °C	270 °C
Cost per sq. in.	Approx. \$10	Approx. \$2
Water Absorption	0.0 %	0.025%
Density grams/cu.cm.	4.0	1.2
Hermetic (MIL-STD-882)	Yes	Yes

Table 1-1

LCP Plastic has a significant weight and cost advantage over traditional ceramic RF circuit substrates.

Navy aircraft require RF avionics that can withstand a wide range of operating temperatures and high levels of shock and vibration. Current rack-mounted circuit boards need heavy air or water cooling hardware so that thermally induced strains do not cause electronic components to fail at the surface mounted solder joints. Foster-Miller has made electronic substrates with LCP dielectric layers from 0.05 to 0.5 mm thickness to support and interconnect electronic chips in these critical RF applications.

Foster-Miller controlled the processing of the LCP substrates to achieve a coefficient of thermal expansion (CTE) matched to the printed circuits and electronic chips. Testing showed that these new interconnect substrates were more reliable and were lighter in weight than ceramic, fluoropolymers, or fiber reinforced composite dielectric substrates. Foster-Miller's LCP circuit substrate technology was licensed to a major electronic laminate manufacturer and is being used in both flexible and rigid printed circuit boards for high-speed digital and RF circuit applications. There are already some applications of the LCP technology within the DoD. But the major implication of the use of LCP for RF electronic packaging is the ability of the LCP material to be used to make a "near hermetic" enclosure or package, thus saving the weight and cost of the traditional ceramic package while still displaying sufficient hermeticity for the DoD application.

Shown in Figure 1-3 are typical Foster-Miller LCP based RF circuit board and hermetic enclosure shapes, courtesy of Foster-Miller and Quantum Leap Packaging. The Foster-Miller RF commercial circuit substrate and package products shown in Figure 1-3 might be usable on military RF modules.

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Ask the EMPF Helpline!

Customer Issue: The EMPF recently received a phone call from a customer looking for assistance with analyzing a surface mount component package (0.300" Wide SOIC package) for a digital-to-analog converter chip. This chip had failed a mechanical shock test of approximately 100Gs at the customer's site. Furthermore, the customer requested level 1 component failure analysis to be performed.

The customer supplied the EMPF with two converter component packages. One had been damaged, and one was known to be functional (as a reference). The customer's end use for this component was for an electrical circuit breaker product line.

Analysis Technique/Methodology

- ◆ External visual inspection of package
- ◆ Electrical inspection of package using a Tektronix 370A curve tracer
- ◆ X-ray inspection
- ◆ Decapsulation per EMPF procedure AP0600-1
- ◆ Optical inspection using an Olympus SZX12 microscope
- ◆ Optical inspection using an Amray 1830I scanning electron microscope

Results

The incoming assessment of the device was completed and recorded, showing the device markings and package/lead formation. No major mechanical damage was observed during this process. During the test, the failed device was analyzed and compared to the functioning device using a data sheet supplied by customer.

Using a Tektronix I-V curve tracer, a curve trace analysis was performed on two test pins for both packages. A I-V curve tracer is an indispensable tool for troubleshooting circuits and testing semiconductor components. On the failed device, the curve tracer analysis of the I-V characteristics revealed an open connection from pin #24 to pin #1, and from pin #24 to pin #22. The internal lead-frame was inspected with a live X-ray system with rotational capability. No anomalies were found in the lead frame, ball, or wedge bonds.

The plastic mold compound encapsulant was then selectively removed (per EMPF procedure AP0600-1) from the failed device to expose the active die. The device was heated to approximately 125°C and subjected to fuming nitric acid until the bond wires and die were exposed. The device was then cleaned in a methyl alcohol bath. The ball bond on pin 24 and its corresponding bond pad appeared to be intact during optical inspection, but some smearing of metal was observed to be surrounding the ball. Previously bonded bond pads were also observed next to bond wire pad #12 and #13, from which the metal in the missing ball area was removed. This indicates that some level of re-work was most likely performed.

The exposed lead-frame, bond wires and die surfaces were inspected using a stereo microscope with digital

image capture. A scanning electron microscope (SEM) was also used to examine the device in accordance with EMPF lab procedure AO0280-1. When compared to other bonds on the die, the device exhibiting a failure showed ball bond separation from the pad on pin #24. Generally, the ball bonds also appeared somewhat flat and over-compressed. The slight separation was also accompanied by metallization smearing and build-up around the ball due to over-bonding. Subsequent examination of the bottom surface of the ball bond and the remaining bond pad surface showed major metallization transfer from the pad onto the ball bond.

Conclusions

On pin #24, the device failed a continuity test due to ball-bond/ bond-pad separation. A very loose connection most likely existed in the device and became opened during mechanical shock testing. The ball bonds were over-bonded to the pads, thus causing metallization smear which lead to separation susceptibility. Intermetallic formation was satisfactory, but after lifting the bond, large metal lift-out was observed and was attributed to over-compression and/ or excess bonding energy. Bonds that were attached to unused bond pads also appeared to be removed and/ or re-worked.

Recommendations

The EMPF recommended that the customer review this problem with the device manufacturer. They were advised to address their concerns that were related to the specific device lot and date code included with this device, and also the predicted survivability that was assessed during shock testing. Developing a method for screening the devices that are received, and also implementing a corrective action process with the device manufacturer for fixing the over-bonding condition would be beneficial in removing suspect devices, and preventing this problem with future devices.

If you have any questions about package testing and analysis, or any topics related to electronics manufacturing, please contact the EMPF helpline at (610) 362-1320. A manufacturing expert will be able to offer technical insight and appropriate advice regarding your concerns.



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Packaging Technologies for C-band and Above

In order to describe the behavior of packaging technologies that operate at microwave frequencies, the appropriate spectrum must be defined and disclosed. If a circuit is digital and its clock speed is above 10MHz, or when an analog circuit operates at 100MHz to 100GHz, it can be considered to be high-speed or microwave, respectively. The microwave band usually refers to the centimeter wavelength range of the spectrum (300 MHz to 30 GHz). This article is focused on packaging behavior in C-band (4-8 GHz) and above. The Navy is interested in a number of platforms, including RF modules, operating within this frequency range. To satisfy the need for this technology, the EMPF has been challenged to develop suitable packaging.

Short development cycles, higher density, more functionality, greater performance and miniaturization are all driving factors in the development of electronic systems. Miniaturization, portability, cost and performance have been the driving force for the evolution of packaging and system-on-package approaches in RF, microwave and millimeter wave applications. As a result of rapidly emerging technologies and applications, the technology boundaries between semiconductor, packaging and system technologies are no longer clear, and must be considered concurrently in a system-level approach to optimize the substrate design. Electronic packaging evolution involves systems, technology, and material considerations.

Microwave systems have unique packaging requirements as a result of the relatively short wave length of the electromagnetic energy, the functions performed by the systems, and the types of devices used. Major packaging issues, which must be addressed in any microwave system, are coupling and interconnection. Very special microwave packaging technologies are employed because interaction between circuits on the same or neighboring substrates or printed wiring boards can occur and weaken circuit performance. Circuit performance could be altered by the undesirable coupling of a signal from one part of the circuit to another. At microwave frequencies, circuit components must be considered as distributed elements rather than lumped elements because of the relatively short wavelengths. In microwave circuitry, as opposed to DC or low frequency circuits, signals carried by both the conductors and dielectrics are influenced by the high frequency properties of the dielectric. Thus, conductors are chosen for their electrical conductivity and compatibility with the dielectric to which they are attached or bonded.

To more easily discuss packaging features, RF electronic packaging can be categorized into three levels as shown in Figure 2-1.

- ◆ Level 1: die, flip chip, wire bond
- ◆ Level 2: package to substrate, solder joint, BGA, AFP, CSP
- ◆ Level 3: system interconnections, connectors, cables

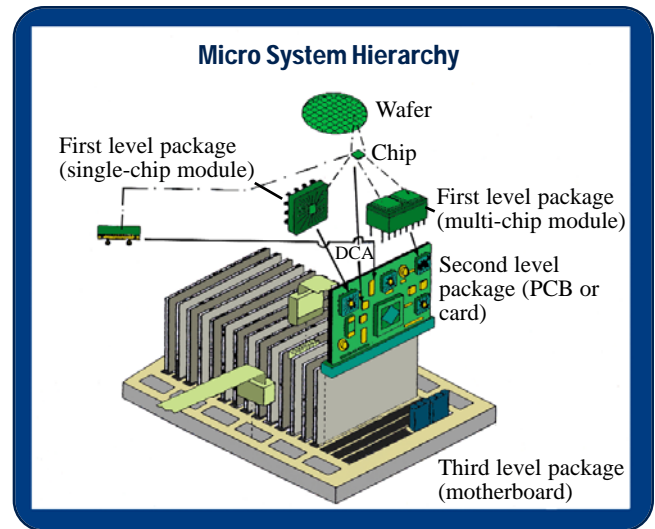


Figure 2-1

Wire bond interconnection is an example of joining technology which is applicable up to frequencies of 10GHz. If higher frequencies are needed, tighter control of the geometry is required. An alternative method is flip chip technology, which easily supports applications up to 60 GHz. For higher frequencies, special designs or the use of embedded chip technology is required. Wire bonding remains, however, the most popular type of chip interconnection.

Wire bonding is very cost effective, but its RF performance is limited. Wire bond design variables include parasitic inductance, which is frequency dependent. Wire bonding forms a loop between the wire bond, substrate and chip. Since the loop behaves as an inductor, the loop form, maximum height and span influence parasitics. Encapsulation material also influences the capacitance of the wire-to-ground. Additionally, the loss tangent of the encapsulant influences behavior. As stated above, coupling between adjacent wire bonds needs to be addressed. This effect is frequency dependent because coupling increases with frequency. Encapsulation with a dielectric constant greater than one increases the capacitive coupling.

One of the fastest growing chip interconnection methods is flip chip technology. Due to the small geometries involved, it is especially suitable for RF applications. RF performance is influenced by the height of flip chip interconnections, bump pitch and underfill material. Compared to wire bonds, flip chips have short connection lengths, a global bonding wiring process and repeatability of bonding, all of which minimize the tuning of the RF functions. Flip chips offer high levels of integration, reductions in device cost due to the elimination of backside wafer lapping (i.e. MMIC), improvements in module performance, and reductions in package size. In the case of T/R modules, up to a 2X reduction in assembly cost is achieved due to the elimination of the epoxy component attachment process. Flip chip technology requires an understanding of the effects between

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Use of Commercial Technology in DoD RF Modules (continued from page 2)

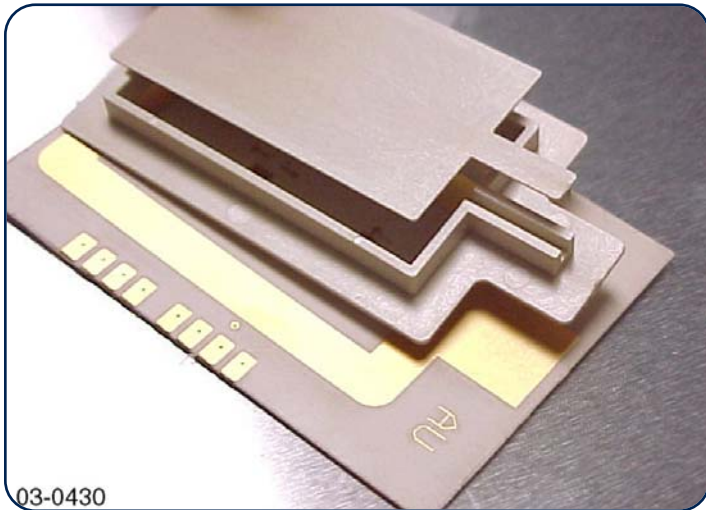


Figure 1-3

Major defense contractors are currently in active pursuit of applications of the LCP material in phased array radars (T/R modules) and avionics for use within the DoD. The incentive for this work is the promise of lower cost and lighter weight with sufficient hermeticity as compared to the traditional ceramic alternative.

In summary, the commercial industry has been actively engaged in replacing the heavy and costly hermetic ceramic packages used for RF packaging with lighter, less expensive, and adequate hermetic plastic packages for more than fifteen years, mostly for low frequency and digital applications. The EMPF is working to begin to introduce these relatively new commercial near hermetic technologies into higher frequency DoD RF packaging applications in order to gain similar benefits.

References

1) Byrne, Robert C., National semiconductor corporation, Santa Clara, CA and Camilletti, Robert C., Dow Corning Corporation Midland, MI "Reliability without Hermeticity (RWOH) for Integrated Circuits-Sealed Chips for Hermetic-Like Properties".



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Packaging Technologies for C-band and Above (continued from page 4)

adjacent solder bumps. These effects can be observed in mutual capacitance, inductance, self-inductance and capacitance. One effect of wafer level packaging is that solder bumps have parasitic inductance and capacitance. Inductance is important for power integrity analysis whereas parasitic capacitance is important to signal integrity analysis. Tests have shown that a lesser degree of parasitic capacitance produces better signal integrity (in the test vehicle).

Any high frequency design must consider packaging to produce the ideal platform. The design should consider all three levels of packaging. Finally, potential negatives such as parasitics must be limited.



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For information on any of the following Laboratory Services,
please contact the EMPF Helpline @ 610-362-1320.



Environmental Laboratory Capabilities:

- ◆ Thermal cycling: -65 to +155C, ramp rate 10C/minute maximum
- ◆ Thermal shock: -75 to +160C, <5 seconds switching time
- ◆ High temperature exposure, to +160C
- ◆ Low temperature exposure, to -75C
- ◆ Highly accelerated stress testing (HAST) (temp/humidity/pressure),
- ◆ Temperatures to 143C max, Humidity 75 to 98% RH, Pressure .02 to .2 MPa (maximum similar to 2 atmospheres)
- ◆ Vibration, to 1 pound-weight UUT, sine, sine-sweep, and random
- ◆ Humidity/heat, typically 85% RH/85°C, capable to 95%/-15 to +90°C
- ◆ Salt fog
- ◆ Rain

Materials Laboratory/ Failure Analysis Capabilities:

- ◆ Optical microscopy with digital imaging
- ◆ Micro-sectioning
- ◆ SEM (scanning electron microscope) analysis
- ◆ Fourier transform infrared spectroscopy
- ◆ Ion Chromatography
- ◆ Wetting balance
- ◆ Transmission X-ray imaging
- ◆ Shear testing
- ◆ Reduced oxide solderability activation (ROSA)
- ◆ Ultra-violet visible (UV-Vis) spectroscopy
- ◆ Sequential electrochemical reduction analysis (SERA)
- ◆ Level 1 component analysis

PWB Qualification: Peel Testing

There are many ways to qualify a PWB manufacturer. Tests such as plated through-hole inspection, solderability, and cleanliness testing are common methods for assessing the general quality of a bare circuit board. There are however, additional tests that are not as well known that help in the understanding of a PWB manufacturer's capabilities. These tests often yield quantifiable data that can be used to compare the performance of boards manufactured from competing board houses (Figure 3-1). Pull testing is one such test, and is used to assess the bond strength of copper traces (peel test) and the plated through holes (land bond strength integrity test). The method is used to determine the strength of a material in a uni-axial direction. Both the peel test and land bond integrity strength test determine circuit board manufacturing quality. Other uni-axial mechanical stress tests include shear and compression stress tests.

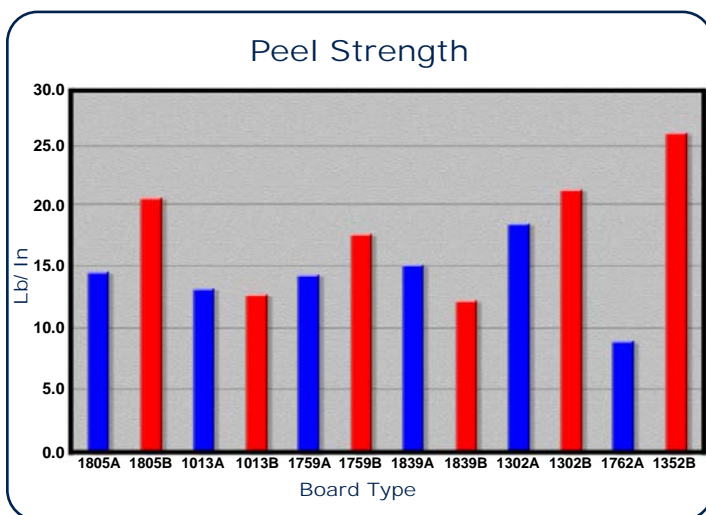


Figure 3-1

The IPC has recommended test methods for mechanical testing, to include peel testing, in section 2.4 of their TM-650 documents. The test performed at the EMPF is a modified version of these tests. To perform a trace peel test, a trace has to be raised and clamped by the digital force gauge. The circuit board is held fast to the testing surface, and the trace is then "peeled" perpendicularly from the surface of the circuit board. Specifications set by the IPC require a circuit board trace peel test to have a peel rate of two inches per minute.

The base-line of the test at the EMPF is a modification of several tests, which include peel strength of metallic clad laminates at ambient and elevated temperatures, and peel strength of flexible printed wiring materials.

The peel strength of metallic clad laminates at ambient temperature (IPC TM-650 2.4.8) was designed to determine the peel strength of metallic cladding. There are a few different ways this test may be performed depending upon a manufacturer's need. Testing a sample in its received condition requires no additional preparation before testing. However, a thermal or chemical preparation may be applied to deter-

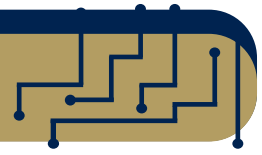
mine their effects on the peel strength of the metallic clad laminates. The samples would be stressed as required before the actual peel test, which is identical for all three types of metallic clad laminates at ambient temperature. IPC TM-650 2.4.8.1 (peel strength, metal foil, key-hole method for thin laminates) describes the procedure for the peel test. Regardless of preparation, each test requires a minimum of two strips measuring 0.125 inches wide (etched) per specimen. The tab to be clamped onto the load applicator is to be no longer than 0.5 inches long. The specimen is fixed to maintain a peel at an angle of 90°. A force is applied in the vertical direction at 2 inches per minute, and the specimen must be peeled for a minimum of 1 inch. The actual width of the test strip is then measured and recorded along with minimum load. Finally, the peel strength is calculated using an IPC supplied formula.

The test called peel strength of metallic clad laminates at elevated temperature (IPC TM-650 2.4.8.2a) is performed while submerged in a hot liquid. Two test strips are etched-once lengthwise for each clad side, and once cross-wise for each clad side. The dimensions of the test strip are the same as the ambient peel test. Before the test, the specimen must be pre-conditioned by baking for four hours at 125°C. The actual test is performed when the specimen is immersed 1 inch below the surface of the hot liquid. After the specimen is peeled, the sample is observed for laminate degradation.

The IPC TM-650 2.4.3 peel strength test applies heat to the sample via hot air. The method requires that the sample be placed into a hot air chamber after pre-conditioning for a minimum of 60 minutes. The specimen is then clamped and the test is performed in accordance with IPC TM-650 2.4.8.1. Upon completion of the peel test, the sample is observed for laminate degradation as it was with the hot liquid method.

For flexible printed wiring materials, IPC TM-650 2.4.9 defines the procedure for determining the bond strength of copper foil clad. Depending upon the test method, the sample is to be etched to 9 inches by 0.125 inches or cut to 9 inches by 0.5 inches. In all cases the peel must be mounted onto a sliding plate or free wheeling rotary drum test fixture to ensure that the peel is at an angle of 90° for the length of the peel. A minimum of 4 specimens, two from the machined direction and two from the transverse direction, must be prepared. Method A describes the procedure for received etched specimens. Method B is virtually the same with the exception of the sample having to be cut to the required size using a Thwing Albert sample cutter. Once cut, the specimens may follow Method A procedures. In methods C and D, specimens are thermally stressed by performing a solder float prior to peel testing. The specimens must first be conditioned by being dried in a circulating oven maintained at 135°C for an hour. The samples are then floated (conductor side down) just beneath the surface of the molten solder at 288°C for at least 5 seconds. During immersion, the sample is agitated from side-to-side. The

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Determining the root cause of a failure is crucial so that the appropriate corrective actions can be taken to prevent reoccurrence or to remedy ongoing problems. The investigation of the failure should indicate if the failure was caused by materials, design, process, or conditions. There are a few tips that apply to engineers, designers, managers and technicians when evaluating failures. These tips apply to both internal investigations and also to situations where outside laboratories are contracted for analytical services.

Confirm Before beginning

The first step in an effective analysis of failures is to confirm that the failure has occurred. Confirmation may be as simple as reviewing test data or it may actually require re-testing of an assembly. Optimally, images of the sample should be obtained and recorded before the investigation begins. Isolating a failure helps the investigator by reducing time and the area of investigation. This increases the probability of identifying the root cause, increases the efficiency of the analysis, reduces cost, and prevents mis-diagnosis. One key theme to remember during the analysis is that documentation is critical.

Become a researcher

Determining the root cause of failures is like being a detective or investigative reporter. The key to a rapid and thorough investigation is gathering as much information as possible before disturbing the sample. Collect a sample history that includes component data sheets and the characteristics of the failure (short, open, etc.). Some key questions to ask when investigating component, board or assembly failures include:

- ◆ What is the suspected failure?
- ◆ What are the symptoms?
- ◆ Where is the failure located?
- ◆ What is in the area of the failure (next to and on the opposite side)?
- ◆ What was happening when the failure occurred?
- ◆ Was the device under power?
- ◆ Was it undergoing any stress testing (heat, cycling, vibration, etc.)?
- ◆ Did it work prior to assembly, prior to shipping, or did it ever work?
- ◆ How many failures are like this one?

If there are other similar failures, look for shared characteristics such as production lots, operators, manufacturing sites, process changes, a change in materials, a change in vendor or a change made by a vendor. Assumptions made about failure modes without gathering as much information as possible can result in incomplete or incorrect conclusions. The BGA failures like those observed from the board shown in Figure 4-1 were once thought to be a result of poor processing. Review of the reflow profile, storage conditions, component and solder paste data sheets, and BGA design guidelines revealed possible alternative causes of

failure. The answers to the previous questions should help to build a chronicle that may then be used to focus the investigation.



Figure 4-1

Bring it into focus

Review all of the gathered information and form a hypothesis of what may have occurred. Many find it beneficial to use peers to brainstorm about theories of what could have occurred. The majority of problems that occur in electronics manufacturing are not new, and the chances of someone having experienced the same issue are high. Experiments can then be modeled from past experimental design. The experiments should involve proven techniques with methods and specifications that are clearly outlined.

Select test methods

At this stage, determining the conditions (possible events) that could have caused functional changes is a key objective. With this information, the investigator is now ready to choose the correct analytical techniques and test equipment to determine the root cause of the failure. There are usually multiple test methods available to test for a particular problem or defect. Complimentary test methods can be selected, but care should be taken to ensure that conflicting results are not produced. Table 2-1 outlines some of the most common test methods for BGA failures.

Test Method	Applicable Conditions
Transmission X-ray Imaging	voids, open circuits, misalignment, wire bond failure, bridging, short circuits, warping, poor reflow conditions
Solderability Testing	poor solderability, voiding, misalignment, open circuits
Acoustic Microscopy	die attach failure, popcorning, board delamination, warping
Optical Microscopy	poor design, intermittent open circuits, poor solderability
Scanning Electron Microscopy	voiding, wetting/solderability, solder joint fractures, open circuits, intermetallic formation, contamination, improper reflow profile, poor design
Decapsulation/Die Surface Analysis	wire bond failure, die related fabrication issues, ESD and electrical overstress
Cleanliness Testing	contamination, short circuits

Table 2-1

continued on page 8

Cut here and save!

PWB Qualification: Peel Testing (continued from page 6)

sample is then peeled as described in method A. Method D is executed in the same manner with the exception that the sample must be cut to the specified size. When utilizing methods E and F, samples are exposed to five temperature cycles prior to testing. As with methods B and D, F samples must be cut to a specified size.

All methods are evaluated by averaging the chart recordings for both specimens over the entire peel length. The width of the conductor is measured and recorded to calculate the peel strength in pounds per inch of width.

Peel and land bond strength testing can be performed with standard shear/tensile testing equipment. However, the test equipment must have the capability to maintain displacement at a constant rate. Some common electronics pull testing equipment maintains the force applied to the sample as a constant and neglects the rate at which the sample is displaced. This does not conform to the intentions of the peel strength test method. A low-cost alternative to expensive automated pull/shear testing machines are manual units affixed with sensitive force gauges. The operation of these types of tools is simple. The test specimen is clamped or fixed to the sample stage. The opposite end of the test specimen is then clamped fast to the digital force gauge. The digital force gauge is then raised or lowered manually (the EMPF's unit utilized a hand crank wheel) to create a tensile or compressive force in the test specimen. However, these machines, like the automated constant force testers, do not displace the sample at a constant rate.

The EMPF utilizes a cost-effective modification to the manual equipment. An electric motor is applied to the hand crank using a timing belt/pulley assembly. The selected motor has enough torque to ensure the distance rate remains constant. The motor is affixed to a stand, ensuring that the motor will not move during testing. Power is supplied to the

motor using a DC power supply with varying output voltage. The motor speed is adjusted by changing the voltage output on the DC power supply. Data is obtained by linking the digital force gauge with a spreadsheet program running on a near-by laptop computer. The data is graphed, and several basic calculations such as mean, median, and max, are performed. The following is a list of the components required to make a low-cost peel test:

- ◆ DC power supply
- ◆ DC high torque motor
- ◆ Timing pulleys and belt
- ◆ Electronic connection parts (quick disconnect wires/plug, three way switch)
- ◆ Digital force gauge with laptop patch cable and spreadsheet capability

Whether used as a means of comparison or quality control, peel testing is an effective method for determining the bond strength between the trace and the circuit board. The quantitative data that is obtained is useful when qualifying new or existing board vendors. One of the benefits of this test is that it is relatively inexpensive to perform in-house or at external laboratories. This modified pull-test makes the EMPF more capable of determining the quality of a PWB manufacturer by supplementing existing electronics manufacturing qualifying tests.



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Tech Tips... Failure Analysis 101 (continued from page 7)

Perform testing to validate the hypothesis

Experiments should have a control or reference sample that can be used to validate the experiments. Design the testing to answer any questions created by the hypothesis.

Perform testing to disprove the hypothesis

Many overlook this step in experimental design. Utilize experiments that prove or disprove the counterpoint of the hypothesis.

Become a reporter

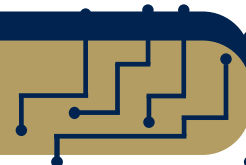
Once all the data is collected and determinations are made, communication is key. The use of written reports is the most effective method for relaying information. The reports should have data, images, graphs and bulleted conclusions that are easily explained with minimal wording. The pur-

pose of the reports are not only to communicate the cause of failure, but also to record failure mode, cause and corrective action for future users. This allows for prevention methods to be established that avert future failures.



Author of article: *Blaine Partee*- Blaine is a Materials Engineer at ACI. Comments or questions pertaining to this article can be sent to bpatee@aciusa.org.

Manufacturers' Corner... NuClean In-Line Aqueous Cleaner



In the past, “low residue - no clean” processing has played a dominant role in electronics manufacturing, and the cleanliness of final assemblies was no longer a critical issue in the manufacturing process. Recently, however, with the advent of ultra fast processing speeds, smaller components, denser assembly packaging and the use of more aggressive flux chemistries on alternate plating finishes, the cleanliness of final products is once again a dominant issue.

The ability to effectively and reliably clean under component packages can greatly affect the manufacturing yield by improving electrical contact during the test, preventing corrosion from residual flux contamination and also enhancing the appearance of the final assembly. Today, an ever increasing number of manufacturers are realizing the necessity of final product cleanliness and are seeking effective solutions to meet that need.

Traditionally, manufacturing companies have chosen to use a rosin mildly active (RMA) flux because of the solder reliability. The RMA flux is very aggressive and very forgiving in all processes while maintaining excellent solderability. While the RMA flux provides a good solder joint, it must also be completely removed to prevent deterioration of the circuitry. The flux requires chemistry or a cleaning agent to remove the contamination, as these fluxes are not soluble in water. In the past, manufacturers used vapor degreasers containing hazardous chemicals.

Today, flux contamination can be removed with EPA-approved, water-based chemistries. To date, many military based manufacturers still specify an RMA flux, as it is a proven technology with long-term reliability. In the late 1980's and early 1990's, the industry pushed to move towards Organically Activated (OA)/water-soluble fluxes. Although these fluxes are milder than RMA's, they are still aggressive, still corrosive, and still reliable, providing a quality solder joint. These fluxes also required the manufacturer to remove the flux contamination from the PCB, which could only be achieved using water (de-ionized (DI) preferred). Both water-soluble and RMA contamination can cause test and field failures. PCB manufacturers feel that if they clean either with water only or with water containing a water-based chemistry, they will produce a more stable product. No-clean fluxes are much milder than water soluble fluxes. This means that the parts to be soldered (boards and components) must be more solderable for a no-clean process than a water soluble process. If they are not, an increase in post-solder touch-up may be required. As a result of limitations in the solderability of no-clean fluxes, the window of the soldering process is greatly reduced. Many PCB manufacturers will clean even though they are running a no-clean process. The removal of solder balls and the removal of any remaining residue are two of the many reasons for the continued cleaning.

There are PCB manufacturers who originally switched to a no-clean process and have gone back to a water-soluble process. They have found that the unforeseen difficulties they encountered outweighed the originally forecasted savings of switching to the no-clean process. After cleaning, the PCB assembly will show significantly lower levels of ionic contamination as compared to PCB assemblies that are not cleaned. The EMPF uses a Technical Devices Company Aqueous Cleaner, Model 318 XL (Figure 5-1).



Figure 5-1

An Aqueous Cleaner involves several cleaning processes and considerations:

- 1) First, determine if a cleaning agent is necessary for your process. The mixture of cleaning agent to water is normally in the range of 3 to 30 percent. One way to determine if this percentage is correct is to use a refractometer.
- 2) The PCB is then pre-washed to help remove a majority of the contamination prior to entering into the wash chamber. An increased amount of physical space between the pre-wash and the wash will facilitate the removal of contamination in the wash chamber. The pre-wash is critical in a water-soluble application. OA fluxes contain organic elements (primarily sodium), which have a tendency to foam if not handled properly. The pre-wash runs at low pressure (30-40 PSI) and flows approximately 3-6 GPM of either tap water or water fed from a wash pump (cascading system). In an OA process, the majority of the flux is removed in this stage. After the water is applied to the PCB it should be directed to a waste water system or to a drain. It is extremely important to avoid recirculating this water in order to prevent excess foaming. Additionally, there must be enough physical space between the pre-wash and wash to prevent the organically filled water from “dragging” into the wash chamber. The high pressure recirculation of the wash pump will create a tremendous amount of foam, reducing the wash chamber's ability to properly remove the contamination, and could possibly damage the pump itself. A pre-wash in an RMA/chemical application is used to apply the “cleaning agent” to help loosen the soils, allow extra time to expose

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Manufacturers' Corner... NuClean In-Line Aqueous Cleaner (continued from page 9)

the contamination, and aid in the wash chamber's removal of the contamination. The pre-wash and wash tanks can and should be shared. Foaming is generally not an issue with these types of fluxes.

3) After the pre-wash, there is typically an isolation chamber (known as a dead zone). Some cleaning manufacturers consider this a part of the pre-wash chamber.

4) Next, there is the wash spray, which is traditionally a high pressure, high flow and heated chamber where all of the flux contamination should be removed. It generally contains 3-7 spray wands on the top and bottom, depending on the supplier. The longer the chamber and the more spray wands, the more exposure the PCB will have to the water. Most cleaning manufacturers recommend pressures and flows between 90-115 PSI at 50-80 GPM to effectively clean underneath fine pitch, BGA and micro BGAs. The correct combination of pressure, flow and length allows for faster throughput, and conveyor speed can be increased with an increase in flow. Also, increased pressure allows the spray to penetrate underneath tight clearance areas.

5) The isolation spray chamber's purpose is to "isolate" the wash water and the rinse water. Isolation spray is not necessary in a straight water system. If the wash water is carried over into the rinse water, recontamination may occur, thus lowering the cleanliness level. If the wash water contains a cleaning agent, it can redeposit the cleaning agent onto the PCB, causing other contamination. If the rinse and final rinse water are closely looped, they will almost instantaneously exhaust the DI and carbon resins. It should also be noted that air knives should be placed before and after the isolation spray.

6) The rinse spray is a process used to completely remove contamination. This step uses a cleaner level of water, as this water cascades into the wash chamber. In an RMA process, this step is used to remove the cleaning agent from the PCB. It generally applies nearly the same pressure and flow as in the wash chamber but may have less spray wands. The water from this chamber cascades into the wash chamber.

7) Final sprays, depending on belt size, flow DI water at 3-5 GPM and 30-60 PSI to remove any possible remaining contamination. DI water acts as a cleaning agent by attaching to both positively and negatively charged ions. If the ions are still present, the DI water absorbs them as it passes over the product. The DI final rinse also lowers the surface tension, helping the water to move more freely and aid in the drying process.

8) The next zone is the drying chamber. The complete removal of the water is critical, as even good quality DI water can leave water spots and create contamination. A completely dry board is important when going directly into

testing or conformal coating. Most cleaners use turbine style blowers with air knife technology that effectively removes all water. While some do offer infrared (IR) panels, it is not recommended in most applications. Using IR panels, the water is evaporated and often baked on, leaving water spots and possible contamination. Turbine blowers with air knife technology act as a squeegee to remove the water, leaving no water spots. The air is generally applied to the PCB at an elevated temperature (120-150°F) to help increase the "flashing" off of water.

The EMPF is currently using the Technical Devices Company's Model 318 XL for numerous pilot PCB production runs. This cleaner recently assisted the EMPF in resolving a customer issue concerning the process used to clean PCB assemblies with a water soluble flux. The customer was interested in determining the levels of contamination and the effect of cleaning the assembly on those levels. Six identical, populated PCB assemblies were provided for testing. Three PCB's were assigned to group one, and three were assigned to group two. Group one was only tested with an ion chromatograph. Group two was first cleaned in the 318 XL, then tested with the ion chromatograph. Fluoride and Chloride contamination levels decreased significantly after washing, and both levels were well below recommended guidelines for surface mount assemblies. After reviewing the test results, the customer initiated a process requirement for aqueous cleaning of their PCB assemblies. A second batch of more than 500 PCB assemblies were successfully cleaned and immediately placed into service.

If you would like to see a demonstration of the Technical Devices Aqueous Cleaner, please call Jeff Stong at 610-362-1200, extension 224.



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For details, please contact Jeff Stong, the Equipment Advisory Board Coordinator, at (610)362-1200, extension 224.

Characteristic Properties of Materials Used in Electronics Manufacturing

The Electronics Manufacturing Training Center course entitled “Characteristic Properties of Materials Used in Electronics Manufacturing” is an effective resource for obtaining the knowledge required to perform more comprehensive quality inspections. This is particularly essential for domestic businesses that design and perform quality inspections of their own products that have been manufactured off-shore. As the role of the manufacturing engineer evolves, the job of making informed decisions about materials selection, performance, and reliability becomes more critical.

Material properties and selection influence the cost, performance and reliability of the final product. This course deals exclusively with materials-related issues in electronics. The course relates material properties to product and process quality. The objective is to provide participants with the ability to make educated assessments of all of the materials used in their components and assemblies.

Participants in the class are first exposed to the definition of material properties. These material properties are then associated with the chemistry and physics that influence product yield, reliability, and quality. Throughout the class there are a number of hands-on laboratories and demonstrations to improve understanding of the topics, and relate them to current manufacturing situations such as the following:

- ◆ PCB board materials analysis
- ◆ Metallography of solders
- ◆ Polymer characterization and selection
- ◆ Halide content characterization of fluxes and circuit boards
- ◆ Wire bonding
- ◆ Oxide detection and quantification

A wide range of topics are covered including:

- ◆ Board finishes
- ◆ Viscosity
- ◆ Electrical properties
- ◆ Corrosion
- ◆ Diffusion
- ◆ Ceramic and composite substrates
- ◆ Fluxes
- ◆ Semiconductors
- ◆ Solder alloys
- ◆ Lead materials
- ◆ Plastic packaging
- ◆ Wire bonds
- ◆ Underfills and adhesives
- ◆ Solderability
- ◆ Contamination
- ◆ Advanced packaging materials

Participants divide their time between the state of the art class-rooms, analytical laboratories, and the manufacturing facility during the three day course. They work with analytical equipment such as optical and scanning electron microscopes. Production and demonstration materials are used to provide a comprehensive learning experience that applies to real manufacturing situations. Attendees are also encouraged to bring sample products from their companies to use as examples during the labs.

The curriculum is divided into three main sections as follows:

1) Selection

Material selection is one of the most common tasks for design engineering. The ability to interpret data sheets and assess the material’s impact on the performance of a product is crucial for reliable performance. For example, knowledge of how Young’s modulus affects the mechanical behavior of an underfill can reduce the cracking of flip chips and improve the overall reliability of the assemblies.

2) Behavior

The actual behavior of a material can be much different from the reported theoretical value. This course discusses the causes of the variables and teaches the participants how to troubleshoot property variation.

3) Testing

The testing of material properties is widely understood to be the key to obtaining data for a project, performing failure analysis, or understanding material interactions. Material testing also provides information on the quality of incoming and outgoing products. Inspection test equipment and techniques are demonstrated for a wide range of materials and assemblies during the class. This provides the participants with both knowledge of the common failure modes observed in electronics and the proper techniques for evaluating them.

Engineers, quality managers, technicians, and designers attend the course to gain an understanding of the fundamentals of material properties. Topics such as diffusion and intermetallic formation are extremely useful for solder selection and process control. Those converting to lead-free solder alloys appreciate the understanding of phase diagrams, grain coarsening, and solder microstructure. The fundamental understanding of surface tension, oxide formation and flux can improve solderability awareness and increase product yield. The course curriculum was developed to translate complicated concepts into useful knowledge to assist in product development and production support.



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EMLC Upcoming Course Schedule 2004

Skills

BGA Manufacturing, Inspection & Rework
November 29-30

Chip Scale Manufacturing
November 15-17

Electronics Manufacturing

Boot Camp A
October 4-8

Boot Camp B
October 11-15

Certifications

IPC J-STD-001 Instructor Certification
September 13-17
October 18-22

IPC-A-610 Instructor Certification
September 20-24
October 25-29

IPC Challenge
September 1
October 27
December 8

IPC/WHMA-A-620 Requirements and Acceptance for Cable and Wire Harness Assemblies (CIS)
November 15-17

IPC-7711 Certified IPC Specialist (CIS) SMT Rework
December 1-3

J-STD-001 Instructor Recertification
July 15-16
August 30-31
October 28-29
December 6-7

IPC-A-610 Instructor Recertification
September 2-3
October 25-26
December 9-10

IPC-7711/7721 Certified IPC Specialist (CIS) SMT Rework and Circuit Repair
October 4-8

IPC-7721 Certified IPC Specialist (CIS) Circuit Repair
November 18-19

IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCBs
September 7-10

IPC-7711 Certified IPC Specialist (CIS) Rework of Electronic Assemblies
August 30- September 3
December 6-10

Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing
November 1-2

Design for Manufacturability
August 30-31
December 6-7

Failure Analysis and Reliability Testing
November 29-December 1

Characteristic Properties of Materials
October 25-27

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org



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