empfasis

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The EMPF is a U.S. Navy-sponsored National Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

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ETO Building Blocks

Power electronics are being developed by the EMPF during its ongoing work for the Department of Energy's Sandia National Laboratories. The EMPF is developing manufacturing processes for a high power semiconductor switch Emitter Turn Off (ETO) project. This effort, and actual hardware prototype devices, will be valuable resources or "building blocks" for use during the early phases of the Regional Electrical Power Technology Integration Leveraging Enterprise (REPTILE) program.

The REPTILE program focuses on the test and integration of power electronic devices and subsystems that will benefit the advancement of Navy ship systems and the transfer of that technology to commercial and industrial applications. One of the attribute goals of the REPTILE program is the verification of high power electronic components for use in the next generation of Navy / DoD power and utility applications.

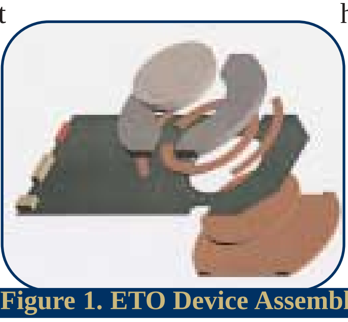

Figure 1. ETO Device Assembly

Another REPTILE program goal is the development and implementation of high power test capability at NAVSEA (Philadelphia). The ETO prototype building blocks will ensure the attainment of these goals.

The ETO assembly is a high power (Megawatt) semiconductor switch consisting of one large (120 mm dia.) Gate Turn Off (GTO) thyristor and a grouping of parallel Metal Oxide Semiconductor Field Effect Transistors (MOSFET). The GTO and MOSFET are mounted onto a single printed circuit board containing circuitry for the thyristor's gate control and interface. The advantages of this ETO device include improved performance in switching speeds, low conduction losses and "snubberless" operation all contained in a single economical assembly.

Technical Description of Tasks

Four of the numerous tasks to be accomplished by the EMPF during this development program include determining the reliability, calculating the internal power losses, and performing both thermal and mechanical finite element analysis of the entire ETO assembly.

Reliability Prediction

In order to determine the reliability prediction of an electronic device, such as this ETO assembly, the concepts espoused by MIL STD HDBK-217 F2 have been employed. This standard handbook contains two methods for determining the reliability prediction: "Parts Count" and "Part Stress Analysis."

The Parts Count method is applicable during the early design / prototype phase, and requires less information such as general part quantities, quality level, and the environment. It yields a more conservative (higher failure rate) estimate of the reliability prediction than the alternate method.

The Part Stress Analysis method requires a great deal more of exacting detailed information concerning each individual component used in the design. This includes stress levels of rated power, voltage, temperature, etc. This method requires tedious calculations to be made in order to determine the device’s reliability. Several software programs, currently under

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ETO Building Blocks
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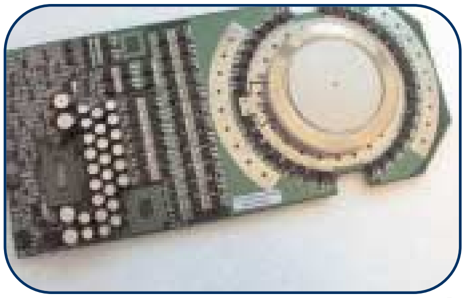

Figure 2. ETO Device

evaluation are now commercially available to assist in these calculations, and they also have the flexibility to rapidly recalculate the prediction for different environments, temperatures, and stress levels to demonstrate "what if" scenarios.

Using the "Parts Count" method, the reliability prediction of the prototype ETO device was calculated to exceed 47,000 hours for a Ground Fixed (GF) operating environment. This prediction is reduced to 4300 hours if the operating environment is changed to Naval Unsheltered (NU). These Mean Time Between Failure (MTBF) calculations will continue to be refined as the design of the ETO device is finalized.

Power Calculations

How much power is dissipated within the ETO assembly itself during its application is a critical factor in determining the performance specifications of the device. This power also determines the thermal requirements of the mechanical components and heat sink mounting design.

Table 1 lists the power dissipated in the ETO assembly for various levels of current through the device. Based upon the semiconductors specification sheets for determining the voltage drop across the parts, the GTO thyristor and the parallel grouping of power MOSFETs, will account for the power levels shown.

While these power levels appear large, consider that this device is capable of switching power up to 20mw loads, they really represent well under 1% of the switched power. The REPTILE program testing will confirm these power levels as well as the thermal performance of the devices.

I = 1000 amps	GTO power = 1.3 K watts	MOSFET power = 150 watts
I = 2000 amps	GTO power = 3.4 K watts	MOSFET power = 600 watts
I = 3000 amps	GTO power = 6.0 K watts	MOSFET power = 1.4 K watts
I = 4000 amps	GTO power = 9.0 K watts	MOSFET power = 2.4 K watts

Table 1: Power dissipated by ETO assembly

Thermal Analysis

To maintain the junction temperatures of the semiconductors (GTO and MOSFETs) below their maximum rated values (125° C and 175° C), it is necessary that the heat generated by the internal power dissipation be removed from the ETO device. This is accomplished by the effective design of the mounting plates and also the layout of the six layer printed circuit board (PCB) with a four ounce copper circuitry. This thick copper serves the dual purpose of allowing the circuit board to carry these large values of current while also lowering the thermal resistance of the PCB so that heat can flow efficiently through it.

Calculations of the thermal impedance of the complete ETO assembly result in a junction to case value of < 35° C/Kwatt for single side cooling, and < 13° C/ Kwatt for double side cooling. These numbers indicate that at a current load approaching 4000 amps, even with the double sided cooling heat sinks being water chilled with 5° C water, the junction temperature of the GTO will be approaching its maximum limit.

The high thermal conductivity of copper and aluminum made them the obvious material choices for the heat sinking plates. Parts will be made from both types of material for evaluation during the testing stages of REPTILE.

One section of the ETO assembly has the unique requirement that two of these adjacent metal plates must maintain good thermal contact, yet also be electrically isolated from each other. This problem was resolved in the design by using a thin (.002") substrate of Kapton material coated on each side with special thermal grease.

Mechanical Analysis

It is necessary to apply a high amount of contact mounting force (40 K newtons) on the anode and cathode connections of the ETO assembly. This ensures both maximum heat flow out to the heat sinks, and also guarantees a good electrical connection at these high current terminals. For this purpose, the surface finish is specified to be 15mm flatness and 1mm roughness.

The additional stress from thermal expansion on a stack of these press-pack ETO assemblies, during operation, must not exceed the limit where the GTO wafer is subjected to damage / cracking.

Other mechanical issues being resolved include the modular mounting of the high cost GTO semiconductor, alignment / attachment of the heat conducting plates onto the PCB, including the gate pin connection, and the design of a mounting frame and protective cover for the PCB components.

Summary of Benefits

In summary, the EMPF, in its partnership with Virginia Tech and Sandia National Laboratories, continues to build on its experience and expertise in the rapidly developing power electronics area through the ongoing work with the ETO project and its related interactions with the REPTILE program. The EMPF will continue to focus on transferring this new electronics manufacturing technology to its partners in industry, academia, and government.

For this specific project, the end result will be a better performing, high power electrical semiconductor switch becoming available for use in both military and commercial applications.

Manufacturing with Ball Grid Array Components

Continuous advancements in ball grid array (BGA) component packaging technology not only means that more component configurations are widely available, it also means that BGA components are becoming more prevalent in all forms of PCB assemblies. In this article we will examine several different BGA component package technologies and discuss the characteristic effects of these packages on the PCB assembly manufacturing processes.

The main BGA package configurations in use today are plastic BGA (PBGA), ceramic BGA (CBGA), tape BGA (TBGA) and metal BGA (MBGA). Of these, the most widely used are PBGA package configurations.

PBGAs are actually silicon die attached either through wire bonding or direct chip attachment to a glass epoxy substrate. The silicon die is then encapsulated with epoxy. Solder ball interconnections are added to the underside of the component substrate to provide I/O capability with the PCB assembly. Because these types of BGA components are built on a glass epoxy substrate, there are special considerations that must be accounted for during the manufacturing assembly process. These components in most cases have a limited time of exposure to the ambient environment and will absorb moisture from the air.

All BGAs are rated with a moisture sensitivity level, which dictates the allowable time of exposure to the ambient environment before special procedures must be employed, prior to assembly processing. These special procedures usually require the baking of the component for 24 hours at 125° C, in order to evaporate any moisture trapped within the component. If this is not done prior to sending the component through a high temperature reflow process, internal component delamination and fracturing (known as popcorning) can occur.

The interconnect balls on PBGA components are made of a eutectic alloy with a melting temperature of 183° C. This means that during the reflow portion of the assembly process, both the applied solder paste and the component balls will fully melt to form one integral solder connection. It is vital to ensure there is sufficient heat from the reflow process to ensure complete melting of all component balls. The center of a full array BGA will be the area of highest component thermal mass and the most difficult to reach maximum temperature. When developing a thermal profile for an assembly incorporating BGA components, it is advised to monitor the temperature directly under the center of the BGA component.

Similar to PBGA components, MBGA components incorporate eutectic solder connections for attachment of the component to the PCB assembly. The advantages of MBGA components are their thermal stability, increased flexibility and excellent heat dissipation. MBGAs by nature of their design, provide an excellent coefficient of thermal expansion (CTE) match between the component and the PCB substrate. This high CTE match translates into higher long-term reliability and less solder joint stress. However, be aware that the increased flexibility of MBGA components makes them more susceptible to deviations in coplanarity and increases the risk of assembly defects such as solder opens and solder shorts. Other considerations are the high moisture absorption rate and increased thermal mass of MBGAs as compared to PBGAs.

CBGA component interconnects are primarily made from high temperature alloys such as Sn10/Pb90 that has a melting temperature of 217° C. These high temperature component interconnects (either balls or columns) are attached to the component using a eutectic alloy or they are fused in place to the component substrate. During the reflow process, the thermal profile must be fine tuned sufficiently to ensure the eutectic alloy fully melts and attaches the BGA to the PCB, while also ensuring that the reflow temperature is not excessive enough to melt the high temperature interconnects of the BGA component.

The second type of BGA component that utilizes high temperature interconnections is the TBGA. As the name implies, these components incorporate the use of a low cost, low dielectric substrate, usually polyimide, as the component substrate. The use of this flexible substrate allows for absorption of stresses and strains during thermal cycling and provides a very good CTE match between the component and PCB substrate. TBGAs are more expensive and not as readily available as other component package types. However, be aware that the copper coverplate and internal copper stiffener give these components a higher thermal mass. This combined with the use of high temperature interconnections places tight restrictions on the reflow thermal profile.The main disadvantages to using TBGA components is their moisture sensitivity, usually level 4 and higher, and the availability of the components.

Knowing the type of component and its advantages and limitations will aid tremendously in assembly process development and provide greater end product acceptability yields. If you would like to explore these topics in greater detail, the EMPF offers a two-day course, "Ball Grid Array Processing, Rework and Inspection." Not only are these topics discussed in depth, the attendees have the opportunity to utilize the state of the art processing equipment available in the EMPF demonstration factory.

If you would like additional information on this topic or any other curriculum available at the EMPF, please contact the Helpline at 610-362-1320 or visit us online at www.empf.org.

J-STD-001 and IPC-A-610 Compared

IPC-A-610 or IPC/EIA JSTD-001C why two electronic assembly acceptance standard? What is Worker Proficiency Certification? How is the J-STD-001 Operator Proficiency Certification different? This article will answer these questions .

The IPC relies on industry volunteers, working in committees, to develop the standards. The committees are apportioned into eight major function categories. One of these, the Product Assurance Committee, has responsibility for the technical content of the IPC-A-610 standard through its IPC-A-610 Task Group.

The IPC-A-610 presents acceptance requirements for the manufacture of electronic assemblies. Essentially, the IPC-A-610 is a book of pictures and illustrations portraying acceptance criteria reflecting the requirements of other standards and specifications.

Historically, electronic assembly standards did contain more comprehensive and tutorial information relating principles and techniques. One consequence, the standardization of methods, resulted in conflicts because process methods changed faster than the standards.

The Assembly and Joining Process Committee, with the EIA Soldering Technology Committee, developed the joint standard, J-STD-001C: Requirements for Soldered Electrical and Electronic Assemblies. The IPC committee deals with automatic component placement, insertion, handling, attachment and joining techniques, as well as the cleaning operation prior to coating and encapsulation. The two documents will probably not be merged. The activities of the committees are different. We have the IPC-A-610C, a picture book that provides clarification and definition to the end item requirements that should result from the use of materials, processes and design (by extension) requirements described in the J-STD-001.

Board Type	Design Specification	Fabrication Specification
Generic Requirements	IPC-2221	IPC-6011
Rigid Printed Boards	IPC-2222	IPC-6012
Flexible Circuits	IPC-2223	IPC-6013
Rigid Flex Board	IPC-2223	IPC-6013

Table 3-1 Design and Fabrication Specification

Both the IPC-A-610 and J-STD-001 can be referenced on contracts to define end item acceptance. The IPC-A-610C preceded the J-STD-001 by a couple of years, therefore, the 610 was the more frequently referenced. However, the Department of Defense (DOD) adopted Handbook 001B and then J-STD-001C, consequently J-STD-001 is being referenced on many DOD High Reliability contracts. In practice, the requirements of the two standards are well harmonized, but there are significant differences.

Consider this excerpt from J-STD-001C Section 3 General Requirements: The soldering operations, equipment, and conditions described in this document are based on electrical / electronic circuits designed and fabricated in accordance with the specifications listed in table 3-1.

The table, courtesy of the IPC, references Design Standards and Fabrication Specifications. These govern many characteristics of the boards. Paragraph 3.1.2 states: “Mounting and soldering requirements for specialized processes and /or technologies not specified herein SHALL be performed in accordance with documented procedures which are available for review.”

Compare the above requirements with the following guidelines from the IPC-A-610C. Paragraph 1.2 (Purpose) states: “The visual standards in this document reflect the requirements of existing IPC and other applicable specifications. In order for the user to apply and use the content of this document, the assembly/product should comply with other existing IPC requirements, such as IPC-SM-782, IPC-2221, IPC-6011 and IPC-A-600. If the assembly does not comply with these or equivalent requirements, then the acceptance criteria needs to be defined between the customer and supplier.”

We see in the paragraphs above of a significant difference between the two standards. In the case of the J-STD, referenced standards extend the standard. In the case of the 610, referenced standards are provided for reference, unless specifically identified as an extension of the standard.

Quoting from J-STD-001C, “Section 5.2 Solderability: Electronic/mechanical components and wires to be soldered SHALL meet the requirements of J-STD-002 or equivalent, and printed boards SHALL meet the requirements of J-STD-003 or equivalent. When a pre-tinning

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Automated Optical Inspection

Automated Optical Inspection (AOI) uses the camera's eye to see the defects produced during the assembly process of printed circuit boards (PCBs). AOI's main focus in the manufacturing process is to monitor the processes during assembly. The process searches for defects that arise after printing, component placement, or reflow.

The PCB assembly of surface mount components, begins with the screen printing of the solder paste. Most of the problems that appear during this stage of the assembly are quickly identifiable. One problem could be the offset of the print onto the PCB. In some situations the inspection for this problem can be done manually but when there are fine pitch component pads and smaller PCBs, the problem can be easily missed. Using an AOI system at the end of the printing stage, helps detect these kinds of problems.

The AOI system can also determine the height of the paste printed on the pads to detect any discrepancy. An AOI system can help in the quality of the print that is demanded in a good assembly of a PCB. It can also record data that can be used for analysis of the performance of the printing machine. The result can be in calibration issues of the machine or consistency of the print.

The next step in the assembly line is the pick and place machine that places the components onto the PCB. Placement of components can be another area where problems arise. Problems such as absent parts from the PCBs and wrong polarities are some of the defects an AOI system can detect during this process. Although an operator programs the pick and place machine to do its job properly, the AOI system can be a secondary check to ensure the consistency of the machine and potentially improve the accuracy of the placement of components. Aside from the presence of the component and its polarity, the AOI system recognizes co-planarity tilted up or down of parts. Other recognition AOI can have is optical character recognition (OCR), size, color and orientation. Again, the AOI system generates data to analyze the performance of the pick and place machine.

Once the PCBs have the right components and they are placed the right way, the PCBs enters the reflow oven, where components are soldered. There will be times when the reflow process doesn't produce the quality demanded. Although defects can occur during any process step, defects occur more times during this stage of the assembly than any other part of the assembly line. Some defects are apparent, while others are not. In many cases, an AOI system is found at the end of the assembly line, where final inspection of the PCB is done. Some of the defects associated with the reflow stage are discrete component tombstoning or missing components.

An AOI system at this stage will help in identifying these defects more quickly and readily. As PCBs get smaller, the components used get smaller and spaced closer to accommodate the shrinking surface area of the PCB. In this case, the AOI system is ideal to have and use verses human inspection with a microscope.

AOI system courtesy of Gopel Electronics

An AOI system can be used to improve the process of assembling the PCBs. There are a number of different companies that make these systems and they all have their ways of inspecting. For the most part, the one area that distinguishes one machine from another is the vision system itself.

Most traditional AOI systems will take an image of a golden PCB and compare it to the PCBs that will be inspected. This technique is called template matching. However, problems can occur as a result of poor lighting. Often it is difficult in finding a golden PCB that will be an exact match, as most components vary in color, size and shape.

One of the better approaches to image comparison is the use of an adaptive AOI system that takes several images of components and compares them to the captured image of the component under inspection. This method is called Statistical Appearance Modeling (SAM). As mentioned in an article in the SMT Magazine on AOI systems, "SAM software builds a flexible, mathematical model of the object. As it examines more samples, the software successively refines its estimates of what the object should look like…. SAM is an empirical approach that demands no inherent understanding by the user or inspection system of what it is deciding.[1]"

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Automated Optical Inspection

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In summation, some of the benefits of an AOI system include:

- One operator to maintain the machine during the inspection
- Eliminates or minimizes the need for groups of employees to handle inspections of PCBs during or after the assembly
- Accuracy and repeatability is much improved
- Improved data acquisition which leads to better analysis of the processes in the assembly line
- May be used offline to do inspections

An AOI system can improve the assembly process and help monitor its progress. Along side in-circuit testers, AOI systems improve the production of good products. More and more manufactures are looking to have these systems implemented into their lines to reduce fallout. Quality control becomes easier to handle and maintain thus improving cost efficiency for production.

For more information on AOI systems, please contact the EMPF Helpline at (610) 362-1320.

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[1] Reis, Bob. “New Advances in AOI Technologies.” SMT Magazine. January 2001

J-STD-001 and IPC-A-610 Compared

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and inspection operation is performed as part of the documented assembly process, that operation may be used in lieu of solderability testing.” The IPC-A-610 is silent on the subject of solderability testing and dedicates one paragraph to "process control methods." These differences might go unnoticed, until something goes wrong in your customer supplier relationship.

Let's take a look a the training programs. The IPC-A-610C Worker Proficiency training will provide your company and employees with skills in discriminating acceptable conditions from defect conditions as defined by the IPC-A-610 Standard. The 610 training focuses on process results, defining what is acceptable and what is not at the end item. The operator level program requires about 24 hours of classroom instruction. Class A Instructor certification requires about 40 hours of classroom time. There is no hands-on skills component to the IPC-A-610 programs.

The IPC J-STD-001C Operator Proficiency training provides a modular approach to certification training. The J-STD program is a combination of lecture and hands on soldering skills training. There are five modules, with each module requiring about eight hours to complete. Module One is required, a prerequisite overview of the requirements of the standard. There is no hands-on component to module one. Proficiency is demonstrated through a closed book test. The remaining four modules all require operators to demonstrate proficiency in soldering skills, defect recognition and in understanding the process requirements of the standard. Class A Instructor Certification is not modular. Instructors must demonstrate soldering skills, defect recognition and pass a comprehensive test covering the requirements of all five modules.

The J-Standards modular approach to training can save money. We see this when a smaller company has a few workers with specialized skills that parallel the content of the existing modules. The 610 program is appropriate for companies with specialized inspectors. Frequently, we see this in companies doing final assembly only, or in large Original Equipment Manufacturers (OEMs) and contract manufacturers.

For more information on certification training call the EMPF Helpline at (610) 362-1320.

Electronics
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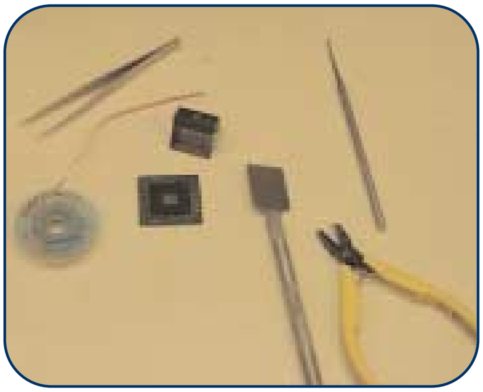
TECH TIPS...

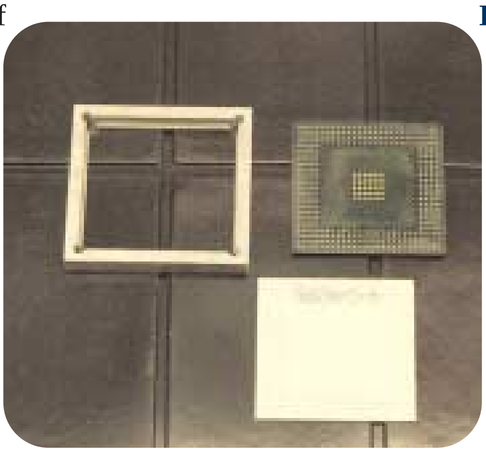
BGA Reballing

Ball Grid Array (BGA) packages are becoming more prevalent in their usage and the availability of the component cost has been decreasing for the more commonly used package configurations. It may not be a sound economic decision to reball a component that has a low initial cost. However, many custom ASIC and even some "off the shelf" BGA components, because of their complexity, are very expensive and have limited availability. For these types of components, it can be rather cost effective to have the ability to reuse components that may have failed on assemblies due to soldering defects. This article will discuss some considerations that must be addressed in order to successfully perform reballing of BGA components.


Typical material required for component substrate preparation

Package Specifications

Before attempting a reballing process, it is important to know the component package specifications. These specifications include maximum thermal limits for the component materials, alloy type (eutectic or high temperature), ball size, moisture sensitivity level and most importantly the manufacturer's recommendations for the maximum number of reflow cycles the component can withstand. This information can easily be obtained from the component data sheets or directly from the component manufacturer.


Solder preform material and fixture

Component Substrate Preparation

Prior to reattaching the new component interconnects, the component substrate must be carefully prepared by removing all remaining residual solder. The most efficient method of accomplishing this is to use solder braid and a wide blade soldering iron tip. The use of flux during this process will increase the effectiveness of the solder braid in wicking the residual solder from the component substrate. Care must be taken to avoid "scrubbing" the substrate surface with the solder braid and iron tip during this process, which can increase the chances of component substrate damage. Once all of the residual solder has been removed from the component substrate, it should be thoroughly cleaned using isopropanol alcohol (IPA) to remove any remaining flux residues. The component substrate should then be inspected for any evidence of component substrate damage.

Reballing Process Options For Eutectic Interconnects

Once the component has been properly prepared for attachment of new interconnects, either balls or columns, a process for accomplishing this task must be selected. The two main options available when reballing with eutectic balls is either the screen method or the preform method. The screen method requires specialized fixturing to place individual solder balls over the corresponding component substrate land pattern. Once all of the lands have a new ball in place, the entire fixture is sent through the reflow process to melt the solder balls onto the component. An alternate method is to use solder preforms in conjunction with a simple frame sized to match the outside dimensions of the component. This method has proven more efficient and reliable than the screen method. The solder ball preforms are available in literally thousands of package configurations and are very easy to use. The

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BGA Reballing

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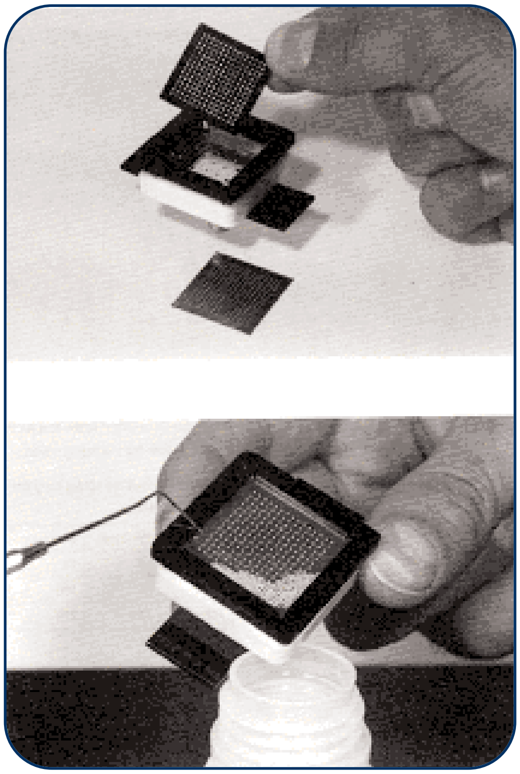
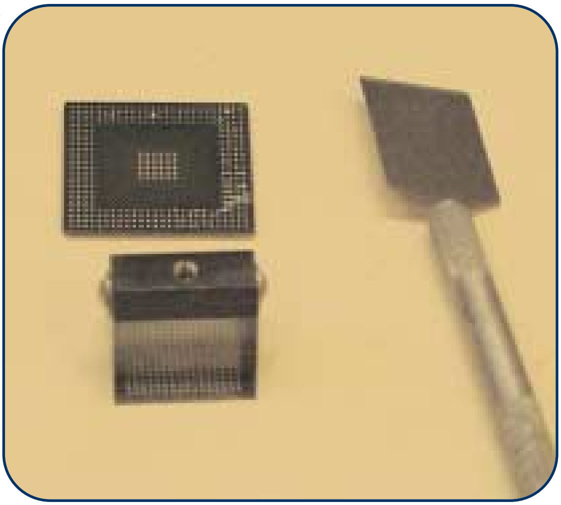
preform consists of precisely spaced balls sandwiched between a lamination of cardboard that has been impregnated with a water-soluble flux. Simply apply a water-soluble tacky flux to the component substrate, place the preform onto the component and then place the component into the frame. Reflow the component in the frame to melt the solder balls onto the component substrate. Once the solder preform balls have wetted to the component substrate and resolidified, the cardboard can simply be peeled away from the component and cleaned using DI water. This method, although more efficient, does require a bake out cycle of the reballed components for approximately 24-hours prior to placement of the components onto an assembly.



Solder reballing screen and fixture

Reballing Process Options For High Temperature Interconnects

When attaching high temperature interconnects to a component, the only viable option is to first screen solder paste onto the component substrate using a solder paste stencil and then placing the high temperature preform into the screened solder paste. The use of a split vision rework station helps in alignment of the preform to the component. The thermal profile requirements for reflow are also more critical when working with high temperature interconnects as opposed to eutectic. It is critical that the thermal profile be of sufficient heat to fully reflow the eutectic solder paste (without reflowing the high temperature interconnect) and remain within the maximum component temperature rating.



Solder paste stencil required for High Temperature attachment

Cleaning vs. Flux Chemistry

The cleaning process of the reballed component will depend upon the type of flux chemistry used during the reballing process. If using a no-clean or rosin based flux chemistry, isopropanol alcohol will do a very good job of removing flux residue. When using the solder preform method, which requires the use of water-soluble flux, cleaning in DI water is necessary. Because of possible water absorption by the component during the DI water cleaning process, it is necessary to perform an additional process step of a bake-out cycle of the component prior to use. The recommended bake-out for standard PBGA packages is 24 hours at 125°C. Other component configurations may have different recommendations, which can be obtained from the component data sheet.

When properly performed, the reuse of BGA components is possible and can be very cost effective. Understanding and adherence to the component and process specifications is critical to success and with experience, reballing and reuse of BGA components can be achieved rather easily.

The EMPF offers a two-day curriculum on BGA manufacturing, inspection and rework that discusses all aspects of BGA reballing methods. If you would like additional information please contact the EMPF Helpline at (610) 362-1320 or visit the EMPF website at www.empf.org.

Cut here and save!!

Manufacturer's Corner

DiagnoSYS Systems

PCB manufacturers face many challenges with today's changing technology. Contract manufacturers and captive assemblers are juggling the fine line of good yield, reliability and low volume production with reducing time to market for new products, and maintaining profitability in an extremely competitive market place.

One of the unifying issues tied to meeting these goals is the ability to test a circuit board once it has been assembled. Visual inspection and automatic optical inspection (AOI) (see page 5) provides some level of quality verification to ensure that components are properly placed and soldered. This stops short of actually verifying that the board functions to the required levels. The only thing that can accomplish this goal is a tester. However, there have been many challenges to overcome in testing today's densely populated, mixed technology PCBs. Challenges include fine pitch components in close proximity with other devices, faster time to get the product to market, and more complexity but lower budgets.


Flying Probe testing QFP

The transition from pin-through-hole (PTH) to surface mount technology (SMT) components pose some difficulty for testing both bare and populated circuit cards. What once was a simple bed of nails test on the bare board was made difficult by components and traces located only on the top of the board. In-circuit test (ICT) was often accomplished with power applied to the board. This could result in any number of failures including fried components and potentially scorched boards.

As board population density increased, the space between component leads and pads was shrinking. Actual lead dimensions were also shrinking, making it more difficult to reach. The solution presented by test equipment manufacturers at the time was very expensive, requiring significant investment in training and the purchase of custom fixtures for each board or a variable software license based on the number of test points required by a specific board.

In the end, board manufacturers were, and still are for some, faced with the challenge of validating product yield and reliability while maintaining an ever-shrinking profit margin.

The larger Contract Electronic Manufacturer (CEM) and captive houses have found a solution to their needs that is typically out of the price range for small and medium facilities. With the larger volumes and higher speeds, the answer is a flying probe tester that can perform traditional ICT with offline or inline systems.

ICT comes in various formats, the most popular method uses a fixture mounted on a base system, which detects component, board and process related faults. This technique is also known as manufacturing defect analysis (MDA). As board density increase and the node count increases, the use of fixtures becomes more expensive and oftentimes impractical. The result of these limitations was the development of the flying probe style of ICT.

For the uninitiated, the perception of flying probe systems is that they are more difficult to program than other forms of ICT. Fortunately for those 'in the know,' that's far from fact. Today's systems take advantage of Microsoft Windows interface technology to provide a recognizable front-end to the operator. Flying probe systems use the same 'fixture' (the probe tip) for many jobs. Space to store the tips is minimal due to their size.

The basic tenet of any tester is to improve quality by early detection of faults. Successful identification of a high percentage of potential failure modes is the key. Flying probe systems should be capable of capturing a majority of the most common faults typically experienced in your facility.

The EMPF is currently using a DiagnoSYS Auto Point II System on a CECOM communication module. The Auto Point II System provide the EMPF with a solution for every board test scenario including:
· Conveyor line high volume production test
· Pre-design testing
· Low volume, high product mix
· Detecting manufacturing defects
· Volume repair
· One-of-a-kind verification
· Non-destructive testing

The EMPF will use this equipment to compare board performance levels to the specified performance levels set by the military and their industrial-manufacturing partners. In addition, the EMPF is planning to use this system on the other projects such as MEMS assembly, and the REPTILE project.

Programming a dedicated test feature requires intimate knowledge of the circuit board and the fixture. You need to understand what each node of the fixture 'sees' to be able to program your test routine.

Flying probe systems can reduce that requirement by using an 'auto learn' feature imbedded within the software. The programming is now reduced to moving the camera, locating the probe tip on the desired point, and pressing the learn button on screen. Simply pressing the button starts a process whereby the

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Manufacturer’s Corner - DiagnoSYS Systems

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test system characterizes the node based on its library and stores the information not only for the target test routine, but also for future use. This technique allows your flying probe system to use each circuit node to its repertoire of library information.

Shrinking pitch on SMT devices has been steadily getting smaller. With each change in pitch come new difficulties for traditional test fixtures to reach the lead or pad without shorting adjacent pins. Flip chip and BGA only complicate matters since the interconnects cannot be reached directly. The probe tip solves this issue by reaching test points, such as via or traces, into tight spaces with a thin pin.

The simple act of reducing the need for a dedicated fixture allows faster turn around time for both programming and testing of new products. Any reduction in the complexity of the testing phase is welcome.

Removing the fixtures from the test equation has a trickle down effect. Without fixtures, modifications for circuit revisions are no longer required. Delays in production testing disappear since there are no fixtures to modify. Reducing the complexity of the testing set-up also reduces the maintenance requirements. Without costly fixtures, small spring loaded test pins, and large plugs being connected, removed, and re-connected, the overall wear and tear on the test system is reduced. Minimal routine maintenance on the probe mechanism and the probe tip is all that is required.

Flying probe systems help to increase profits by reducing the need for fixtures. Removing fixtures from the equation lowers your ongoing storage and maintenance costs. Easier programming techniques reduce the need for expensive, time consuming per job programming. It also reduces the training required to set-up and run the system for each board. The end result is that you can provide a better product for a more competitive price.

The most common method used by low cost probe systems is signature analysis. This is a non-destructive test technique used for manufacturing defect analysis (MDA) applications. Signature analysis is not only effective, but also extremely simple to work with, bringing technician level programming to ICT.

Signature analysis is performed by injecting a low level, current limited waveform into the node of a circuit. The waveform is distorted by the combination of elements that reside on the node, such as the resistance, capacitance, PN junction, etc. Once the node test is completed, a visual display of the waveform is shown onscreen as a lissajous figure. It is stored electronically, allowing the system to automatically compare the signature of the device under test (DUT) with previous results. Any variances will be seen as an altered waveform, with those outside a specified tolerance flagged as an error for repair or replacement.

There are many advantages to this technique. One of the most important benefits is that no power is applied to the DUT. This is extremely important since damage can occur when power is applied to a circuit with defective or incorrect components. In fact, this non-destructive technique prevents damage to the DUT and any other component within the circuit.

The technique tests the actual pin junctions of an active device as well as its relative values of inductance, resistance and capacitance. This allows the system to detect leakage and bonding problems at the device level. Shorts, opens, incorrect polarity and incorrect values are also detected.

Once the circuit has passed the initial test, it is safe to begin additional, enhanced optional tests via the probe using external instrumentation. Some of the additional tests include making voltage measurements, frequency tests, checking for correct signals and even injecting various waveforms at specific points in the circuit. Adding extra tests to the process assists you in tailoring each program to specific applications to ensure that maximum test coverage is provided. Keep in mind that additional tests will increase the programming time. Most of the additional tests can be performed using the probe by attaching other test equipment to an integrated general purpose interface buss (GPIB). Some of the entry level flying probe systems allows the integration with 3rd party boundary scan companies. Boundary scan sends test vectors to compliant digital IC's on the board and reports the results via a serial data link. It also provides interconnection testing, cluster testing and in-circuit programming of flash devices along with other tests to verify functional integrity. Combining test processes ensures an excellent form of test integrity and is capable of producing high yields for a very small investment.

Probe systems in conjunction with AOI can now provide additional improvements to quality and yield. When a testing system is integrated into the manufacturing process, it improves quality by ensuring the product is good. If manual testing is currently being used, switching to an automatic testing system will increase the number of units tested. Over the past few years, improvements in AOI equipment have lead to reliable systems that provide comprehensive coverage for visible faults. Locating faults earlier in the process with AOI can reduce the number and types of in-circuit tests required. The combination of AOI & ICT reduces scrap, waste and saves money.

Meeting today's quality, yield and business targets is an achievable goal. There is a way to make a real difference in the company's bottom line by including a real test component into the mix. The simple introduction of ICT technology can and does make that difference.

If you would like to have a demonstration on this machine, please call Jeff Stong at (610) 362-1200 x 224.

Ask the EMPF Helpline!

CUSTOMER ISSUE: The EMPF Helpline received a call from a measurement instrument manufacturer involving field failure returns of small circuit board controllers. Through electrical testing, they traced the problem to a plastic Small Outline Integrated Circuit (SOIC). The EMPF was tasked with confirming the failure and performing a Level 1 Integrated Circuit failure analysis.

The EMPF Helpline Recommendation

The EMPF investigated the cause of the IC failure using the following Level 1 methods:

- Electrical testing to verify the failure mode
- Decapsulation to selectively remove the exterior package for die observation
- Optical inspection of pins, die surface, wire bonds, and other surface features
- Scanning electron microscopy (SEM) analysis of the die surface, wire bonds, and other surface features

Figure 1. A device after decapsulation showing the die surface

Three failed assemblies and one "good" assembly were tested and analyzed. The identified failing SOIC's were removed from the assembly using a hand soldering iron due to their small size (14 lead device).

Electrical Testing

All devices were electrically tested for the supply current, Icc, with Vcc=5volts and Vout=2.5volts or Vout=float per the data sheet specification as a baseline for analysis. Curve tracer current-voltage pin to pin characteristics were also analyzed and compared to the "good" unit. Two devices showed current levels that were above specification. One device passed all electrical testing.

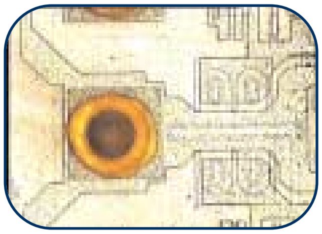

Figure 2. Optical microscopy showing die circuitry and metallization buss at approximately 200X

Decapsulation

To expose the surface of the die and wire bonds, the package mold compound was selectively removed. Small indentations in the package exterior just above the die were drilled with a rotary tool at low speed. Then, the device was placed on a hot plate set at approximately 100^{o}C. The encapsulation was then subjected to fuming nitric acid until the surface of the die was exposed. The device (figure 1) was then cleaned in an isopropyl alcohol bath.

Figure 3. Top down angled SEM image of a ball bond and Ground metallization circuitry

Optical Inspection

The die surfaces were inspected using a low-power stereo and high power incident light microscopes. External inspection of the failed devices did not reveal any anomalies. Inspection of the die surface after decapsulation did not reveal any obvious defects in the circuitry of the devices, with special attention paid to the Vcc and ground metallization busses. Figure 2 shows an example of a close-up of die circuitry and the ground buss metallization.

Scanning Electron Microscopy

SEM analysis was also used to examine the die in accordance with lab procedures. No abnormalities were detected on the die surface. Although the exposed ball bonds appear to have a flatter shape than normal, there were no failure mechanisms detected in any of the failed devices. The condition of the die exterior for the good device and the failed devices were identical. Figure 3 displays an example of a SEM image of the die surface.

Conclusion

Level 1 failure analysis of the failed devices was completed. The devices were verified to fail Icc, which would cause excess current flow and problems in board operation as seen by the customer. Shifted curve tracer I-V characteristics also show that these devices were most likely damaged electrically. One of the failed devices passed both Icc and curve tracer testing and is classified as an "unverified" failure.

No external damage to the package or the die surface was found during optical and SEM analysis. Therefore, absolute evidence of major Electrical Over-Stress (EOS) was not observed and no evidence of any other contamination, packaging, or wire bonding issues was found.

While electrical overstress is suspected in this case, the root cause failure mechanism of the device failures lies below the die surface. Further analysis would require removing the passivation layer with a plasma etcher and contacting the metallization using a probe station with micro-manipulators to electrically test and isolate the failure site with use of a laser cutter. The metallization, silicon dioxide and poly-silicon layers would be removed sequentially by plasma (dry) and/or chemical (wet) etch to expose damage and evidence of the layers affected. In addition, liquid crystal analysis can be used during these steps to look for a high current "hot spot" site to assist with rapid failure site location. These additional processes are referred to as a Level 2 IC failure analysis and the customer was informed that further analysis would require this level of detail, using additional equipment, techniques and time.

If you have an electronics manufacturing problem, call the EMPF Helpline at (610) 362-1320

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Electronics Manufacturing

Electronics Manufacturing BOOT CAMP A - Week 1
Sept. 16-20 Oct. 28-Nov. 1

Electronics Manufacturing BOOT CAMP B - Week 2
Sept. 23-27 Nov. 4-8

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SMT Soldering/Rework
Nov. 18-22

BGA Manufacturing, Inspection & Rework
Oct. 7-8

Advanced Packaging Techniques
Oct. 9-11

Certifications

IPC J-STD-001 Instructor Certification
Sept. 23-27 Oct. 14-18

J-STD-001 Instructor Recertification
Sept. 16-17 Nov. 4-5

IPC Challenge
Sept. 18 Nov. 6

IPC-A-610 Instructor Certification
Oct. 7-11

IPC-A-610 Instructor Recertification
Sept. 19-20 Nov. 7-8

IPC-7711/7721
Rework, Repair and Modification of Printed Boards and Electronic Assemblies
October 7-11, 14-17

Continuing Professional Advancement

Design for Manufacturability
Oct. 21-22

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For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

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