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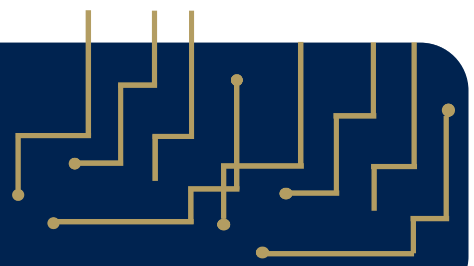

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American Competitiveness Institute
One International Plaza
Suite 600
Philadelphia, PA 19113
(610) 362-1200 • **FAX**: (610) 362-1290
HELPLINE: (610) 362-1320
WEBSITE: www.empf.org
www.aciusa.org

The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

EMPF Director
Michael D. Frederickson
mfrederickson@aciusa.org

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Office of Naval Research Manufacturing Technology Program

ONR Program Officer
Richard Henson
hensonr@onr.navy.mil

Link-16

The EMPF in a partnership with ONR, NAVAIR and Rockwell Collins, has undertaken the Link 16 PAI Affordability Program to develop a highly manufacturable Power Amplifier Interface (PAI) unit for the Link-16 Multifunctional Information Distribution System Low Volume Terminal (MIDS LVT1, Figure 1-3, Next Page) currently employed on E-2C, F/A-18 and F-16 platforms (Figure 1-1).

The purpose of this project is to re-layout and re-package the 200 Watt PAI portion of the terminal to reduce cost, size and position the equipment for inclusion in smaller size terminals. This will be accomplished through the use of industry state-of-the-art technologies in circuit boards, semiconductor packaging, MMIC devices, and heat-transfer and by incorporating new technologies, including Wide Band Gap (WBG) devices, that enable low/no tune strategies to enhance the producibility and significantly reduce the cost of the PAI.

The goals of this program include a 40% reduction in cost of the PAI for the LVT1, as well as to achieve a significant reduction (20% volume and 15% weight) of the physical size enabling the potential utilization in size limited applications such as missile systems, patrol boats, armored vehicles and rotary platforms. Additionally, all U. S. Government equipment programs will benefit from the semiconductor, packaging, and manufacturing technology being advanced and transferred across industry. Specifically, NAVY Communications, Electronic Warfare, and Radar programs desiring the use of WBG semiconductors will benefit by an earlier implementation of this technology.

The EMPF will promulgate industry standardization of modular and WBG packaging methods based on lessons learned during the execution of the program. This effort will include the evaluation of various methodologies to mitigate the thermal challenges that accompany WBG devices. This article will discuss the opportunities for redesign and a proposed new design concept.

In the conceptual redesign of the LVT1 PAI (Figure 1-2, Next Page), emphasis was placed on partitioning to modules that performed a specific electrical function that would be portable from location to location within this design and/or applicable to other designs. Additionally, electrical functions that could be tested or tuned and known assembly time and material cost drivers were also considered.

Figure 1-1: F-16, F/A-18 and E-2C aircraft equipped with Link-16

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NAVY MANTECH
manufacturing technology program

Link-16 (continued from page 1)

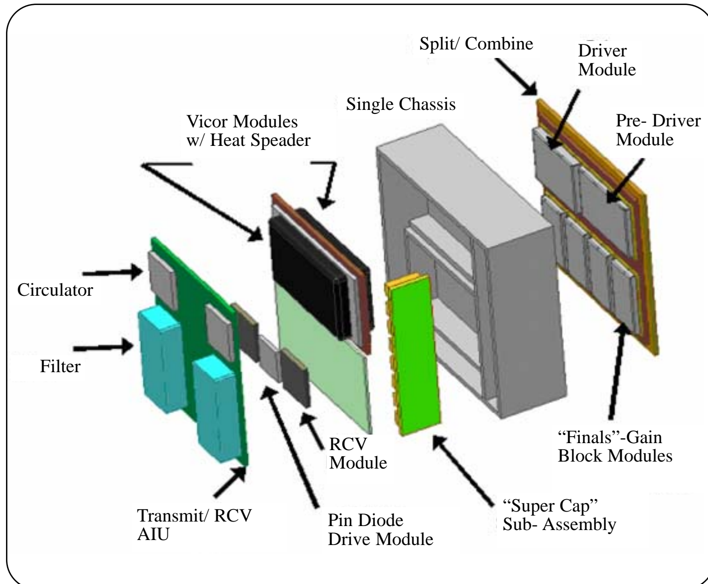

Figure 1-2: Redesigned PAI concept

The first proposal is to combine the Transmit and Receive functions into one printed wiring assembly, with interconnection between the two accomplished by using thru-holes or transitions within the PWB. Increasing the dielectric constant of the substrate would allow this AIU board size to be reduced relative to the existing design. The receive function would include two identical modules containing one low noise amplifier, two buffer amplifiers, bias circuitry, splitters and an output antenna select switch, all mounted to the backside of the new AIU board. The benefits of this redesign include reduced testing, a simplified chassis design, reduced assembly time and a simplification in terms of rework.

The control function of the PAI could be accomplished by creating multi chip modules (MCM) for each of the three main sub-functions of the current design. These MCMs would then be mounted in appropriate locations to take advantage of existing circuit board laminate structure. The control Power Amplifier function would be assigned to one MCM and combined with the main PA section of the PAI.

Figure 1-3: Link-16 Multifunctional Information Distribution System Low Volume Terminal

Similarly, a PIN diode driver MCM would be mounted on the AIU combined board. The remaining front end control MCM would be housed on a "mother board" that will interconnect the AIU, power supply, and PA sections. Within the power supply section of the LVT1 PAI, the use of a commercially available power supply module produced by VICOR® was a driving factor in the conceptual redesign. The use of two of these modules will provide the necessary power.

The important areas regarding the redesign of the PA section of the LVT1 PAI were:

♦Developing and implementing modules will help reduce overall material costs as modules may be used for other programs.
♦Modules may be tested and tunable at a lower assembly level and be easier to rework. Thermal management may be easier in a module.
♦Finally, consideration of alternative Power Amplifier technologies, such as LDMOS or Wide Band Gap materials can result in higher RF power, fewer output stages and fewer support components.

All modules would be housed in a single machined metal chassis, providing significant weight reduction.

Upon completion of this project, the U. S. Navy will have a new, miniaturized and affordable PAI, validated through independent testing by Rockwell Collins and the EMPF. The new PAI will be qualified for use in the currently fielded MIDS LVT1 terminals. Additionally, this PAI will be sized positioned for new smaller terminals which will better fit platforms that have less space available, such as missile systems, UCAV, patrol boats, armored vehicles, and rotary platforms.

Author of article: *Mark Nelson*- Mark is a Senior Manufacturing Engineer at ACI. Comments or questions pertaining to this article can be sent to mnelson@aciusa.org.

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Acceptability Criteria for Cable and Wire Harness Assemblies

IPC/WHMA-A-620, Requirements and Acceptance for Cable and Wire Harness Assemblies, describes the acceptability criteria for producing crimped, mechanically secured or soldered interconnections as well as the lacing and restraining criteria related to cable and harness assemblies. IPC/WHMA-A-620 was jointly developed by the IPC and WHMA (Wire Harness Manufacturer's Association) along with 86 additional user and supplier companies.

In addition to providing Industry with this new specification, IPC/WHMA has developed the Operator Proficiency Training Program to accompany the specification. The course is designed to enable operators to recognize the difference between an acceptable and unacceptable assembly. The ability to properly identify acceptable assemblies will help dramatically reduce the amount of rework required during manufacturing.

In an effort to meet and exceed customer and quality system requirements, electronics manufacturers are relying more on standardized training for their workforce. Assembly operators, technicians, and engineers are ideal candidates for this course. The knowledge they gain in just a few days can be immediately applied to many process issues related to cable and wire harness assemblies.

The Operator Proficiency course is designed modularly in order to accommodate the wide variety of cable and wire harness assemblies currently being used in industry. There are eighteen modules and manufacturers can select the ones they need to meet their needs.

Proficiency in understanding the specification is determined through a series of written standardized exams developed by the IPC/WHMA. Operators will be tested on each module in which they are trained. Operators who demonstrate proficiency will receive a portable certification in the areas where proficiency is demonstrated. Certifications are valid for 2 years. A brief description of each module follows.

Modules 1 and 2 (prerequisites for modules 3-18) covers the purpose and scope of the document, general criteria, and related applicable industry specifications. Students will learn how to properly interpret the acceptability requirements, understand the difference between the classes of electronics, and become familiar with commonly used terminology. Companies can select additional training to the various other cable and wire assembly acceptance requirements.

Module 3-Preparations: Covers the allowable amount of conductor strand damage, wire separation, and insulation damage.

Module 4-Solder Terminations: Covers the requirements for tinning and gold removal of wires, cleanliness, insulation, flexible sleeve insulation, wire separation, wire attachment and solder requirements for wires attached to commonly used terminals.

Module 5-Crimp Terminations: Covers the requirements and allowable deformation for stamped/formed contacts and machined crimp contacts.

Module 6-Insulation Displacement Connections (IDC): Covers the acceptance criteria for mass termination, flat cable and discreet wire terminations.

Module 7-Ultrasonic Welding: Covers the insulation clearance and weld nugget criteria.

Module 8-Splices: Covers soldered splices, crimped splices and ultrasonic welded splices.

Module 9-Connectorization: Covers acceptance criteria for hardware mounting, strain relief, sleeving, boots and allowable amount of connector damage.

continued on page 4

Acceptability Criteria for Cable and Wire Harness Assemblies (continued from page 3)

The EMPF Learning Center at the National Electronics Manufacturing Center of Excellence.

Module 10-Molding Potting: Covers the requirements for molding and potting of cables and wires.

Module 11-Cable Assembly and Wires: Covers the identification of reference designators and surfaces and how to properly measure wire lengths.

Module 12-Marking and Legibility: Covers the requirements for marking content, legibility, permanency, location, functionality, and marker sleeves.

Module 13-Coaxial and Twinaxial Assemblies: Covers the requirements for stripping, center conductor terminations, solder ferrule pins, coaxial connectors, terminal covers, shield terminations, center pin position, semi-rigid coax, swage-type connector, and soldering and stripping of biaxial or twin axial wires.

Module 14-Wire Bundle Securing: Covers the proper tie wrap and lacing application, requirements for wire breakouts, and wire bundles.

Module 15-Shielding: Covers the requirements for electrical shielding. Operators will learn requirements for braided shielding, shield termination, proper tape wrapping, conduit shielding, conductive coating, and shrink tubing.

Module 16-Cable and Wire Harness Protective Coverings: Covers protective coverings used for cable and wire harness assemblies. Subjects include braid, taping, sleeving and spiral plastic wrap.

Module 17-Installation: Covers the requirements for installation of hardware and wire harness installation. Operators will learn the proper assembly sequence for hardware and the stress relief required for wires.

Module 18-Solderless Wrap: Covers the acceptance requirements for solderless wrap connections. Topics include number of turns, turn spacing, end tails, insulation wrap, raised turns, connection position, wire dress, wire slack, plating and damage.

At the request of industry, the EMPF is now offering Operator Proficiency training to this latest industry consensus specification. Interested parties should call the EMLC Registrar for more information at (610) 362-1295 or send email to registrar@empf.org.

Author of article: *Tracy Clancy*- Tracy is an instructor at ACI. Comments or questions pertaining to this article can be sent to tclancy@aciusa.org.

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- IPC-A-610 *Instructor Certification*
- IPC-7711/7721 - *Rework, Repair and Modification of Printed Boards and Electronic Assemblies*
- IPC-WHMA-A-620 - *Requirements and Acceptance for Cable and Wire Harness Assemblies*

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Contact the EMPF Training Center to acquire additional information and schedules for any of the classes listed.

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Cut here and save!

Tech Tips...

NO-CLEAN PROCESS OPTIMIZATION

Typical "no-clean" fluxes differ from fluxes that are intended to be cleaned in two important ways. First, no-clean fluxes employ acids with lower activity levels. Secondly, they contain lower quantities of non-volatile solids. It is important to identify the characteristics of no-clean fluxes as follows:

♦The flux cannot reduce heavy oxides from boards or component termination.

♦The flux may not promote thermal transfer, through convection.

♦The flux residue may not inhibit formation of oxides at high temperatures.

♦The flux may not enhance surface tension of the solder, nor promote wetting of the metals to be connected. Low residue means reduced surfactant properties.

♦The flux residue may be more active when improperly processed. Many low solid flux formulas have very low viscosity. This can present problems in selective and hand soldering applications where the entire assembly may not see process temperatures required to properly render the flux.

No-clean fluxes result in wider variations in solder process results. Users of these materials must control other solder process variables to prevent problems with heat transfer during hand soldering, increases in solder balls, webs, bridging, and unexpected field failures from corrosion (Figure 2-1).

Figure 2-1: Image of a Dendrite

Process Recommendations

1. Components must be solderable at the start of the soldering process. Optimize handling and storage by verifying that boards and components satisfy the requirements of J-STD-002 and J-STD-003 before you put them in stock.

2. In addition to solderability, verify that boards and components are clean.

3. Flux performance can change from one component or board finish to another. Some fluxes seem to work better on nickel under gold compared to immersion tin. Others seem to work better with immersion silver and OSP (Organic Solder Preservative). Choose a flux that works well with Pb-Free finishes.

4. Increase soldering process control. Establish a time temperature profile for each assembly. Oxides form quickly at high temperature. If the flux is cooked off too early in the soldering process, new oxides may form at the connection site. Some fluxes form an electrically insulating varnish (polymerization) between the carrier and the activator. If complete polymerization takes place before reflow, formation of the solder connection may be inhibited. The machine settings should be established by a proven process. Validate solder process settings for preheat controls, conveyor controls, solder pot controls, machine recipes and inert atmosphere controls.

5. Train hand soldering and rework technicians. Sometimes the methods used with one formula will not work with another. The transfer of heat into the work piece is accomplished by means of radiation, convection, conduction, or a combination of the above. Excessive heat can cause the flux to be boiled away from the solder connection. This results in the loss of its contribution to the process. Technicians may need the following alternative approaches to be successful:

♦ Consider lower tip temperatures.

♦ Consider the benefits of hot air rework.

♦ Validate manual soldering and rework techniques.

♦ Establish rules for hand soldering and rework cosmetics that everyone can live with.

Author of Article: *Guy Ramsey*- Guy is a Master Instructor at ACI. Comments or questions pertaining to this article can be sent to gramsey@aciusa.org.

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SIR Testing

Shifting domestic/global economics and technological advancements have proven one thing as fact: Electronics manufacturing is about change. It is becoming unusual for an electronics manufacturer to produce the same product for the same customer while utilizing the same equipment, same processes and materials for an extended period of time. Surface insulation resistance (SIR) testing is a powerful tool electronics manufacturers can use when adapting to changes in processes, materials, and manufacturing equipment. It is commonly used to assess process and design changes, qualify new and existing materials, and compare like materials or processes. Once product performance and reliability have been established using SIR, testing results can be used as equally powerful marketing and quality assurance tools.

What is SIR testing?

In the electronics manufacturing industry, SIR testing is an extremely sensitive test method for evaluating the reliability of materials used for board assembly. SIR testing evaluates the propensity for assembly failure caused by shorts or current leakage between metal conductors. These failures can be induced by material interactions, inadequate process control, or poor material performance. SIR is an electrical test that measures a change in current over time and is typically performed at elevated temperatures and humidity levels.

Surface insulation resistance is defined as electrical resistance between two electrical conductors. Sheet resistance, bulk conductivity, and electrolytic contaminant leakage are all factors that affect the insulation resistance. For the electronics manufacturer or producer, surface insulation resistance can be thought of as a system's ability to resist surface shorting of leads or traces.

It is well known in the electronics manufacturing industry that the cleanliness of a printed wiring board (PWB) is crucial to the performance and reliability of an assembly. Monitoring and quantifying the degree of cleanliness is necessary in order to ensure that the final cleanliness of an assembly is acceptable. Performance of SIR test samples are directly related to cleanliness. It is the reason why bare PWB manufacturers, flux and conformal coating producers, and assemblers embrace SIR as a process and product development tool.

SIR test results can be used for a variety of purposes, including:

- ♦ Classifying fluxes
- ♦ Qualifying fluxes and pastes
- ♦ Improving a cleaning process
- ♦ Qualifying and comparing conformal coatings
- ♦ Comparing cleaning materials
- ♦ Comparing flux materials
- ♦ Qualifying bare-board cleanliness

Contamination

Contamination can severely diminish the ability to resist shorting of leads or traces. There are specific types of contamination that are indigenous to the electronics manufacturing process prior to or after product assembly. Harmful residues and contaminants are separated into two main categories- ionic and non-ionic.

Ionic residues can be described as residue that contains molecules or atoms that are conductive when in solution. Some of the most common sources of ionic residue include:

- ♦ Plating chemistries
- ♦ Flux activators
- ♦ Perspiration
- ♦ Ionic surfactants

Non-ionic residues are not conductive and are usually organic species that can remain on the PWB after board fabrication or assembly. These include:

- ♦ Rosin
- ♦ Oils
- ♦ Greases
- ♦ Hand lotion
- ♦ Silicone

While both ionic and non-ionic contamination can impact the operation and reliability of the device on which they are present, the effects of ionic contamination are of greater interest to the most PWB manufacturers. A higher number of failures are associated with ionic contamination than its non-ionic counterpart.

Electrochemical migration

Electrochemical migration is an occurrence of a conductive metal bridge forming between conductors when they are subjected to a DC voltage bias. Metal conductors, like lead from a tin-lead HASL coating, grow from a positively charged conductor (cathode) to a negatively charged adjacent conductor (anode) creating a short circuit between the conductors. The growth takes the tree-like form of a dendrite as seen in Figure 3-1.

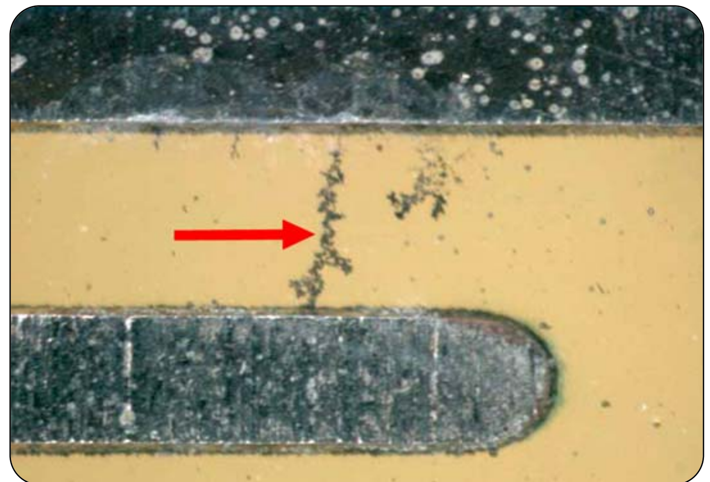


Figure 3-1: Dendrite growth between positively and negatively biased conductors (top and bottom).

continued on page 7

The added presence of moisture can cause ionic residues to disassociate into either negatively or positively charged species and create conductive solutions, known as electrolytic solutions. When there is a voltage bias between a cathode and anode, an ionic species will grow from one conductor to another. Chloride and bromide, commonly found in fluxes and PWB substrates, are two of the most common dendrite forming substances. Metallic salts from copper based metals, which conduct electricity and create shorts across the leads or traces, can also be formed in the process.

Electrochemical corrosion
Chloride and other halides commonly found in fluxes often form acidic solutions that attack the metal surface. Simply put, the higher the concentration of the halides, the stronger the acidity of the solution. The acidic electrolyte solution corrodes metallic conductors such as copper and tin-lead traces and leads. Voltage bias will severely accelerate the corrosive process and free-up metallic ions. Once in the solution, the metallic ions either form dendrites or form conductive salts like copper chloride or copper sulfates. Dendrites and conductive salts both have the effect of lowering the insulation resistance and ultimately result in short circuits or current leakage.

It is the function of conformal coatings to protect a board or assembly from harsh environments. In water condensing environments, conformal coatings are expected to prevent moisture from interacting with any process residues thus preventing dendrite or conductive salt formation. Permeability is one key factor that determines how well a coating performs. Despite having excellent permeability characteristics no conformal coating can proscribe water indefinitely.

The mechanics of SIR testing
SIR test samples utilize specific patterns similar to those shown in Figure 3-2 to assess insulation resistance. The growth of dendrites or the presence of conductive solutions between the conductors of the patterns affects the resistance between them. Higher SIR values are the result of cleaner boards that do not form dendrites. Lower values are a result of the presence of conductive dendrites or salts. A preferred method of testing involves the use of specialized SIR measuring equipment that applies voltage and records DC resistance at programmed intervals. Increasing temperature and humidity can have the effect of accelerating dendrite growth and artificially age the samples to simulate the service life of a product. Having precisely controlled temperature/humidity chambers and SIR measuring equipment are the most reliable and efficient ways of performing an accurate SIR test.

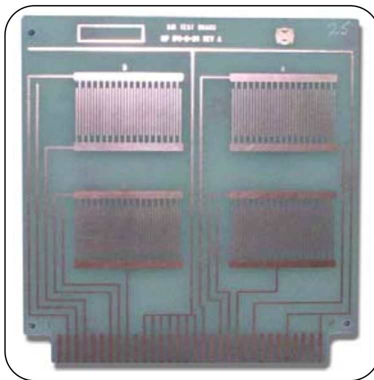


Figure 3-2: IPC comb test pattern

Standards and Test Vehicles
There are several industry standards developed by the IPC, Bellcore, and Japanese Industrial Standards used to classify fluxes, residues, and conformal coatings. The standards used, test conditions, and layout of the SIR pattern are dependent upon the materials to be tested. There are industry accepted test patterns that can be ordered through the IPC or Bellcore as Gerber file data. Many bare board manufacturers will be familiar with SIR test pattern Gerber data thus reducing the cost of producing test samples. Table 1-1 shows some of the typical uses for many of the popular test patterns. One of the most common tests is conducted using IPC TM-650-2.6.3.3. This test is intended to characterize fluxes using a standard comb pattern at 85% relative humidity and 85ºC.

Description	Materials tested	Note
IPC-B-24	*Liquid flux, solder paste, conformal coatings*	*Easily used for wave soldering*
IPC-B-36	*Fluxes, pastes, cleaning materials, cleaning processes, conformal coatings*	*Good for assessing process capability*
IPC-B-25	*Solder masks, and conformal coatings*	
IPC-B-25A	*Solder masks*	
Bellcore Test Pattern	*Fluxes, pastes, cleaning materials, cleaning processes, conformal coatings*	
Low Residue Soldering Task Force Test Vehicle	*Fluxes, paste*	*Provides test data for high reliability no-clean applications*

Table 1-1: Most common SIR test patterns

Is SIR testing right for you?
If you plan to make changes to your manufacturing processes then SIR testing should be seriously considered, particularly if you intend to do any of the following:

- ♦Alter board design or layout
- ♦Change cleaning materials or processes
- ♦Change fluxes and/or pastes
- ♦Perform radical changes in reflow or wave profile
- ♦Use new conformal coating materials or processes
- ♦Qualify bare board suppliers
- ♦Market a product based on reliability

At the EMPF, SIR testing is relied on to improve the reliability of electronic components used in commercial and military applications, and to enhance the overall productivity of electronics manufacturers.

Author of Article: *Blaine Partee-* Blaine is an Engineer at ACI. Comments or questions pertaining to this article can be sent to bpartee@aciusa.org.

Wide Band Gap - Thermal Considerations

Future high power applications will demand that power devices possess high blocking voltages, switching frequencies, increased efficiency, and extended reliability. Silicon technology however is approaching its theoretical limits. Silicon carbide (SiC), as one of the most mature wide band gap (WBG) semiconductors, is a natural choice for high power applications based on its notable material properties. Because of its larger band gap, around 3 eV compared to Si (Silicon) at 1.1 eV, the leakage currents in SiC are much lower than in Si. The high intrinsic temperature (above 800°C) of SiC offers excellent thermal stability. The high breakdown field of SiC and saturated electron velocity are key properties that make SiC ideal for high power operations.

SiC devices have the benefit of high blocking voltages in the diodes and transistors that could help to avoid serial stacking and associated packaging difficulties at higher voltage levels. One of the possible benefits of a higher switching frequency in pulse-width-modulated rectifiers and inverters would be a substantial reduction in the areas occupied by passive circuit components, as well as reductions in the complexity of the circuits. Currently, SiC, IGBTs (Insulated Gate Bi-Polar Transistors), GTOs (Gate Turn-Off Thyristors), MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), Schoktty diodes, and JFETs (Junction Field Effect Transistors) are commercially available examples.

Packaging is a high priority when attempting to optimize the performance of SiC die for high temperature operations. Aspects of SiC devices such as high power density, increased junction temperature and high frequency create considerable challenges for packaging and thermal management. A validated packaging technology for temperatures above 250°C is currently not available commercially.

When packaging and implementing SiC devices in high power electronic systems, proper thermal management is critical. When thermal and package designs are implemented correctly, the component life can be extended well beyond specifications. Removal of waste heat from any given operating component is essential to the effort of establishing long-term reliability for a given device, and also for other components in close proximity on the same print circuit board. If not dealt with, excess heat can cause catastrophic failures of semiconductor junctions and passive components.

Today's advanced packaging technologies like stacked die chips, multi-chip modules, and system-on-a-chip require that thermal management systems be designed to handle maximum power dissipation, power density, and power hot spots at both semiconductor and module levels. The ultimate goal is to produce a minimal temperature differential between the component surface and the heat spreader surface and further dissipate the heat out of the system.

Material	CTE (ppm/K)	Thermal Conductivity (W/m.K)
Silicon (Si)	2.6	130
Gallium Arsenide (GaAs)	5.7	55
Silicon Carbide (SiC)	5.1	700
Gallium Nitride (GaN)	5.4	110
Aluminum (AlN) substrate	4.5	200
Aluminum (AlSiC) substrate	6.5	30
w/ Copper (Cu) (85/15) metal matrix composites	6.5	170
Beryllium Oxide (BeO) substrate	6.1	280
Copper (Cu) baseplate	17	400
Tungsten (W)	4.6	188
Molybdenum (Mo)	4.9	140
Aluminum (Al)	23	235
Lead (Pb)	29	35
95/5 high temp Pb/Sn solder	29	35
Eutectic Pb/Sn solder	25	50
Tin (Sn)	23	66
Thermal Grease	N/A	0.75

Table 2-1: Various Semiconductor and Package Material Parameters at 300K

Packaging materials, reliable interconnection approaches and cooling techniques need to be further modeled and evaluated. Information gained from packaging Si and GaAs (Gallium Arsenide) semiconductors has shown that the coefficient of thermal expansion (CTE) and thermal conductivity of materials are critical when the package is designed and processed. Some packaging and semiconductor materials' CTE and thermal conductivity parameters are listed in Table 2-1. A close CTE match between the die and substrate, close CTE match between the device and the circuit board, lower thermal resistance at each heat transfer stage and a high heat dissipation rate from the junction to the ambient environment are some of the important characteristics that contribute to the high reliability of more ideal systems.

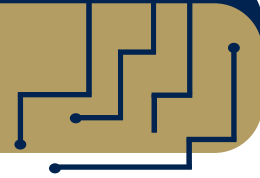
The influences of many packaging materials on the overall thermal resistance of Si and GaAs devices have been evaluated extensively by the EMPF. Taking advantage of these results by incorporating suitable packaging techniques for WBG technology will not only speed up the package development but also make the WBG technology more affordable for commercial and military applications.

References:

1) J. Hudgins, et al "An assessment of wide band gap semiconductors for power devices". IEEE transactions on power electronics. May 2003

Author of article: *Charlene Yao*- Charlene is an engineer at ACI. Comments or questions pertaining to this article can be sent to cyao@aciusa.org.

Manufacturers' Corner... Beamworks Process



In today's mixed assembly board, surface mount components represent the majority of all components. However, it is rare to see the complete absence of through-hole components in most assemblies.

In some cases, selective soldering can be avoided by using the paste-in-hole process for through-hole components. The paste-in-hole process is not always feasible when the component is temperature sensitive, has too many rows of pins to allow sufficient solder paste deposition, or the board is not designed for paste-in-hole process (e.g., other components may be too close).

Whenever the board's secondary side contains devices that cannot go through a wave solder machine, the through-hole components can be selectively soldered without impacting the adjacent components already soldered in the reflow oven. Examples of components on the bottom side that cannot go through the wave soldering process are any components that have solder spheres on the package bottom (PBGA, BGA and CSP).

Figure 4-1: Selective Soldering System
The BeamWorks Spark 100

This makes a strong case for the co-existence of through-hole and surface mount packages on the same board (mixed assembly). Continued use of through-hole components like sockets and connectors along with fine-pitch and BGAs means there are no options but to use selective soldering for the foreseeable future. The following are some commonly used selective soldering options, along with some that are not used currently but may be popular in the near future.

1. The most common method to selectively solder through-hole components in a mixed assembly board utilizes non-metallic fixtures. Board design is critical to reduce the number of iterations needed to come up with the final fixture that will only expose the through-hole components and completely hide the surface mount components on the bottom side. This option can be very expensive. Also, it is easy to run out of storage space for fixtures because about half a dozen fixtures are typically needed for each product.

2. Another method, generally referred to as solder fountains, uses a metallic fixture that covers the solder pot. The solder comes out like a fountain at the designated locations under the through-hole leads. These fixtures also can be very expensive and take more than a month to design and fabricate. The soldering defect levels can be high because the solder fountains change the wave's flow dynamics.

3. Another method, generally known as site-specific soldering, where a robotic carrier moves the board to the solder fountain, is becoming common. A variation of this method is a "dancing" wave, in which the board remains stationary but the solder fountain travels to protruding leads. The solder fountain solders each lead or row of leads at a time. Site specific soldering machines have built in fluxers, preheat and solder fountains and tend to simulate the standard wave soldering process. Such machines are flexible and do not use fixtures but can be expensive.

4. Another method uses intense focused light to heat the leads and provides solder by wire feeders. The key disadvantage of this process is that allowance must be made at the board design stage to keep solder mask away from the pads. Otherwise the solder mask close to the through-hole pads tends to burn or discolor. Additionally, such machines are flexible and do not use fixtures but can be expensive.

5.An increasingly popular method for selective soldering is a laser that also uses wire feeders. A built in IR sensor(s) in some of the commercially available systems use high powered diode lasers and can turn off the soldering when the joint achieves the desired solder temperature and volume. Some of these systems also can use the paste-in-hole process eliminating the need for wire feeders. These

continued on page 10

Beamworks Process (continued from page 9)

machines use fiducials for alignment and CAD data for locating the leads and therefore do not need fixtures. The laser can be focused from the top or bottom. Eliminating the need to flip the board before soldering is one advantage of using the laser and wire feed from the bottom. Another advantage is lasers are environmentally more desirable because they do not require hot metal pots. Additionally, laser systems can be less expensive than most other selective soldering options. The disadvantages of laser systems are 1) the processes may be slower and 2) diode laser soldering is a new technology and not everyone feels comfortable being on the leading edge.

To select the right solution for your application, examine your product volume, mix, complexity and capital budget.

The BeamWorks Spark 100, a Selective Soldering system designed for the SMT assembly industry, is used at the EMPF. The system utilizes a power controlled diode laser with a closed loop temperature and volume control for the soldering of the through-hole components. If you would like to see a demonstration of this system, please contact Jeff Stong at 610-362-1200 Extension 224.

Author of article: *Jeff Stong*- Jeff is the Equipment Advisory Board coordinator at ACI. Comments or questions pertaining to this article can be sent to jstong@aciusa.org.

Equipment Partners of the EMPF
To see some of the equipment in use at the
National Electronics Manufacturing Center of Excellence,
please visit our partners webpage at:
http://www.empf.org/html/partners/

Lead Free Manufacturing Training

Overview:
Lead-Free Manufacturing is a new initiative to eliminate lead from the electronic assembly process. Pending legislation as well as commercial market pressure from Asia and Europe, is forcing electronic manufacturers to consider new processing materials and techniques to meet this challenge. The EMPF, as the National Center of Excellence in Electronics Manufacturing, has developed a program that provides a combination of lecture and hands-on factory experience, all housed in the same facility. The objective is to introduce participants to the technical challenges of developing and implementing Lead-Free Soldering in a production environment.

Course Content:

- **Legislative Status:**
  Europe
  Asia/Japan
  United States
- **State of the Market Concerns:**
  Commercial vs. Military/Aerospace Market
- **Materials Issues:**
  Solder Alloys Available
  Board Finishes Available
  Component Finishes Available
- **Manufacturing Processes:**
  Screen Printing/Component Placement
  Reflow & Wave Soldering
  Hand Soldering/Rework & Repair
- **Reliability Topics:**
  Components
  Boards
  Solder Joints
  Microsectioning
  Failure Analysis
- **Additional Considerations:**
  Environmental Issues
  Configuration Management
  Program Sustainment

Courses scheduled for 2004: March 8th – 9th, September 13th – 14th

Contact the EMPF Training Center for additional information and registration:
Registrar: (610)362-1295 or email at: Registrar@empf.org

Ask the EMPF Helpline!

Customer Issue: The EMPF Helpline received a call from an EMS (Electronic Manufacturing Services) provider who had experienced delamination of the gold surface finish from the nickel under layer ENIG (Electroless Nickel - Immersion Gold) finished Printed Wiring Boards (PWB). The boards were from (and limited to) two PWB fabricator date codes. The PWBs had been solder assembled with surface mounted components and this delamination represented "open" failures of the finished Printed Wiring Assemblies (PWAs) during burn-in of the assemblies. The customer wanted to know whether these delaminations of the gold from the nickel could be repaired on currently failed product or avoided in the future.

Three samples were provided for investigation. Each sample was examined visually using low magnification. One of the samples was cross-sectioned in accordance with IPC-TM-650- 2.2.1D and examined using optical microscopy, Scanning Electron Microscopy (SEM) and EDS (Energy Dispersive Spectroscopy, also known as EDAX)

When an ENIG surface finished PWB undergoes soldering, the solder must adhere to the underlying electroless nickel plate. This is because the immersion gold is so thin that all of the gold dissolves into the solder upon soldering. The solder bonds directly to the electroless nickel.

If that nickel surface is contaminated in some way, the resulting joint will be weak and the locus of failure will be just below the surface of the nickel, leaving both nickel and phosphorous (a normal constituent of electroless nickel) on both the pad and the failed solder joint surface.

The EDAX analysis of the failed solder joint showed the presence of nickel at both the fracture surface of the solder joint and the pad from which the solder joint had lifted (see Figures 4-1 and 4-2) This is a positive indication that contaminated nickel was the cause of the failure.

"Black Pad" is a defect of ENIG boards that is a separation of solder joints formed to the surface of the electroless nickel underplate. This is commonly attributed to excessive phosphorous in the electroless nickel (i.e. nickel electroless bath out of control). However, any kind of nickel contamination (phosphorous or not) that results in the failures characterized here, are often reported as "black pad" failures.

The presence of 7.2% phosphorous in the nickel on the pad-side (see Figure 4-1) shows the normal concentration of phosphorous in the electroless nickel deposit, and proves this is not a classic "black pad" defect in which the electroless nickel would show an excessive amount of phosphorous. However, the presence of nickel and normal levels of phosphorous on both pad-side (Figure 4-1) and the lead-side (Figure 4-2) indicates that this "black pad" failure was caused by a mechanism other than excessive phosphorous in the electroless nickel bath

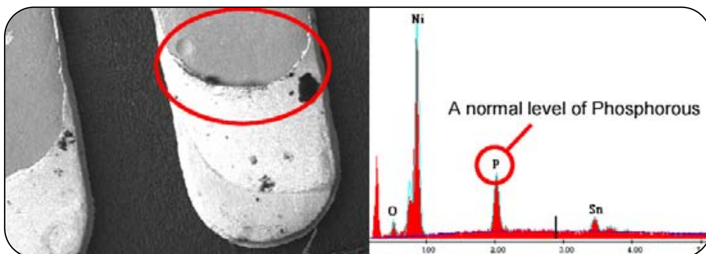


Figure 4-1: SEM and EDAX scan of pad-side of solder failure

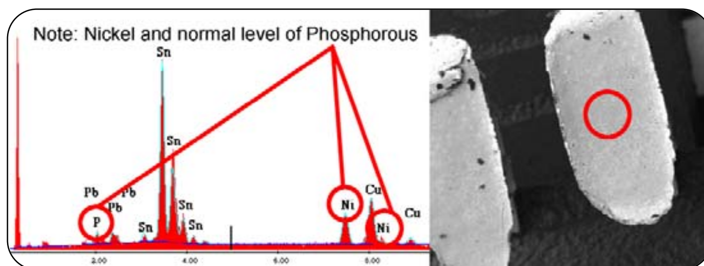


Figure 4-2: SEM and EDAX scan of lead-side of solder failure

Results:
From the initial x-ray analysis, it was determined that the workmanship and solder joint quality of the assembly were within good commercial practice limits.

The optical, SEM, and EDAX analyses showed that the solder joints appeared normal, but the opens were conclusively caused by the delamination of the gold from the underlying nickel layer on the ENIG. EDAX revealed normal electroless nickel phosphorous content, and a locus of failure inside the nickel.

The customer was completely satisfied with this result and the fact that the failures were shown to be related to the board manufacture and not the assembly operation.

Recommendation:
It was recommended that PWBs used by the customer be acquired from a more reliable source of ENIG finished boards.

Satisfied with these results and recommendation, the customer elected to change PWB vendors to one that has a history of more robust nickel gold finishes.

If you have questions about this article or any of the topics, please contact the EMPF Helpline at (610) 362-1320. A manufacturing expert will be able to offer technical insight and appropriate advice regarding your concerns.

Author of article: *Fred Verdi*- Fred is an engineer at ACI. Comments or questions pertaining to this article can be sent to fverdi@aciusa.org.

EMLC Upcoming Course Schedule 2004

Skills

SMT Manufacturing
February 23-27
May 24-28
August 23-27

BGA Manufacturing, Inspection & Rework
January 26-27
April 12-13
July 19-20
November 29-30

Chip Scale Manufacturing
January 21-23
June 21-23
November 15-17

Electronics Manufacturing

Boot Camp A
February 2-6
May 10-14
July 26-30
October 4-8

Boot Camp B
February 9-13
May 17-21
August 2-6
October 11-15

Certifications

IPC J-STD-001 Instructor Certification
January 5-9
March 1-5
April 19-23
June 7-11
August 9-13
September 13-17
October 18-22

IPC-A-610 Instructor Certification
January 12-16
March 8-12
April 26-30
June 14-18
August 16-20
September 20-24
October 25-29

IPC Challenge
January 28
March 24
May 5
September 1
December 8

NEW ***IPC/WHMA-A-620 Requirements and Acceptance for Cable and Wire Harness Assemblies (Operator)***
January 21-23
June 21-23
November 15-17

NEW ***IPC-7711 Certified IPC Specialist (CIS) SMT Rework***
April 14-16
June 21-23
December 1-3

J-STD-001 Instructor Recertification
January 26-27
March 22-23
May 3-4
August 30-31
December 6-7

IPC-A-610 Instructor Recertification
January 29-30
March 25-26
May 6-7
September 2-3
December 9-10

NEW ***IPC-7711/7721 Certified IPC Specialist (CIS) SMT Rework and Circuit Repair***
March 15-19
July 12-16
October 4-8

NEW ***IPC-7721 Certified IPC Specialist (CIS) Circuit Repair***
April 1-2
June 24-25
November 18-19

NEW ***IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCBs***
June 28- July1
September 7-10

NEW ***IPC-7711 Certified IPC Specialist (CIS) Rework of Electronic Assemblies***
April 26-30
August 30- September 3
December 6-10

Continuing Professional Advancement in Electronics Manufacturing

NEW ***Lead Free Manufacturing***
January 15-16
March 8-9
June 17-18
November 1-2

Design for Manufacturability
February 19-20
May 3-4
August 30-31
December 6-7

Failure Analysis and Reliability Testing
March 15-17
November 29-December 1

Characteristic Properties of Materials
March 29-31
October 25-27

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

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American Competitiveness Institute
One International Plaza
Suite 600
Philadelphia, PA 19113
(610) 362-1200 • FAX: (610) 362-1290
HELPLINE: (610) 362-1320
WEBSITE: www.empf.org

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