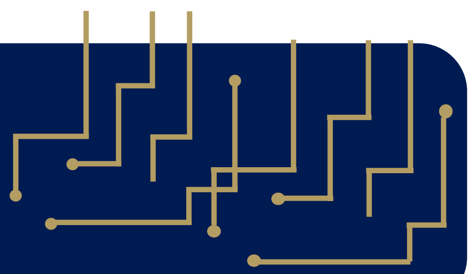
empfasis



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The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application and transfer of new electronics manufacturing technology by partnering with industry, academia and government centers and laboratories in the U.S.

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Beyond Form, Fit, and Function- New Considerations for Legacy Systems

The re-design of current military equipment (formerly known as "legacy" equipment) is most often required to be "form, fit, and function retrofittable". This terminology is used by the military customer to indicate that a replacement is needed that will be interchangeable with the current item. That is, it will take the same:

- shape, material, interfacing, and often appearance (form)
- size, including connectors and weight (fit)
- perform the exact same functions, that is, provide the exact same outputs, given appropriate inputs (function)

In this manner of replacement, it is unnecessary to make changes to interfacing equipment. No perceivable change to the next higher assembly occurs.

Military operations of recent years, however, have encountered environments not previously anticipated. In order to address the new environmental issues, additional requirements have been placed upon any new or re-designed equipment as a reliability and safety precaution. For example, the sand encountered during Desert Storm operations has led AED, the Army Engineering Directorate, to require revised sand/ dust related testing on selected equipment. In many cases, the item being replaced could not have passed these new tests. The replacement item, however, must.

This presents a time and cost increase for the performance of additional tests, but moreover, it presents a new strategy to the design. More stringent testing implies that a hardier design is necessary in order to meet the increased requirements. The replacement must exceed some of the performance levels of, rather than be as good as, the current item.

The changes to electromagnetic interference (EMI) requirements indicate another example of the new testing required. EMI testing allows for the characterization of an item in terms of how incident electromagnetic radiation and other unwanted interference signals will affect the item, and the effect that signals emitted from the item will have on nearby equipment. The signal strengths and bandwidths possible in the defense environment increases as years pass and new threats become un-covered, and as the critical frequencies in use by US forces change. Here again, as in the sand example, current equipment was designed to previous requirements that differed from today's, and was typically less stringent. Depending upon the age of the equipment, cases may be encountered wherein no EMI testing had ever been required.

Figure 1-1

Case Study: C6533 Communications Unit

An example of a legacy item re-engineering effort is the C6533 redesign. This included the design and development of a replacement for the Communications System Control unit of the U.S. Blackhawk and Chinook helicopters (Figure 1-1).

continued on page 2

The unit (Figure 1-2) serves as a link among ground crew, air crew, command radio stations, as well as other aircraft. The previous design used 1969 transistor technology, in an assembly of seven boards and plates that were hard-wired together. The control unit chassis had significant gaps in metalwork through which wavelengths may pass unobstructed. As a simple example, a 10GHz signal may pass through a gap of only 1.25 inches as the wavelength of the signal is 1.18 inches (full sinewave). Precautions for less than quarter-wavelengths should be taken, so, in this example, gaps smaller than .295 inch would be appropriate, in an environment with 10 GHz present.

Figure 1-2

Two characteristics of electromagnetic waves are connected with interference: the amplitude and the frequency of the waves. The control unit chassis had significant gaps in the metalwork into which energy from electromagnetic waves resonating at a quarter wavelength of the signal could have been radiated. Note also that what may be perceived as a shielding issue may actually be a cavity resonance issue. Here, the use of absorptive materials in the cavity has also proven to be effective in damping resonance.

In the older configuration, if an EMI problem were to arise, a correction would have probably included the addition of wire mesh and adhesive-backed copper foil to fill the gaps. These shielding methods, test-bench fixes, may prove to be effective, but interference should be anticipated and prevented in the early design stages of new equipment. The mechanical design of the new communications unit incorporates a more modular assembly and an EMI gasket.

Testing to Show Conformance

MIL-STD-461 incorporates conducted and radiated, emissions and susceptibility tests. Emissions tests are performed to demonstrate that the device under test (DUT) will not emit levels substantial enough to interfere with other equipment. Susceptibility tests are performed to show whether signals in the surrounding environment may adversely influence the DUT. This influence may mean catastrophic failure, distortion of the intended outputs, mis-tracking of data, or other interference with the throughput function of the DUT.

Typical EMI tests

The tests required of the Communications System Control unit included MIL-STD-461 revision E, applicable conducted emissions (CE), conducted susceptibility (CS), radiated emissions (RE), and radiated susceptibility (RS) tests. These emissions tests indicate allowable limits or threshold levels that the unit may not exceed. The susceptibility tests differ from the emissions tests, in that they define the levels to be subject upon the DUT, its interfacing cables, and the power, return, and ground leads. Lines are broken during the test in order to inject or measure conducted levels, whereas, during radiated tests, various antennae and monitors are used at predetermined distances from the DUT. The communications unit was subjected to the EMI tests listed in Table 1-1.

Test	Test Type	Range
CE101	conducted emissions, power leads	30Hz-10KHz
CE102	conducted emissions, power leads	10KHz-10MHz
CS101	conducted susceptibility, power leads	30Hz-150KHz
CS114	conducted susceptibility, bulk cable injection	10KHz-200MHz
CS115	conducted susceptibility, bulk cable injection, impulse	N/A
CS116	conducted susceptibility, transients	10KHz-100MHz
RE101	radiated emissions, magnetic field	30Hz-100KHz
RE102	radiated emissions, electric field	10KHz-18GHz
RS101	radiated susceptibility, magnetic field	30Hz-100KHz
RS103	radiated susceptibility, electric field	2MHz-40GHz

Table 1-1

Figure 1-3

The severity of the 18GHz and 40GHz were not found among the previous requirements for the unit. Figure 1-3 is a photograph of one of the many test setups used.

Comparison With Legacy Requirements

The re-engineered communications unit is replacing technology that is circa 1969. In its last build in 1996, still adhering to the revised requirements of 1974, the unit specification document did contain limited EMI requirements. At that time, the applicable MIL-STD-461 tests included CE01, CE03, CS01, CS02, CS06, RE02, and RS03. Most of these have a similar counterpart from among the revision E tests (i.e. CE101, etc., as listed in Table 1-1).

continued on page 4

Ask the EMPF Helpline!

Customer Issue: The customer wanted to evaluate a proposed supplier's capabilities to manufacture printed circuit boards (PCBs) that meet or exceed IPC specifications and their own internal PCB specifications that were based on the results of seven standard IPC tests.

The customer asked the EMPF Helpline staff to compare the product quality of their current PCB supplier to that of the proposed supplier. They wanted to obtain quantitative data for statistical qualification and tracking. The information would also be applied towards an evaluation of the effect their manufacturing process has on PCBs. The test used to ascertain this information was the dielectric withstanding voltage test.

Test Plans and Technique

The dielectric withstanding voltage tests were performed in accordance with IPC TM-650-2.5.7. The initial testing was performed at 500Vdc (spacing greater than 80um) for 30 seconds in accordance with IPC 6012A. Testing was continued at 50V intervals until failure, or until the limits of the test equipment were reached. The voltage was applied between conductor patterns of the individual layers and an electrically isolated pattern of the adjacent layers. Testing was performed on a total of 12 samples using the test set up shown below in Figure 2-1.

Figure 2-1

Purpose

The dielectric withstanding voltage test (also called high potential, over potential, voltage breakdown or dielectric strength test) applies a voltage higher than the test subject's rated voltage for a specific duration between electrically isolated circuits and portions of a PCB, or between its isolated circuits, portions, and ground. The test is used to determine if the design (including materials and geometries) is adequate so that the PCB can operate safely at its rated voltage and be able to withstand transient over-voltage conditions caused by surges, faults, or other phenomena.

Background

Dielectric breakdown is a phenomena that typically must be avoided in circuit design to prevent failures leading to the replacement of the module and possibly further damage to adjacent circuits. However, some transient protection devices use dielectric breakdown as the method of protection.

Dielectric breakdown, in most laminates, typically results in localized oxidation and the destruction of the material's electrical characteristics. The breakdown can either occur in the laminate itself, or as a result of "surface flashover", where the material immediately adjacent to the laminate (i.e. air, oil, water, surface contaminates) suffers a breakdown. According to manufacturers' data sheets, laminates commonly used in printed circuit boards have a dielectric breakdown voltage of at least 1000 V/mm of thickness. Thus, to withstand a 3KV transient surge, the laminate must be at least 3mm thick. With surface flashover, the root cause must be eliminated within the operational environment. If the circuit is exposed to surface contaminates, moisture, or variations in pressure, a conformal coating (with its own dielectric breakdown) should be considered.

Some transient suppression devices and circuits use dielectric breakdown as a shunt to shift energy away from the rest of the circuit. A transient suppression device is either a sealed device with a self healing dielectric (i.e. gas, oil) that will break down at a specific voltage, or it is an integral part of the PCB design that utilizes air as a dielectric. Gaps are cut in the PCB between circuits at a width that will provide creepage clearance and isolation during normal operation, but would cause a dielectric break down in the air between the circuits in a fault mode. The dielectric breakdown of air is defined by Paschen's Law (V = f{pd}) or the Paschen curve. The curve is usually written as a graph of breakdown voltage (V) vs. the product of gas density (sometimes referred as pressure (p)) and gap size (d). For the designer, it should be noted that while the curve is defined by the function of the gas density and gap size, many other factors such as radiation, dust, surface irregularities, and humidity have an effect on the breakdown of a gap.

Results

The PCBs not only passed the criteria required by the IPC standard, but also the 1000V limitation of the test apparatus. The images in Figure 2-2 show the visual inspection results after the tests, and are representative of all PCBs tested. The image to the left is the top side of one of the PCBs to which wires were soldered. These wires allowed the high voltage testing to be performed at the location shown in the center image. The right image is the bottom side of the PCB. None of the boards that were tested showed physical damage from the application of high voltage.

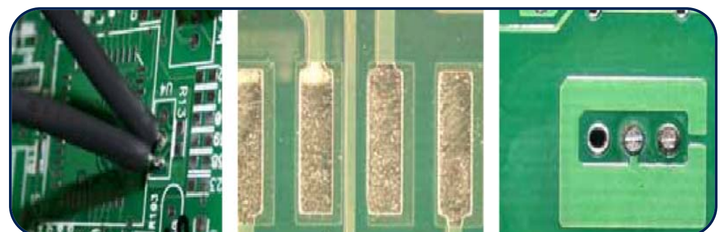

Figure 2-2

continued on page 4

Beyond Form, Fit, and Function- New Considerations for Legacy Systems (continued from page 2)

However, several of the older tests are not directly comparable to the current set. CS02 (30% amplitude modulation (AM) at 1 KHz of all signals 150KHz to 400MHz) has no true counterpart among the revised group of tests, and is taken into account by other CS tests. A test similar to an even older 'RS02' was performed - a radiated susceptibility test called 'induction field' that imposed 400 Hz, 5 Amp rms upon the power line. RS03 (30% AM at 1KHz of all signals 2MHz to 30MHz, 10V/m) compares with today's more stringent RS103 (see Table 1, item 10: 2MHz to 40GHz, 200V/m field strength). The requirements of the older unit indicate that it could not be expected to meet today's EMI requirements.

Conclusion

While the form, fit, and function of legacy equipment must be maintained in re-designed versions, the re-designed items must also adhere to more stringent environmental and EMI requirements.

New requirements and increased testing, such as the changes made to EMI, will help to ensure the survivability of today's defense systems. Becoming familiar with new test requirements, before initiating the design phase of a project, will help to assure that a product will be reliable, and will have minimal issues at the time of qualification.

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Ask the EMPF Helpline! (continued from page 3)

Conclusion

No clear advantage in PCB quality between the two suppliers was obtained from dielectric withstanding voltage testing. However, some clear conclusions were deducted from the testing.

- The PWBs from each manufacturer exhibit similar dielectric characteristics.
- The current PWB fabrication quality exceeds the limitations of the specifications and test equipment.
- Although 500V was specified in the IPC test method, the boards showed no sign of failure when driven to 1000V.
- The current IPC dielectric withstanding voltage test is not an effective test for comparing the product quality of substrate manufacturers. The withstanding voltage test is commonly used as a quality control tool. When PWB quality is high, this test cannot efficiently compare the performance of one substrate manufacturer's PCBs with that of another.

Future plans for test development include increasing test equipment capabilities to exceed 1500V. In addition, material analysis following testing may reveal micro-indicators that can be used to quantify board quality.

Authors of article: *Paul Kelley and Blaine Partee*- Paul is an Electrical Engineer. Blaine is a Materials Engineer at ACI. Comments or questions pertaining to this article can be sent to bpartee@aciusa.org.

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The Advantages of Environmental Stress Screening in Reliability

Product reliability screening processes help define better products through rigourous measurement of predictive behavior. At the EMPF, environmental stress screening (ESS) can be performed on components, board assemblies, and end products to predict their reliability and performance under specific conditions. The EMPF has assisted many customers to determine the robustness of their products.

When performing ESS, it must be thought of as a process rather than a test. There is no accept/ reject criteria, and failures are beneficial. Failures are necessary to effectively predict a product's reliability. Some of the tests that are a part of the ESS process are described below.

- *Temperature cycling*: temperatures are varied between high and low values at a specific rate of change within a thermal cycling chamber (Figure 3-1). This process is repeated (cycled) at a specific time interval. The ability of the component or product to withstand temperature transitions is measured.
- *Vibration*: random and sinusoidal frequencies are implemented in the process to determine mechanical stress limitations.
- *Salt and fog*: salt atmosphere conditions are simulated to indicate the product's robustness in an ocean environment during storage, shipment or use.
- *Temperature/ humidity*: components or products are subjected to a specified temperature and relative humidity to understand the effects of these conditions.
- *High/ low temperatures during storage/ operation*: components or products are tested in storage or under operating conditions at high and low temperature extremes.
- *Rain*: wet conditions are simulated to determine the level of hermeticity that is sufficient to protect against rain penetration.

Figure 3-1

These are just a few of the analytical tools that are available to determine failure rates and service life in components/ products. The failure rates obtained during testing can be used to facilitate improvements in the design of a product or manufacturing process to meet customer expectations.

The ESS process is not complete without comparing the results to the standards and specifications that apply to the customer's needs. These critera are applied to the product to identify the performance level that is expected of it within its intended enviornment. The product may be intended to fit the requirements of many different commercial, industrial, military, or international standards and specifications. At the EMPF, engineers and scientists have performed ESS processes according to several standards and specifications including MIL-STD-810F and IPC-9701, as well as additional customer-specified criteria.

IPC-9701 is an industry specification that manufacturers use to qualify the reliability of commercial products. This specification establishes specific test methods to evaluate the performance and reliability of surface mount solder attachments of electronic assemblies. MIL-STD-810F is a military standard that contains parameters that a material must meet to fulfill the expectations of its service life. The standard also provides guidelines for the ESS process.

The following benefits accrue from a satisfactory ESS program:

- fewer warranty period failures as a result of better operational reliability in the field, promoting a better image with customers and lower repair costs
- help in planning for spare parts
- better economy through fault detection and correction during the product development cycle
- help in making business decisions such as a product's warranty period
- improvement in the overall quality of designs and manufacturing processes
- assistance in streamlining processes to filter out infant mortality failures
- improved productivity
- fewer unexpected product failures in the field

In summary, customers are better satisfied if the product they purchase is reliable and performs to their expectations. An ESS process implemented during the design of a product will improve its service life. Assistance with running an ESS process and the facilities at which to perform such a test are available at the EMPF. Please call the Helpline at 610-362-1320 for more information.

Author of article: *Ron Macapagal*- Ron is an Electrical Engineer at ACI. Comments or questions pertaining to this article can be sent to rmacapagal@aciusa.org.

Verification of Reliability in Components

The verification of reliability in terms of failure modes and their associated calculations is important in understanding the expected lifespan of components in electronic systems. The U.S. Navy is constantly exploring new technologies through the EMPF for both surface vessels and aircraft that require a high level of reliability in harsh environments. Military applications involve the widespread use of new semiconductor devices, especially in the areas of power and radio frequency (RF), which are vital to the long term expansion of military electronic circuits. Gallium arsenide (GaAs) is one of the most popular semiconductors used to fabricate these devices. Semiconductor manufacturers have generally reduced the infant mortality population by improving repeatability in the fabrication process. Much of the available reliability data on long-term failure mechanisms is pertinent to silicon technology. GaAs should not be assumed to follow the same predictions. Thus, the high reliability required for these systems necessitates extended studies on new GaAs technology, particularly monolithic microwave integrated circuit (MMIC) devices. For these new devices, failure mechanisms and mean time between failure (MTBF) rate calculations need to be based on measurements.

Reliability is defined as the probability that an item will perform its intended function for a specified interval of time and at stated environmental conditions. Identifying part failures and failure mechanisms is critical to understanding, predicting, and testing for reliability. Failures can occur as a result of any stress applied to the device such as temperature, environmental conditions, or voltage. The long term failure distribution is usually determined by the chemical and physical properties associated with the technology, design, material, and full impact of the environmental stresses imposed. Qualification testing is essential for the prediction of product reliability. This testing is critical to any reliability program to highlight any deficiencies in the design, and to verify that corrective actions will improve quality. The product should be tested in all of the environments it will experience during its application. These include high and low temperatures, humidity, corrosion, mechanical shock, high pressure, fungus, sand, dust, explosive atmosphere, vibration, and acceleration. [1]

Two areas of qualification can be pursued to verify reliability. Qualification of the process utilizes statistical process control (SPC) to insure consistent device fabrication. This can be used to work toward lower costs and shorter delivery times. Product qualification is essentially a validation of the circuit's ability to perform to a minimum specification under stress and environmental conditions. It typically includes a measurement demonstrating the failure rate of the part using accelerated life testing. By conducting tests in both of these areas, the technology and fabrication of the part may be verified to meet the indicated level of quality and reliability.

SPC provides a baseline for measuring the continuous improvement of a manufacturer's semiconductor production process. The SPC program should use in-process monitoring techniques to measure key process characteristics that affect device yield and reliability. Every device lot typically has built-in control monitors from which data is gathered. The resulting data should be analyzed using appropriate SPC methods to determine the effectiveness of continuous improvement plans. Cause and effect, pareto analysis, and design of experiments can all be used to verify which key characteristics are the most important to measure for quality purposes. Control charts are used to plot data based on the assumption that the data follow a normal distribution. Upper and lower control limits are then calculated from the data. The process capability (Cp) is also calculated and incorporates the upper and lower specification limits (USL, LSL) that are set by the manufacturer. The Cp index compares the statistical process variation to the specification range. If the process variation band matches the specification range exactly, the Cp index is 1.0. The higher the Cp, the more capable the process is of routinely meeting specifications. A general depiction of Cp is shown in Figure 4-1. Curve A represents a Cp of 1 which indicates a capable process, whereas curve B represents a Cp less than 1, and indicates a process which is not.

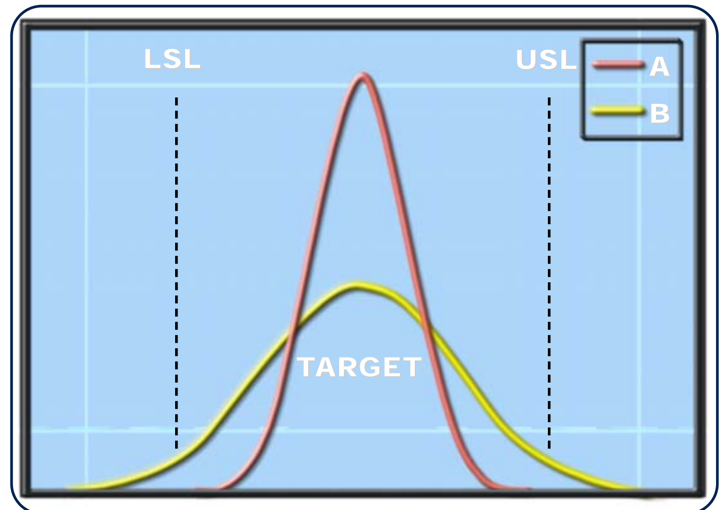

Figure 4-1

For most semiconductor devices, accelerated-life testing is the most common form of qualification used to conduct reliability studies. The most direct method to determine accelerated-life data is to test a large number of samples under applicable conditions and monitor performance against failure criteria over time. Since the lifespan of many military applications is 20 years or more, this method would require an excess amount of time. To gather reliability data in a more practical way, accelerated-life tests at high temperatures are employed. Using elevated temperature reduces the time-to-failure of a component.

Since reliability can be defined as the probability that an item will perform a required function under stated conditions for a stated period of time, it can be modeled as a probability

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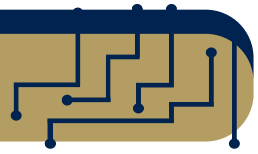
Tech Tips...

Wire Bonding Techniques



As the industry is pushed toward reducing costs and saving space, while also increasing complexity and reliability, wire bonding techniques will play an ever increasing role in the area of electronics manufacturing. For that reason, it is beneficial to review basic wire bonding techniques.

A wire bond is the welded electrical interconnection on a PCB, usually from the semiconductor die to the non-common lead frame or substrate pad. Normally, gold wire is used for interconnecting techniques.

There are three basic wire bonding techniques:

- *thermosonic bonding*: utilizes temperature, ultrasonic and low impact force, and ball/ wedge methods. Figure 5-1 illustrates a thermosonic ball bond.
- *ultrasonic bonding*: utilizes ultrasonic and low impact force, and the wedge method only. Figure 5-2 illustrates an ultrasonic wedge bond.
- *thermocompression bonding*: utilizes temperature and high impact force, and the wedge method only.

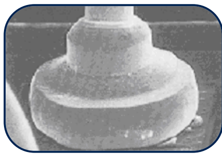


Figure 5-1

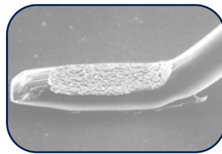


Figure 5-2

The following are the basic requirements needed for successful wire bonding:

1) Cleaning is the fundamental process needed prior to wire bonding. The metallization must be free of organic and inorganic contamination. For example, finger print oil on the bonding area reduces the reliability of the interconnection.

There are two popular cleaning methods, which are plasma cleaning and ultraviolet (UV) ozone cleaning.

- Plasma cleaning is effective for removing epoxy bleed-out, which is caused by outgassing.
- UV ozone cleaning emits significant amounts of radiation(wavelengths 1848A and 2537A) to remove organic contaminants.

2) Setting the proper temperature for thermosonic, ultrasonic, and thermocompression techniques are critical for consistent wire bonding.

- Thermosonic bonding must be set at 100°C-150°C.
- Ultrasonic bonding can be set at 25°C or ambient temperature.
- Thermocompression bonding must be set at 300°C-500°C.

3) Setting the proper force for the thermosonic, ultrasonic, and thermocompression techniques provides the pressure needed for reliable wire bonds.

- Thermosonic bonding requires 0.5- 2.5g force per wire bond.
- Ultrasonic bonding requires 0.5-2.5g force per wire bond.
- Thermocompression bonding requires 15-25g force per wire bond.

4) Setting the proper power is essential for the thermosonic and ultrasonic bonding techniques. To ensure quality bonds, increase the power setting without exerting or over-stressing the wire. You will know over-stressing is taking place when the pull testing device indicates a low break.

5) Make sure the unit is properly clamped in the work hold er, as it is critical that no movement takes place. You can verify this by nudging the object with tweezers. If movement takes place, the unit must be secured during high speed bonding.

6) Make sure the tool (the capillary) is in functional condition. Factors such as bond size, bond pad pitch, wire diameter, harness type, and metallization have an effect on bonding performance. The proper tool selection is essential for consistent wire bonding.

Bonding Evaluation:
After bonding, the wire bond may be evaluated using visual methods and mechanical testing, depending on the requirements and situation. The visual method uses an optical microscope, scanning electron microscope (SEM), and other analytical instruments to find the undesirable bonds. Mechanical testing is employed for the evaluation of bond strength. Wire bond evaluation methods are listed in MIL-STD-883D. They include the following:

1) *internal visual (method 2010, test condition A and B)*: checks for internal material, construction, and workmanship of micro-circuit.

2) *delay measurement (method 3003)*: measures the propagation delay of micro-circuit.

3) *destructive bond pull test (method 2011)*: evaluates the bond strength by hooking and pulling the wire until failure takes place.

4) *non-destructive bond pull test (method 2023)*: detects unacceptable wire bonds while avoiding damage to acceptable wire bonds.

5) *ball bond shear test*: determines the ball bond strength by detecting a "cratering" anomaly that the pull test typically does not.

6) *constant acceleration (method 2001, test condition E)*: finds improper interconnected wires through subjection to high acceleration using 10Kg of force.

7) *random vibration (method 2026)*: rigidly fastens wire bonded devices and subjects them to random frequencies and intensities of vibration to detect discrepancies.

continued on page 8

Cut here and save!

Verification of Reliability in Components

(continued from page 6)

distribution. The probability of a component surviving to a time (t) is the reliability (R(t)).

$$R(t) = \frac{\text{number surviving at instant t}}{\text{number at time t = 0}}$$

The failure rate can be expressed as f(t) below.

$$f(t)= \frac{\text{number failing per unit time at instant t}}{\text{number surviving at instant t}}$$

Thus, the failure rate can be defined as the probability of failure in unit time of a component that is still working satisfactorily. For a constant failure rate f, R(t) varies exponentially as a function of time as given below.

$$R(t) = e^{-f(t)}$$

The failure rate, f(t), is given as the number of units failing per unit time. Since the number of components failing is typically very low, the units are usually reported as the percent (%) failure per $1x10^6$ hours, or as the number of devices failing in $1x10^9$ hours. This unit is referred to as the FIT (failures in time).

1 FIT = 1 failure per $1x10^9$ device hours

Another common method for reporting component reliability is defined by the MTBF. Assuming that the failures occur randomly at a constant failure rate, the MTBF is given below.

$$MTBF = 1/ f$$

This may also be written as the probability of success (P(s)), or zero failures.

$P(s) = e^{(-t / MTBF)}$ where t = time

Figure 4-2 shows P(s) versus time as normalized to the MTBF. From this plot it can be seen that after 1/2 MTBF, the probability of no failures is 60% and after 1 MTBF, the probability of no failures is 37%.

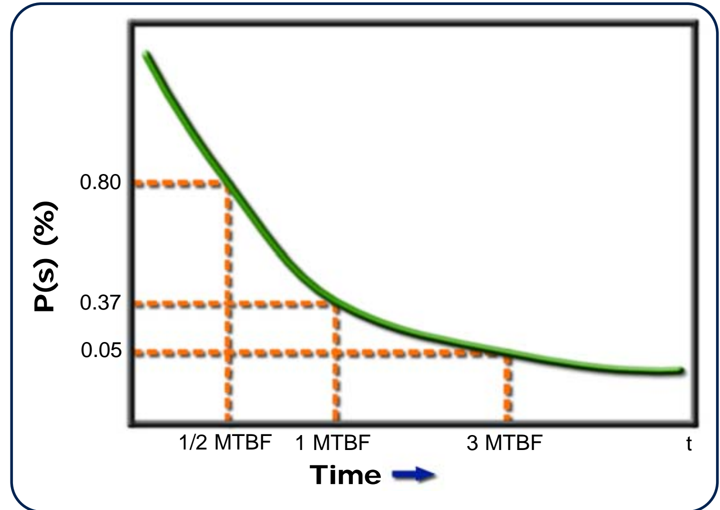


Figure 4-2

In summary, military electronics systems and the accompanying semiconductor devices, particularly GaAs, require thorough reliability testing. This includes both SPC monitoring to observe and improve the key characteristics and accelerated-life testing to gather failure rate data to characterize MTBF and FIT over the long term life of the component and system.

References

1) Mouradian, George, "Basic Elements of Reliability" American University of Armenia, http://www.archassociates.com

2) Kayali, S., Ponchak, G., Shaw, R., eds., GaAs MMIC Reliability Assurance Guideline, JPL Publication 96-25, NASA Lewis Research Center, 1996, pp. 10.

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Tech Tips... Wire Bonding Techniques

(continued from page 7)

8) *mechanical shock (method 2002)*: applies sudden force to wire bonds to produce failures.

9) *stabilization bake (method 1008)*: aims at determining the effect of storage at high temperature without electrical stress.

10) *moisture resistance test*: performed to evaluate, in an accelerated manner, the corrosion resistance to high humidity and heat.

Wire bonding techniques may pose a new challenge to your manufacturing assembly. However, by understanding the different wire bonding techniques with MIL-STD 883D screening methods, you can optimize and refine the wire bonding process that is dictated by your design and the manufacturer's requirements.

** Figure 5-1- image courtesy of Aprova*

*** Figure 5-2- image courtesy of K/S Micro-Swiss*

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Manufacturers' Corner...
METCAL- BGA Visual Inspection System

BGAs, hidden joints, and low standoff heights combine to make traditional post-placement inspection extremely difficult to accomplish. When performing post-placement inspection, there is no line-of-sight access to the solder joints, and with the more conventional electrical testing, it does not yield sufficient long-term quality data.

Until recently, X-ray technology was the only effective option for the inspection of hidden solder joints. However, X-ray systems, depending on the user requirements, tend to be expensive and will require an experienced operator to interpret the X-ray images.

The search for a cost effective solution has led to the development of a bench-top optical inspection system and the introduction of inspection technology that can see beneath array packages to inspect hidden solder joints. It must be stated that optical inspection complements X-ray inspection and is not a direct replacement.

The Metcal VPI-1000-XL (Figure 6-1), which is utilized at the EMPF for all array package inspections, can detect a majority of soldering issues quickly and easily. This optical inspection system utilizes a lens that is enclosed within a mirrored tip. This allows the operator to view beneath array packages with stand-off heights as low as 0.05mm. An articulating lens rotates through 90° horizontally and 5° vertically to allow for both a view of interior solder ball rows beneath array packages and their upper and lower connections.

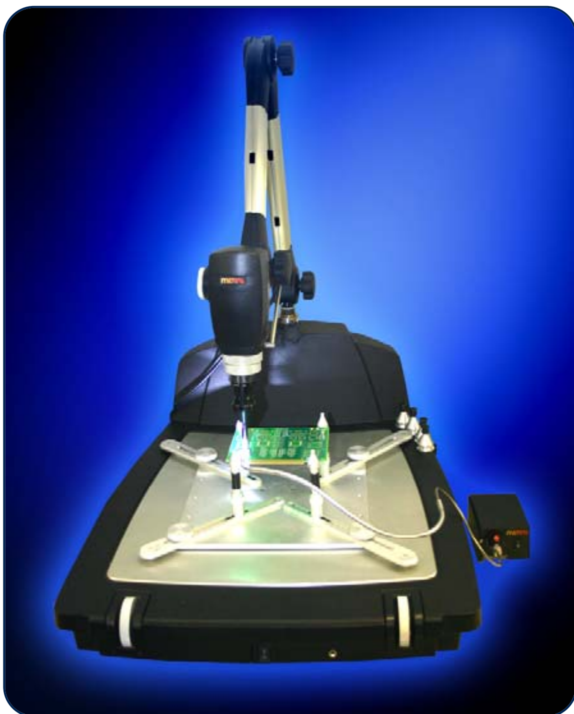

Figure 6-1

The VPI-1000-XL optical inspection system is a versatile system used for inspecting larger PCBs, which are becoming increasingly common in applications such as cellular base stations, data communications and network servers.

For some manufactures, bench top optical inspection is enough. For those requiring the best possible solution, a combination of X-ray and optical inspection offers close to total coverage. In fact, as their assemblies grow in complexity, an increasing number of small to medium sized-manufacturers are investing in bench top optical inspection prior to adding X-ray equipment.

Depending on a manufacturer's needs, optical inspection can provide a cost-effective, high-quality alternative to X-ray inspection. While an X-ray is the only solution for identifying internal defects such as voids, it requires specific technical training to interpret the images and identify defects. However, with optical systems, and especially those equipped with the special lens, any operator with basic soldering and rework experience can easily recognize defects. Defects that are not detected by X-ray, such as unsoldered joints, non-wetting, and flux contamination can be clearly identified and displayed on screen.

Table 2-1 shows a side by side comparison of X-ray and Optical Inspection capabilities:

View	X-ray Inspection	Optical Inspection
Placement	X	X
Bridging	X	X
Show Voids	X	
Cold solder joints	*	X
Reflow Problems	*	X
Excess Flux		X
Contamination		X

X - Yes
* - With training

Table 2-1

Author of article: *Jeff Stong*- Jeff is the Equipment Advisory Board coordinator at ACI. Comments or questions pertaining to this article can be sent to jstong@aciusa.org.

Custom Training

The pace of change in the electronics manufacturing industry requires the continuous acquisition of new knowledge and skills to remain competitive. Companies seeking a competitive advantage through a trained workforce may not find generic certification training and related skills based training enough to clearly differentiate their firm or it may simply not meet all of the current and future training needs of the organization. The development of a custom training curriculum at the EMPF Training Center will address the specific training objectives and work environment needs of a particular organization and deliver a high value, relevant, professional product implemented at either the client's site or at the EMPF's state of the art facility.

The EMPF utilizes a systematic approach to the development of curriculum. The EMPF's team of instructional designers and subject matter experts work closely with clients in order to ensure that the program is successful starting with the assessment phase, through the design, development, implementation, and evaluation of the training program.

This approach has five steps which are:

1) Identify the gap. This process is known as needs assessment. Training needs must be related to the achievement of broader organizational goals, consistent with management's strategy and objectives.

2) Define the training objective. Identify program objectives through operations analysis.

3) Design the training program. One should not select a method or technique for delivering instruction until the subject is clearly defined in terms of objectives. Place emphasis on what is needed before deciding how is to be delivered.

4) Implement the program.

5) Evaluate the program.

Identifying Training Requirements

Ideally, a training plan should be developed by a team represented by management, supervisors, workers and training providers. Begin with a discussion to identify problems occurring in operations. Input from all levels of a company will provide a forum for defining the purpose of the program. The needs assessment must identify the difference between the desired employee performance and the actual performance.

Assessment tools may include surveys, audits, job shadowing, focus groups, skills assessment tests, and self-assessment by workers. Needs analysis tools should provide accurate quantitative and qualitative information while being sensitive to company time and cost restraints.

The EMPF's team will first meet with key members of the client organization in order to help determine needs, establish goals, and perform assessments of the performance environment, student potential, and the training site.

Establishing Training objectives

Objectives should be S.M.A.R.T. That is specific, measurable, attainable, realistic, and timely. The program objectives should be specific to the goals of the organization. If training needs are synchronized with organizational goals and can establish SMART training objectives, then the successful evaluation of the program's results is assured. The EMPF's team will develop performance objectives that will address the client's requirements, needs, and ultimate project goals. Upon approval of the performance objectives by the client organization, the team will proceed with the development of assessment instruments that will determine whether the trainees have met those objectives. Assessment instruments may include written or oral tests as well as laboratory exercises.

Selecting Training Techniques

Once assessment instruments have been finalized, the instructional design team will begin the development of instructional materials and an appropriate instructional strategy (instructor-led, activity-based, computer-based, or a combination thereof). The instructional strategy will be identified as one that will effectively maximize the transfer of skills and knowledge from the classroom to the client's work environment. Delivery methods must take into account the audience, the course content, and the training objectives. For example, there is little point in watching video tapes or listening to lectures if the objective is to demonstrate soldering skills or proficiency in a specific method of rework. Complex subjects can be simplified with demonstrations and directed activities. Tangible examples and hands-on laboratory experience help students make the transition from intellectual understanding to real-world application. The EMPF's unique combination of its demonstration factory, technical instructors, and laboratory facilities provide a hands-on approach, which is well suited to the transfer of technology.

Designing the Program

The information gathered in the previous steps is combined with the experience of the program designers and the tools at their disposal to create the unique course content designed specifically for the individual organization. The instructional design team will be involved in the implementation of the training, and the evaluation of the instructional materials. Follow-up evaluation should verify that the goals of the project have satisfied the company's training needs.

The standard programs offered at the EMPF are exhaustive, and cover nearly every aspect of electronics manufacturing. The standard programs target the various segments of the workforce and manufacturing supply chain. They provide a baseline of information, thus facilitating the transfer of knowledge. Typically, a custom program is based upon one or more of the standard programs, and assembles modules

continued on page 11

Custom Training (continued from page 10)

to emphasize or eliminate material consistent with a client's program objectives. The EMPF Training Center offers customized training programs based on curriculum that focuses on engineering, certification, and skills based training.

Please call the EMPF Helpline for more assistance in developing custom programs.

Author of article: *Guy Ramsey*- Guy is a master instructor at ACI. Comments or questions pertaining to this article can be sent to gramsey@aciusa.org.

EMPF Analytical Laboratory Services

The analytical services laboratory at the EMPF provides a full range of solutions tailored for the electronics manufacturing industry. All testing is conducted in accordance with IPC, JEDEC, ASTM, Belcore, and MIL-STD specifications.

The EMPF not only provides quick and accurate results but also root cause analysis and recommendations on how to prevent re-occurrence.

Please contact the EMPF Helpline at 610-362-1320 for more information about the following tests, or any other tests not listed.

- Scanning Electron Microscopy (SEM) w/ Energy
- Dispersive Spectroscopy (EDS)
- Fourier Transform Infrared Spectroscopy
- Ion Chromotagraphy
- Wetting Balance
- Differential Scanning Calorimetry/ Thermographic Analyzer
- Optical Microscopy w/Digital Imaging
- Bulk Cleanliness Testing
- Microsectioning
- Failure Analysis
- Transmission X-ray Imaging
- Thermal Cycling
- Shear Testing
- Temperature/ Humidity Testing
- Vibration Testing
- Thermal Shock Testing
- Highly Accelerated Stress Testing

The EMPF training center has many classes that highlight specific areas of electronics manufacturing. Some of the upcoming course offerings include:

- IPC 7711 Certified IPC Specialist (CIS) SMT Rework *July 21-23*
- Boot Camp A *July 26-30*
- Boot Camp B *Aug. 2-6*
- IPC-J-STD-001 Instructor Certification *Aug. 9-13*
- IPC-A-610 Instructor Certification *Aug. 16-20*
- SMT Manufacturing *Aug. 23-27*
- Design for Manufacturability *Aug. 30-31*

Call the registrar today to enroll and find out about all of the course offerings at the

EMPF Training Center
610-362-1320
or visit www.empf.org

EMLC Upcoming Course Schedule 2004

Skills

SMT Manufacturing
August 23-27

BGA Manufacturing, Inspection & Rework
July 19-20
November 29-30

Chip Scale Manufacturing
November 15-17

Electronics Manufacturing

Boot Camp A NEW
July 26-30
October 4-8

Boot Camp B NEW
August 2-6
October 11-15

Certifications

IPC J-STD-001 Instructor Certification
August 9-13
September 13-17
October 18-22

IPC-A-610 Instructor Certification
August 16-20
September 20-24
October 25-29

IPC Challenge NEW
July 14
September 1
October 27
December 8

IPC/WHMA-A-620 Requirements and Acceptance for Cable and Wire Harness Assemblies (CIS) NEW
November 15-17

IPC-7711 Certified IPC Specialist (CIS) SMT Rework NEW
December 1-3

J-STD-001 Instructor Recertification NEW
July 15-16
August 30-31
October 28-29
December 6-7

IPC-A-610 Instructor Recertification NEW
September 2-3
October 25-26
December 9-10

IPC-7711/7721 Certified IPC Specialist (CIS) SMT Rework and Circuit Repair
July 12-16
October 4-8

IPC-7721 Certified IPC Specialist (CIS) Circuit Repair
November 18-19

IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCBs
September 7-10

IPC-7711 Certified IPC Specialist (CIS) Rework of Electronic Assemblies
August 30- September 3
December 6-10

Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing
November 1-2

Design for Manufacturability
August 30-31
December 6-7

Failure Analysis and Reliability Testing
November 29-December 1

Characteristic Properties of Materials
October 25-27

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

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