empfasis

A publication of the National Electronics Manufacturing Center of Excellence *November 2004*

American Competitiveness Institute

ISO 9001-2000 Certified

American Competitiveness Institute
One International Plaza
Suite 600
Philadelphia, PA 19113
(610) 362-1200 • **FAX**: (610) 362-1290
HELPLINE: (610) 362-1320
WEBSITE: www.empf.org
www.aciusa.org

The EMPF is a U.S. Navy-sponsored National Electronics Manufacturing Center of Excellence focused on the development, application, and transfer of new electronics manufacturing technology by partnering with industry, academia, and government centers and laboratories in the U.S.

EMPF Director
Michael D. Frederickson
mfrederickson@aciusa.org

In This Issue

Office of Naval Research Manufacturing Technology Program

ONR Program Officer
Richard Henson
hensonr@onr.navy.mil

Technology Refresh Planning Aids in Sustainment of Military Systems

An effective technology refresh plan establishes the points along the service life of a product or system when it is optimal to change, or "refresh," both custom-built and commercial-off-the-shelf (COTS) system components within a larger military system or platform to ensure continued supportability throughout its lifecycle. The EMPF is currently working with its partners, Advanced Technology Institute, Lockheed Martin Advanced Technology Laboratories, and Altarum, on a Navy ManTech project to develop advanced technology refresh tools to support military platforms currently in use by our warfighters. Having a viable technology refresh plan is vital to the mission of supplying the warfighter with hardware that is technically capable, available, sustainable, and cost effective. The changes can be in the form of an electronic component substitution/replacement, or in the form of a re-design of the product. That is, if a military product is to be produced and/or sustained over many years, then there will be points when it is necessary to replace components in the design, or as mentioned, perform a re-design.

There are different interpretations about what influences a technology refresh plan. Here, three factors are considered: 1) Obsolescence risk; 2) New technology benefit; and 3) Requirement change (Figure 1-1). The most well-known impact on technology refresh is obsolescence. It is known that military electronics make up less than 1% of sales in the electronics product market. In addition, military electronic products/systems typically have extremely long lifetimes compared to consumer electronics (decades vs. months in some cases). These two factors are the cause of component obsolescence being a well-known risk with military electronic systems. If a system supplier builds product today with a certain set of components, it is likely that in time, consumer product designs will change at a rapid rate, forcing a change in components that are in demand. Various components of the military system may no longer be profitable for the component supplier to offer, and thus become obsolete.

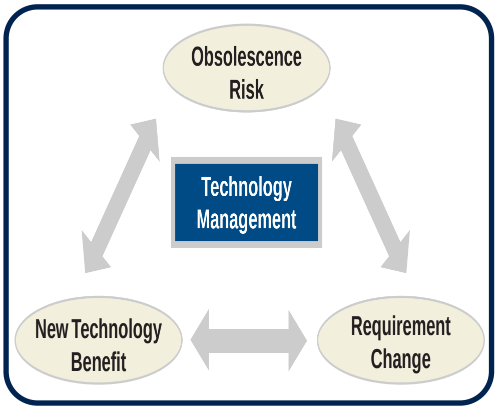

Figure 1-1 – Depiction of the interrelationship of information categories that can impact technology management.

Once it is known or predicted that certain components present an obsolescence risk, there are numerous responses. The three main responses are the following: 1) Execute a long-term buy of the subject component in order to have it on hand for the future; 2) Identify and utilize a substitute part; or 3) Perform a re-design of the product, thus ensuring current, available components are utilized. Each of these responses can lead to costly inefficiencies. For instance, excess component buying is costly from both a purchase and an inventory standpoint. Substitute parts may require timely qualification testing, and re-designs are typically time consuming and costly undertakings. These points illustrate the importance of optimizing the response to component obsolescence risk. This response is part of the technology refresh planning process.

continued on page 2

Technology Refresh Planning Aids in Sustainment of Military Systems

(continued from page 1)

In addition to obsolescence, two other factors can impact a technology refresh plan. First, with the dynamic consumer electronics market, new electronics technology is available regularly. Understanding when the benefits of new technology outweigh the time and cost associated with re-designing a product to implement the new technology is another aspect of a technology refresh plan. Second, customer requirements change, often requiring more capability. This desire for change manifests itself in the need to perform a re-design of the product or system. Knowing the requirement upgrade schedule can impact the optimal time to perform technology refresh.

Currently, there are numerous software tools/services commercially available to assist in technology refresh planning. The main categories of tools include obsolescence identification, analysis tools, and road mapping tools. Obsolescence tools help identify and, in some cases, predict when certain electronic components will become obsolete. Analysis tools include tools to schedule an optimized re-design, or refresh, schedule. Other analysis tools involve reliability or cost evaluations. Road mapping tools can be used to form a requirements upgrade schedule as well as the more familiar new technology readiness application. Many such tools are described and in some cases accessed via the Diminishing Manufacturing Source and Materials Shortage (DMSMS) Center of Excellence website (www.dmsms.org). Another prominent multi-functional tool/service is called the Obsolescence Management Information System (OMIS) out of the Navy Underwater Warfare Center in Keyport, WA. By using a combination of available tools and services, the three vital categories of information needed for optimum technology refresh planning – requirement change, obsolescence risk, and new technology benefit – can be defined, tracked, and integrated into one cohesive technology refresh plan.

Current practices address the three technology refresh planning aspects listed in Figure 1-1, but these efforts are fragmented in nature, resulting in a less than optimized technology refresh plan for a module, system, or platform. One main issue relates to the fact that the appropriate information detailing the up-to-date status of a system's requirements, component obsolescence risk, and new technology insertion opportunities, is not well defined, not visible, and not available to all pertinent parties, including the DOD customer, the prime, and the system suppliers. The EMPF-led Technology Refresh for Navy Transformation (TRENT) program focuses on defining and demonstrating a system framework that uses existing software tools to define the status of requirements, obsolescence risk, and new technology opportunities, as well as to disseminate that information to the needed program Government sites, companies, and personnel. By achieving this activity, TRENT intends to demonstrate that a defined and coordinated sharing of important technology refresh information results in a more

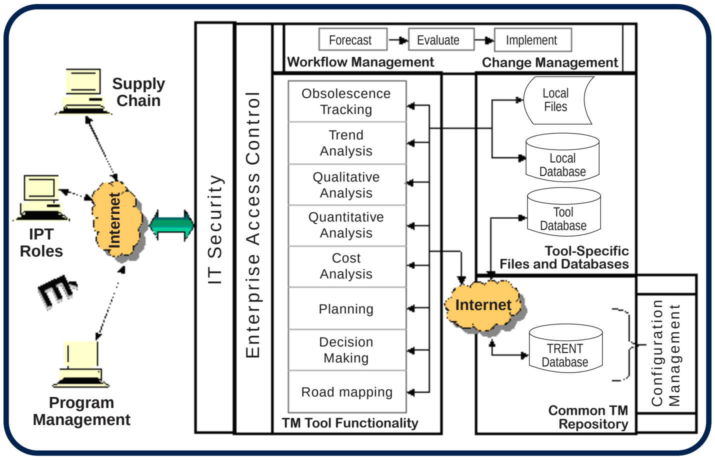

Figure 1-2 – TRENT Collaborative Framework Architecture (Courtesy Lockheed Martin Advanced Technology Laboratories)

optimal technology refresh plan for the systems of a military platform. By achieving an integrated and complete technology refresh plan, cost savings can result due to reduced excess component buying/inventory and a reduced number of costly re-designs of a product/system.

Figure 1-2 shows a conceptual example of the type of framework necessary to maintain, update, and distribute the technology refresh information properly. This framework must also ensure security and informational configuration management so that existing conditions at the time of decisions can be reviewed for justification and decision improvement purposes.

As the commercial electronics world continues to grow evermore dynamic in technology advancement and products, the military electronics producers will need to continue to adapt and blend their long product life cycles with timely refreshes in technology. The three main drivers of such changes – requirement change, obsolescence risk, and new technology benefit – need to have related information tracked and distributed to the important players in the supply chain. The TRENT program is defining and demonstrating a means to accomplish this objective. Only through efforts such as this can a complete picture be drawn that allows an optimized technology management/refresh plan to be embraced and understood by all concerned. Efforts such as this will allow military electronics producers to not only keep pace, but to take advantage of the giant consumer electronics industry, thus ensuring that the needed electronics hardware is available and sustainable for our forces in the field.

Author of article: *Greg Wood* – Greg is a Program Coordinator at ACI. Comments or questions pertaining to this article can be sent to gwood@aciusa.org.

Training for BGA: Manufacturing, Rework, and Repair

Ball Grid Array (BGA) and Chip Scale Packages (CSPs) are gaining popularity as the demand for smaller and faster circuitry increases in electronics manufacturing. The BGA and the more leading edge CSP are packages designed to be soldered to surface land patterns on an assembly substrate. Careful design consideration and process control is critical with these types of packages, making workforce training a key factor in the successful design and production of BGAs and CSPs. The EMPF offers a two-day course in BGA Manufacturing, Rework, and Repair. During this course, participants will learn about the issues that are associated with designing and manufacturing assemblies utilizing BGAs and CSPs. Some BGA process considerations and recommendations that are examined in detail during the course are highlighted in this article.

The characteristics of BGAs

There are many types of BGA and CSP packages. Most of these packages have some type of package substrate, providing mechanical support and an electrical interface. Characteristics of the more common types include high temp solderballs, eutectic solderballs, and Land-Grid Arrays (LGAs). LGAs do not have solderball attachments and provide only a land grid on the package substrate. BGAs with high temp solderballs rely on printed solder paste to attach the package to the assembly substrate. The solderballs are usually attached to the package with eutectic solder. When subjected to reflow, the balls are free to disengage from the package. This constitutes a difference between BGA and other SMT packages.

The solderball of a eutectic-attached BGA provides about 80% of the solder volume at the package-to-board interface. Solder paste provides flux, which promotes good wetting of the ball to the assembly substrate. The fact that the package-to-assembly interface melts to form the electrical interconnect is unique to this SMT package.

LGAs are quite similar to the old leadless chip carriers (LCC). The primary difference between the LGA and the traditional LCC is that the package-to-assembly interconnects are hidden under the package. The hidden interconnect presents the single biggest challenge to manufacturers of assemblies employing this family of components. It is not possible to touch or directly inspect the solder connections under the package.

BGA manufacturing issues related to materials

- **Solder**: The industry is transitioning from Lead (Pb) solder to Pb-Free solders. Some packages are available with Pb-Free balls. Some are available with Pb-Free balls only. Attempts at mixing Pb-Free BGAs with SnPb solder have yielded poor results. While it is standard practice for other SMT package types, do not attempt to mix Pb-free area array packages with solders containing Pb.
- **Flux**: Optimize your process so that no changes should be required. If you are using a no-clean process, make sure the flux under the package is processed adequately. The process goal is to expend all the flux and immediately enter reflow. Reaching reflow too quickly may produce voids. Burning off all of the flux and soaking just below reflow, prior to reflow, may result in non-wetting at the assembly interface.
- **Paste**: We have observed that some pastes have a tendency to produce a percentage of voids. A given paste may perform very well with traditional SMT package types and be simply unacceptable for use in assemblies that have area array packages.
- **Underfill**: Very small CSPs may require underfill adhesive to provide mechanical strength. The solder attachments alone may be inadequate to secure the package to the assembly. An underfill needs to be selected based on its compatibility with the other assembly process steps, the normal service environment, and assembly serviceability.

Level	Floor life (out of bag) – ambient temperature and humidity ≤30˚C/60% RH
1	Unlimited
2	1 year
2A	4 weeks
3	168 hours
4	72 hours
5	48 hours
5A	24 hours
6	Mandatory bake before use. After bake: Reflow within time limit specified on label

Figure 2-1 – Moisture Classification Levels from J-STD-020

BGA manufacturing issues related to components

IPC J-STD-020 establishes test methods and criteria for moisture sensitivity in BGA packages (Figure 2-1). PBGA (Plastic Ball Grid Array) packages absorb moisture, making them susceptible to warp, swell, popcorn (a type of delamination) or crack when processed without appropriate care. IPC J-STD-033 provides guidance on how moisture-sensitive devices should be handled. Check on the JEDEC website (www.jedec.org) for status of the standard and to download the current version.

- **Solderability**: Solder joints exhibiting poor wetting can result in premature failure as a result of mechanical and thermal cyclic loading. Proper storage and handling of components will eliminate many of the solderability issues.
- **Assembly**: Stencil printing for area array packages is less difficult than for fine-pitch, leaded SMT components. However, the risk is greater. Placement requirements may not be as rigorous as those for peripheral leaded packages with similar IO count. Unlike a Quad Flat Package (QFP), the PBGA package tends to self-align on the land patterns during the reflow process. Placement errors less than about 50% of the ball diameter that do not generate bridges will move toward the center of the land pattern. CCGA packages will not "self-align" during reflow, nor can you expect an LGA to float to the target as a result of wetting forces and surface tension.

continued on page 9

Reverse Engineering Key to Sustaining Undocumented Printed Circuit Board Assemblies

When companies are faced with the challenge of manufacturing an undocumented and partially obsolete printed circuit board assembly (PCBA) with only the PCBA as the starting point, the reverse engineering process can be a useful tool for reconstructing the design and production documentation, thus enabling its manufacturability using available and technically compatible components. There are many challenges for the manufacturer in the reverse engineering process, but following some standard process guidelines will increase the probability of manufacturing success and can indefinitely prolong the useful life of an aging PCBA.

Careful planning at the outset is critical to ensure that the necessary equipment, tools, software, expertise, and of course, the PCBAs are readily available. Having several boards on hand provides some flexibility and expediency to the process by allowing some parallel processing of the non-destructive re-engineering steps.

The first step should be the documentation of the components on the board. Access to the various electronic component vendors' databases (current and previously published catalogues, specifications, cross references, etc.) is a good resource for component types and replacement component part numbers. This identification of components will lead to the development of the bill of materials (BOM) for the PCBA, an important documentation step in reconstructing the production materials needed. Coincident with the BOM development, color digital images of the PCBA should be taken. Detailed images are invaluable in the later reconstruction steps of the board layout.

Various methods and tools can be used to regenerate the electrical design of the circuit assembly. An in-circuit tester can be used to generate point to point connections, which include generating a net list, and determine some or all of the values for the components on the board. A system such as ScanCad can be used to regenerate the Gerber files for each layer of the board. X-ray imaging can also help clarify point to point connections. These tools are essential for efficient reverse engineering.

Conformal coating of the PCBA can complicate the task. The type of coating and how to remove it without damaging the board assembly will determine the overall level of difficulty for the reverse engineering process. If the type of conformal coating is not known, observation and testing will help identify the type of coating and the process required for removal. Several removal techniques are available, including using solvents, peeling, thermal, grinding and scraping, and micro-blasting. After removing any conformal coating, component removal can begin. Great care must be taken to insure that the underlying board remains sufficiently intact. Proper use of the right tools and equipment will save the board from damage and preserve it for any remaining analysis.

Up to this point, a list of components on the PCBA should be available from the BOM. Information gathered from an in-circuit tester and/or x-ray machine will be used to develop the design schematic. With this data and the BOM, one can use any of a number of computer aided design (CAD) software packages capable of circuit design and layout to generate the Gerber file, which is the machine code for circuit artwork. This may not replicate the same layout as the original PCBA and depending on the end application, further design work on the PCBA may be necessary to create the replacement design.

Many printed circuit board (PCB) fabricators and vendors claim that there is no easy way to take a PCB apart, layer by layer. Most boards are made of prepreg with an epoxy resin, a copper-clad surface etched for the circuitry design, patterned solder mask, a silkscreen print of the reference designators, and a finish plating on the exposed copper. These materials are designed to keep the PCB intact and to prevent separation, and to conform to strict commercial standards (designed to ensure PCB quality and reliability) but do make the task of separating the layers very difficult.

The board must be separated, layer by layer, which requires effort and patience. In some cases, a poorly constructed board can be separated mechanically using a knife and then pried apart (Figure 3-1).

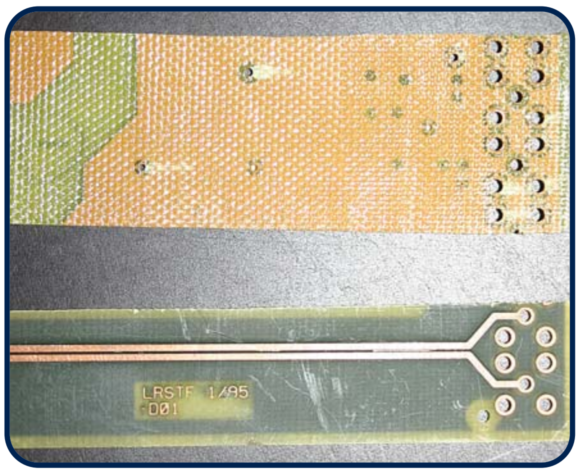

Figure 3-1

A chemical application may be needed to help separate the layers without damaging the board. Methyl Ethyl Keytone (MEK) can soften the epoxy that bonds the layers together. This technique was developed through small sample testing on a modern, well-laminated board. The key process variable was to determine the quickest method to get the MEK soaked into the PCB. One sample was soaked in MEK for a set time period, another was soaked in MEK and then heated to 40°C, and the last was dipped in MEK for a few seconds. In this trial run, it was determined that heating of the MEK helped the PCB absorb it more rapidly. Caution should be taken when working with MEK. Please consult the MSDS. When the PCB is fully soaked, there is not much time before the MEK evaporates and the board re-hardens. This process of delaminating will take longer to work through a thicker board. Figure 3-2 shows the result of this technique.

continued on page 6

Ask the EMPF Helpline!

A customer called in to the Helpline with a signal quality issue on input and output pins/leads of a component on their board assembly. The customer mentioned that the board assembly had been serviced a few times and signal quality had not improved. Residue was also found at the pin/lead tips of the component.

The Helpline team member's initial response was possible oxidation on the pins. An investigative plan was formulated, consisting of the following:

- Visual inspection – optical microscope and x-ray
- Surface finish analysis – Auger analysis
- Cross-sectional optical analysis – Scanning Electron Microscopy (SEM) with Energy Dispersive Spectroscopy (EDS) analysis

The visual inspection revealed areas of concern on the pins/leads of the component. It was noted that the plating appeared to be scratched, possibly exposing the inner layer of the pins/leads (Figure 4-1). The residue on the tips was found to be discoloration on the surface of the pins/leads, which could have been due to oxidation as initially suspected. X-ray inspection showed no problem with the die of the component and the mating socket.

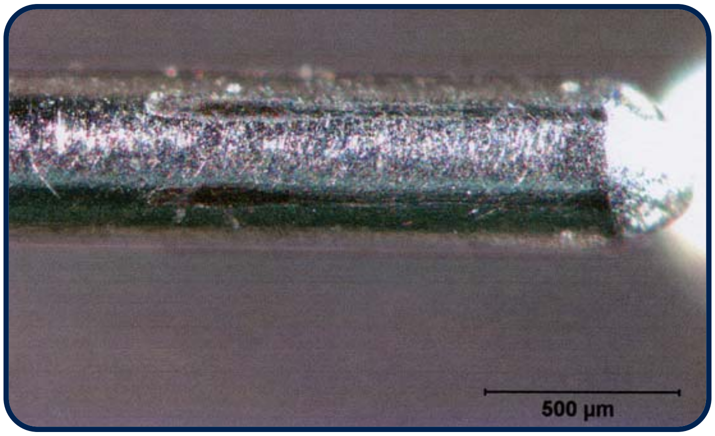

Figure 4-1 – Pin/lead of the component

The Auger analysis indicated the presence of Lead, Tin, and high levels of Carbon on the gold plating of the socket. This suggested that the Lead and Tin were transferred from the pin/lead to the socket. The area referred to can be seen in Figure 4-2.

The SEM images showed the area of the scratches and EDS reading of the socket further supported the Lead and Tin transfer to the gold plating of the socket (Figures 4-3 and 4-4).

The high levels of Carbon present piqued some interest. A Fourier Transform Infrared spectroscopy (FTIR) analysis was conducted to determine the origin of the organic compound. The result implied that the component was handled with bare hands.

Conclusions

1) The contamination from handling the component pins/leads with bare hands increased the chances of added resistance to the pin/lead and socket.

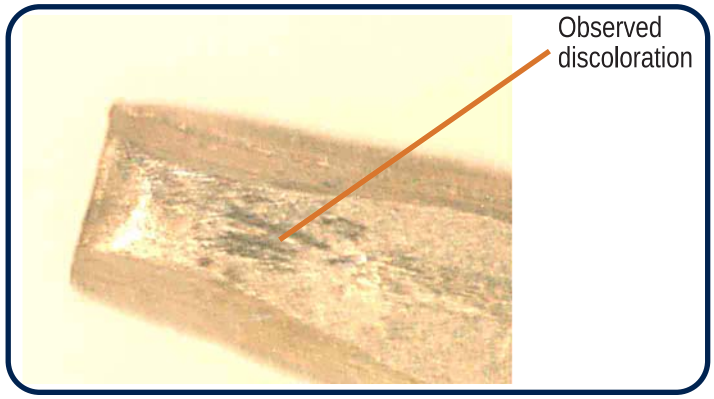

Figure 4-2 – Socket contact

2) The results from the Auger and SEM/EDS analysis pointed to the phenomenon of fretting corrosion.

Fretting corrosion is a process caused by the motions of mating contact surfaces and results in contact failure. Fretting is also influenced by vibration and thermal excursion. In conditions where the resonating and operating frequency match, vibration will have an impact on the degree of fretting. Aircraft and shipboard applications commonly have these conditions which can affect the connections of a component to its socket. Extreme temperature change can cause expansion of materials with different thermal expansion coefficients.

Increasing the holding force of the socket to the pin/lead is not a viable solution. Over time, those forces will also degrade and create the same fretting conditions. Repeated replacement of the component also degrades the holding forces.

Figure 4-3 – Pin/lead at 500x

Recommendation

With the possibility of vibration and thermal exposure to the board assembly, one solution is to match the plating surfaces of both the pin/lead and the socket. This will prevent

continued on page 11

Reverse Engineering Key to Sustaining Undocumented Printed Circuit Board Assemblies

(continued from page 4)

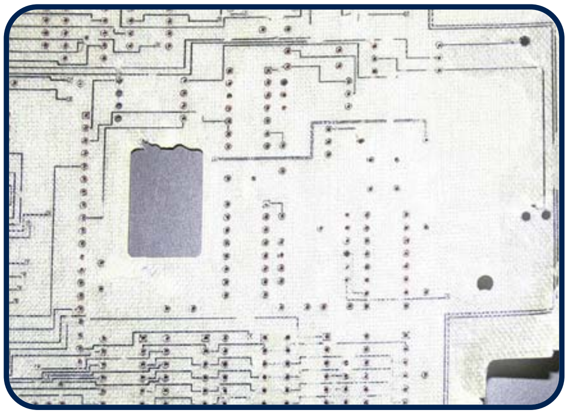

Figure 3-2

After successfully separating each layer, the next step is to create the original Gerber file. There are commercially available systems that can replicate the artwork of the circuit layer by layer. This is done by scanning the board or each of its layers and capturing the image of the circuitry layout. One such system is ScanCad, which is currently used at the EMPF. With help from the software, the operator can begin tracing the image. After creating the PCB artwork, it can be verified with the original schematic that was previously generated. The BOM, schematic, and the Gerber file completes the supporting documentation to recreate the original PCBA.

Reverse engineering is not a straightforward process and requires technical expertise, patience, the proper tools and equipment, and the ability to make adjustments to fit the PCBA and the application. Successful results can extend the useful life of many PCBAs and, more importantly, the continuation of their end-use applications in systems and devices. It is important to know that existing PCBA designs may have proprietary restrictions on their use, so some prudent due diligence on design ownership is important prior to starting any reverse engineering process.

Author of article: *Ron Macapagal* – Ron is an engineer at ACI. Comments or questions pertaining to this article can be sent to rmacapagal@aciusa.org.

Tech Tips... Thermal Cycling for Non-Destructive Product Screening

Thermal cycling can be used to non-destructively screen PCBs for potential defects. The purpose of the following technical tips is to help with the setup of the thermal cycling chamber and its usage for non-destructive screening.

Thermal cycling chambers require an ample supply of cooling water, and it is important to follow the equipment requirements. Most thermal cycling chambers have a water chiller system that holds cooling water just above freezing, at approximately 5°C. Since these systems are typically kept in remote parts of the infrastructure, it is important that properly sized piping is kept throughout the line. For a large thermal cycler that has upwards of 33 ft^3 of space, ¾" pipe is required at the input of the chamber. If the supply line is less than required, the chamber will not be kept full for optimum heat transfer. Flow meters are not used within the chamber. A pressure differential switch is used instead. The pressure differential switch monitors the pressure drop across the chamber as a voltage. For the particular chamber at the EMPF, the water pressure required to input to the system is a constant 10psi. A decrease in water flow, and hence the pressure, will cause the signal voltage to trigger an alarm and shut down the chamber. It is not recommended by the manufacturer to bypass the sensor, although this can be done by simply shorting the sensor signal lines together.

Thermal cycling chambers are typically used for 500 to 1000 cycles for product reliability testing, so both the electrical and water supply must be reliable over the duration. Breaks in the electrical supply will trigger an alarm and can cause a reset of the testing program and a stop condition unless it is specifically programmed to resume testing on revival of power.

Alarms that are triggered from various temperature and pressure sensors throughout the unit can also signal a more critical failure. One such sensor is a pressure sensor of the stage-two compressor. A low signal indicates loss of Freon coolant and requires repair from the manufacturer. It is important that the user contact the manufacturer and become familiar with the different alarms that can occur on the unit. Some of the alarms require only a simple reset to continue, while others indicate major malfunctions with the unit.

Thermal cycling is used to burn-in the PCB for potential defects that may have been present in the plated through holes. Boards are thermal cycled through a standard range from -55 to 70°C to screen for thin plating (Figure 5-1). The units have large volume, 33 ft^3, and can cycle more than 150 large boards during a run.

During experimental planning and setup, it is important to consider the size of the boards and ensure that holders are appropriate and allow for proper clearance of components. The thermal cycler has forced air convection which can cause erratic movement of the boards on the board tray. It is important that the boards are positioned securely to avoid damage. The chambers typically have an internal light for easy viewing of any motion or vibration of the boards. If the boards have some margin area on the edge, placement in the board tray will allow for proper clearance for all components. A brief inspection for obvious defects, at handling stages such as loading of a chamber, is important to perform so that the root causes of any failures observed after thermal cycling are not misdiagnosed.

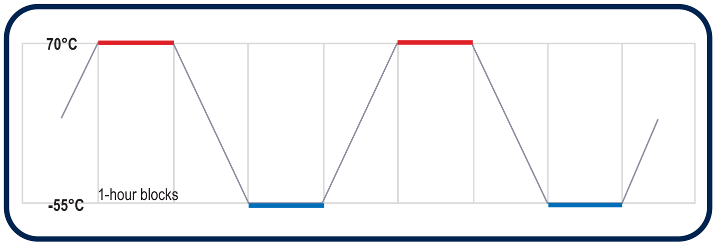

Figure 5-1 – Burn-in cycle (8 hours) from -55°C to 70°C

It is important to discriminate failures that occur from thermal cycling from those that occur from other causes. Boards should first be electrically tested to verify functionality prior to thermal cycle testing. From our experience, the EMPF has observed damage to circuit boards that occurred during shipping. A brief inspection for obvious defects at handling stages such as loading and unloading of a chamber is also important. Electrical connections within the chamber must also be correct and reliable in order to ensure that failures that occur are from thermal cycling and not from intermittent connections. These are important tips to consider so that the root causes of failures observed after thermal cycling are not misdiagnosed.

Thermal cycling is a useful method for non-destructive screening of PCBs. After thermal cycling, boards can be screened for electronic failures by contact probing. If failures are present within a via, they will indicate thin plating of the via. This can be confirmed by microsection analysis and measurement with a microscope.

Author of article: *Anthony Vigliotti* – Anthony is a Materials Engineer at ACI. Comments or questions pertaining to this article can be sent to avigliotti@aciusa.org.

Analysis of RF Signals for Sustainment of Military Communications Systems

The ability to analyze Radio Frequency (RF) signals is critical in applications involving military radios and avionics equipment. Staff at the EMPF have successfully measured the signal content of a survival radio waveform for the AN/ARS-6 commercial-off-the-shelf / open architecture upgrade. As part of the airborne rescue platform for a Combat Search and Rescue System, the AN/ARS-6 is used to locate the position of a survivor's handheld radio. RF signal measurements were performed on the AN/ARS-6 using several instruments, including wireless communication, vector signal, and spectrum analyzers.

Background
RF measurement techniques can generally be divided into three major categories of analysis – spectral, vector, and network. Spectrum analyzers, which provide basic measurement capabilities, are the most popular type of RF instrument in many general-purpose applications. With a spectrum analyzer, the user can view power vs. frequency information and can sometimes demodulate analog formats such as AM, FM, and PM. Vector instruments include vector or real-time signal analyzers. These instruments analyze broadband waveforms and capture time, frequency, and power information from signals of interest. Network analyzers are typically used for making S-parameter measurements, which are often performed on RF components.

Spectrum, vector, and network analyzers offer different functionality to the end user. All analyzers are generally built on either a scalar or a vector architecture, each of which has its advantages and disadvantages. Because it is narrowband in nature, a scalar architecture is not well suited to analyzing the broadband signals which are becoming more prevalent in today's marketplace. In addition, a scalar architecture gives only a 2-dimensional (power vs. frequency) view of the acquired signals, and is typically slower than vector-based.

Vector analysis
To accurately capture and characterize broadband signals, it is necessary to change from narrowband measurement equipment to broadband vector instruments. Using vector instruments with a real-time bandwidth equal to or wider than the bandwidth of the transmitter, it is possible to capture all signals of interest from the device under test.

Though typically more expensive than scalar instruments, vector instruments provide faster measurements and more complex signal analysis and generation.Vector instruments use wider filters than narrowband instruments such as spectrum analyzers. Because this width reduces the number of times the filter must be retuned, a vector instrument can sweep across the frequency spectrum more quickly. With vector architecture, it is possible to generate complex signals such as the modulated waveforms used in most modern cellular communications systems.

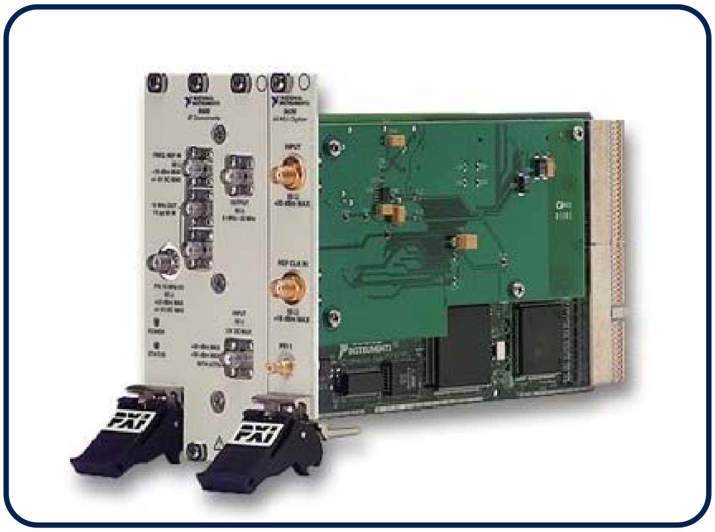

Figure 6-1 – PXI-5660 RF Signal Analyzer

In addition to capturing broadband signals, vector instruments deliver other key advantages to your measurement application. When performing spectral sweeps or other measurements that span a large frequency range, the wide real-time bandwidth of a vector analyzer can dramatically improve test time. For example, the new PXI-5660 RF Signal Analyzer (see Figure 6-1) from National Instruments features a 20 MHz real-time bandwidth and delivers measurement throughput advantages from 30 to 200 times that of traditional instrumentation. The EMPF has utilized this PXI (PCI eXtensions for Instrumentation) based signal analysis system to characterize military communications waveforms. Figure 6-2 shows a block diagram of how the individual modules within the RF signal analyzer characterize incoming signals.

Spectrum analyzer background
At the most basic level, a spectrum analyzer can be described as a frequency-selective, peak-responding voltmeter calibrated to display the root-mean-square (RMS) value of a sine

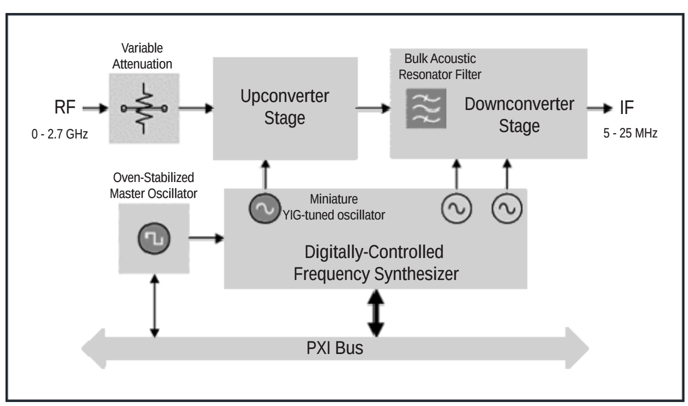

Figure 6-2 – Individual modules within the RF signal analyzer

continued on page 11

(continued from page 3)

• **Reflow**: The process of reflow soldering does not change, but your ability to evaluate the process does. Preheat ramp and soak must be hot enough to drive the volatile compounds out of the flux, to reduce voids. The preheat cycle must be slow enough to allow all of the parts on the board to reach this state but fast enough to prevent oxides from forming on the substrate lands after the protective compounds have been driven from the flux. Developing a good time/temperature profile can be difficult and counterintuitive. Small CSPs can be harder to heat than large BGAs. Heavy PWBs, CBGAs, PBGAs, TBGAs, heat spreaders in packages, and high power components can prove to be a significant challenge even with the best reflow equipment.

Other BGA manufacturing considerations and issues

• **Cleaning**: In general, the cleaning process is the most overlooked and most difficult for manufacturers. The biggest challenge is with CSP and LGA components. The narrow gap formed between interconnects, the package, and the assembly can easily block cleaning media and trap residue.
• **Inspection**: X-ray, acoustic microscopy, and optical microscopy afford users limited ability to assess the results of their manufacturing processes. Generally, the cost of the equipment, training, and time prohibit 100% inspection in the manufacturing environment.
• **Voids**: The industry consensus on acceptability of voids is shifting. There is simply no evidence that voids in the center of the interface present reliability issues. Voids must not be confused with dewetting or non-wetting at the assembly or package substrate. Dewetting and non-wetting at the assembly or package land is a serious problem.
• **Warp and collapse**: It is possible to evaluate the output of the solder process visually and equipment suppliers have developed some useful tools to enhance the inspection process. As noted above, some types of BGAs and all CGAs do not melt during the reflow process. However, it is possible to evaluate process output by quantifying package warp and ball collapse. This may be accomplished through the use of pin gauges, laser inspection tools, and endoscopes. Endoscopes will also enable users to evaluate the characteristics of the outer rows of solder balls.
• **Rework**: Rework of BGAs frequently combines three methods of transferring heat energy into a workpiece: convection, conduction, and radiation. Successful rework requires special tools, knowledge, and experience.
• **Receiving inspection**: Many companies perform receiving inspection only as needed to isolate known vendor problems or to validate corrective actions. Experience has indicated that there are situations that require the users of BGA to inspect for voids in balls, variation in ball size, missing balls, and package bow.
• **Wave solder**: It is somewhat unusual for a manufacturer to develop a sequence that includes wave solder when an assembly employs BGAs. Do not allow molten solder to flow through vias directly adjacent to the interconnects under BGAs. The solder may heat the copper enough to weaken or break connections to the lands at the solder ball. Do not tent one side of the via with solder mask in order to leave the node open for test.
• **De-paneling process problems**: Breaking solder connections under the BGA during de-paneling is not unusual. It is easy to forget that the solder connections under a BGA, while they may be numerous, are individually fragile. Board panels should be carefully designed to prevent damage to individual assemblies at this step.

Board design considerations

Selecting a BGA package for use in a new board design may require an increase in the PWB layer count. It may also require the use of finer lines and spaces on the PWB. The BGA package can accommodate more IO (input/output) attachments than a package with peripheral lead packages at a given pitch and size. Be aware of the escape paths from the inner connections of the array. The escape paths can increase PWB design complexity and cost. Designers may be tempted to compromise manufacturing design rules to reduce layer counts. The process must be as robust as possible. A poorly designed PWB hinders the development of robust manufacturing processes.

Additional considerations include:
• Design the PWB with BGA packages near the edge of the board to mitigate the effects of warping of the board in process.
• Use industry-standard land patterns or design rules such as IPC-SM-782. Proper land pattern design is essential to assure proper solder joint formation.
• Copper-defined land patterns are more reliable than solder-mask-defined lands.

In summary, BGA manufacturing, rework, and repair can be challenging and is certainly ever-changing. The EMPF's unique BGA Manufacturing, Rework, and Inspection course provides participants with two days of hands on training, a copy of the IPC standard, and access to trained instructors and manufacturing specialists that can assist you in developing enhanced BGA manufacturing skills to meet the unique challenges of your individual manufacturing environments. For more information on this course, visit our website at www.empf.org or contact us via e-mail at registrar@empf.org.

Author of Article: *Tracy Clancy* – Tracy is a technician/instructor at ACI. Comments or questions pertaining to this article can be sent to tclancy@aciusa.org.

Manufacturers' Corner... ESSEMTEC

Soldering PCBs in a reflow oven is the most commonly used assembly method in the electronics industry today. While all ovens can perform reflow soldering and the curing of components, time inside the oven can be limited by the thermal specifications set by the solder paste manufacturer and due to the conveyorized transport system.

The EMPF uses the ESSEMTEC RO06-Plus batch oven for the following:

- Small quantity board prototyping
- PCB and component "burn-in"
- PCB and component drying (before rework)
- Curing
- Most lead-free solder applications

ESSEMTEC's RO06-Plus offers the ability to run test cycles with a programmed thermal duration for up to 18 hours of continuous operation. This function is used mainly in the area of component or material testing for special curing applications, or for thermal cycling of components with temperature ranges up to 300°C.

The RO06-Plus also has the capability to solder PCBs with standard or lead-free solder pastes. The integrated, full-convection chamber can achieve low Delta-T temperature values and maintain the narrow process windows necessary for lead-free solder applications. The compact design allows use in space-limited locations.

Two standard Type K thermal couple ports allow the operator to attach multiple thermocouples to the application, set the desired profile parameters, then execute the profile based on the temperature of the PCBs rather than ambient air temperature. The LCD will display the temperature, and the profile will execute based on that reading. A large viewing window allows monitoring of the reflow process, helping to ensure trouble-free soldering while prototyping.

The motorized drawer automatically transports the PCB into the heating chamber when the programmed profile temperature is reached. After the temperature cycles are completed, the automatic drawer system moves the PCB to an integrated cooling zone to complete the process. An additional N2 connection with an integrated flow meter allows oven operation with an inert atmosphere. The PCB holder provides for a single PCB up to 400 x 300 mm in size or the soldering of many small PCBs at the same time (Figure 7-1).

Figure 7-1 – The PCB holder of the ESSEMTEC RO06-Plus

Both small and large ovens require the same reflow profiles. The RO06-Plus offers convection heating, which allows programming of accurate profiles through microprocessor control. Its compact size allows for portable use where needed. An optional software package records real-time temperature profiles of the PCBs and the oven itself. Protocols from the software can be saved, printed, and compared with original profiles.

If you would like a demonstration of the RO06-Plus, please contact Jeff Stong at the EMPF at 610-362-1200, extension 224 or jstong@aciusa.org.

Author of article: *Jeff Stong* – Jeff is the Equipment Advisory Board Coordinator at ACI. Comments or questions pertaining to this article can be sent to jstong@aciusa.org.

(continued from page 5)

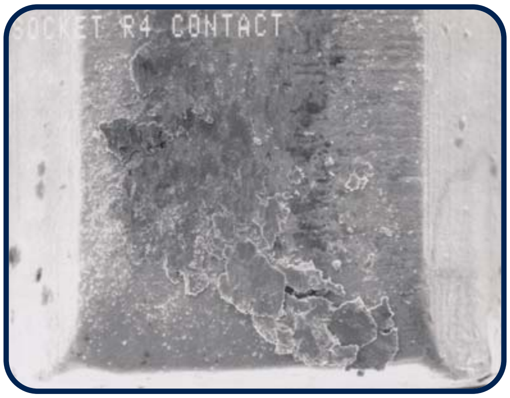

Figure 4-4 – Socket at 400x

any mismatched material transfer. A lubrication to reduce friction between the mating contacts can minimize wear on the contact surfaces.

If you have any questions regarding the diagnosis of connector issues with board assembly components, please contact the EMPF Helpline at (610) 362-1320. A manufacturing expert will be able to offer technical insight and appropriate advice regarding your concerns.

Author of article: *Ron Macapagal* – Ron is an engineer at ACI. Comments or questions pertaining to this article can be sent to rmacapagal@aciusa.org.

Analysis of RF Signals for Sustainment of Military Communications Systems

(continued from page 8)

wave. It is important to understand that the spectrum analyzer is not a power meter, even though it can be used to display power directly. As long as we know some value of a sine wave (i.e., peak or average) and know the resistance across which we measure this value, we can calibrate our voltmeter to indicate power. With the advent of digital technology, modern spectrum analyzers have been given many more capabilities.

Types of measurements

Common parameters measured by a spectrum analyzer include frequency, power, modulation, distortion, and noise. Understanding the spectral content of a signal is important, especially in systems with limited bandwidth. Transmitted power is another key measurement. Too little power may mean the signal cannot reach its intended destination. Too much power may drain batteries rapidly, create distortion, and cause excessively high operating temperatures.

Measuring the quality of the modulation is important to ensure a properly working system and correctly transmitted information. Tests such as modulation degree, sideband amplitude, modulation quality, and occupied bandwidth are examples of common analog modulation measurements. Digital modulation metrics include error vector magnitude, IQ imbalance, phase error vs. time, and a variety of other measurements.

In communications, measuring distortion is critical for both the receiver and transmitter. Common distortion measurements include intermodulation, harmonics, and spurious emissions. Noise is often the signal that needs to be measured. Any active circuit or device will generate excess noise. Tests such as noise figure and signal-to-noise ratio (SNR) are important for characterizing the performance of a device and its contribution to overall system performance.

Spectrum analyzer fundamentals

The output of a spectrum analyzer is an X-Y trace on a display, which is mapped on a grid (graticule) with 10 major horizontal divisions and 10 major vertical divisions. The horizontal axis is linearly calibrated in frequency that increases from left to right. Setting the frequency is a two-step process. Using various frequency control settings (such as span, start, and stop) on the spectrum analyzer, it is possible to determine the absolute frequency of any signal displayed and the relative frequency difference between any two signals.

The vertical axis is calibrated in amplitude using a linear scale calibrated in volts or a logarithmic (log) scale calibrated in dB. The log scale is used more frequently because it has a much wider usable range. The log scale allows signals as far apart in amplitude as 70 to 100 dB (voltage ratios of 3200 to 100,000 and power ratios of 10,000,000 to 10,000,000,000) to be displayed simultaneously. The linear scale can be used for signals differing by no more than 20 to 30 dB (voltage ratios of 10 to 32). Using reference settings on the vertical axis, it is possible to measure either the absolute value of a signal or the relative difference in amplitude between any two signals.

Conclusion

Spectrum analyzers are excellent instruments for inspecting and characterizing RF signals for existing military systems in need of technology upgrades. It is also possible to measure those same signals with commercially-available open architecture which is reconfigurable using virtual instrumentation software. If you have any questions about RF signal testing and analysis, please contact the EMPF Helpline at (610) 362-1320. A design engineer will be able to offer technical insight and appropriate advice regarding your concerns.

Author of article: *John Finn* – John is an RF Engineer at ACI. Comments or questions pertaining to this article can be sent to jfinn@aciusa.org.

EMLC Upcoming Course Schedule 2005

Skills

BGA Manufacturing, Inspection & Rework
January 24-25

Chip Scale Manufacturing
January 18-20

Electronics Manufacturing

Boot Camp A
January 31 - February 4

Boot Camp B
February 7-11

IPC member

Certifications

IPC J-STD-001 Instructor Certification
January 3-7
February 14-18
March 7-11

IPC-A-610 Instructor Certification
January 10-14
February 28 - March 4

IPC Challenge
January 26

WHMA-A-620 Wire Harness Manufacturing (Operator)
January 19-21
March 9-11

IPC-7711 Certified IPC Specialist (CIS) SMT Rework
February 14-16

J-STD-001 Instructor Recertification
January 24-25
March 28-29

IPC-A-610 Instructor Recertification
January 27-28
March 31 - April 1

IPC-7711/7721 Certified IPC Specialist (CIS) SMT Rework and Circuit Repair
March 28 - April 1

IPC-7721 Certified IPC Specialist (CIS) Circuit Repair
February 17-18

IPC-7721 Certified IPC Specialist (CIS) Repair and Modification of PCBs
March 14-17

Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing
January 20-21
March 7-8

Design for Manufacturability
February 24-25

Failure Analysis and Reliability Testing
March 9-11

For more information, please call (610) 362-1320 or e-mail: registrar@empf.org

issue:11-04

Empfasis is a publication of the
American Competitiveness Institute and the EMPF
The EMPF is the U.S. Navy's National Center of Excellence dedicated to advancing the state-of-the-art in electronics and increasing domestic productivity in electronics manufacturing.

WEBSITE: www.empf.org
HELPLINE: (610) 362-1320
(610) 362-1200 • FAX: (610) 362-1290
Philadelphia, PA 19113
Suite 600
One International Plaza
American Competitiveness Institute