

MMIC Flip-Chip Program

The next generation of radar systems requires electronic microwave subassemblies to replace the older mechanical scanning methods currently in place. The new Active Electronically Scanned Array (AESA) radar, currently being developed for the Navy's F/A-18, requires new processes and manufacturing techniques to assemble reliable, low-cost Monolithic Microwave Integrated Circuit (MMIC) Flip Chips at a high yield. A Navy MANTECH program for the F/A-18 is presently underway involving ACI, NAVAIR Program Office PMA 265 and Raytheon Electronic Systems. ACI's role in this program involves three major tasks. The first is to manage the performance of the program for the Office of Naval Research (ONR); the second is to ensure a non-Raytheon second source foundry that understands the process of this new interconnection; and the third is to perform reliability testing on wafers produced by these second source foundries. The ultimate goal for this program is to ensure a cost-effective, reliable, high performance MMIC interconnection that supports the needs of NAVAIR and the USAF radar systems.

An understanding of the different methods used in flip chip technology is necessary in order to apply a solution that will be cost-effective, manufacturable and reliable. A flip chip microelectronic assembly is defined as the direct electrical connection of face-down flipped electronic components onto substrates, circuit boards, or carriers, by using conductive bumps on the chip bond pads. In contrast, wire bonding, the older technology which flip chip is replacing, uses face-up chips with a wire connection to each bond pad. Due to flip chip materials and equipment available, the advantages that flip chips present over other packaging methods are performance, higher density, flexibility, reliability, and cost due to the flip chip materials and equipment available.

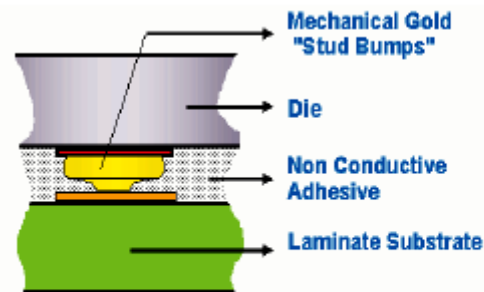


Figure 1. Example of flip chip using stud bumps. Photo courtesy of Valtronic.

The three stages in making flip chip assemblies are:

1. bumping the die or wafer
2. attaching the bumped die to the substrate
3. filling the area under the die between the bumps with an underfill epoxy (if permitted)

Figure 1 shows a typical cross-section view of a flip chip. Flip chips have survived tests that simulate artillery firing, as well as millions of hours of actual use in computers and automobiles.

The main requirements that bumps must fulfill are:

1. provide a conductive path from the flipped chip to the substrate, or
2. provide a thermal path to carry heat away from the chip to the substrate, and
3. provide a spacer to prevent electrical contact between the chip and substrate, and
4. relieve mechanical strain between chip and substrate

The type of conductive bump and the materials used to attach the flip chip are different for each type of flip chip assembly. The cost, space and performance required will determine which method is best for a particular application.

The three main types of flip chip bumps considered here are:

solder bump, plated bump and stud bump.



Solder bumps require an Under Bump Metallization (UBM) to be applied to the chip bond pads by sputtering, plating, or other method to define and form a proper surface area for solder wetting. This UBM consists of successive layers of metal. The adhesion layer must provide good contact to both the bond pad metal and the surrounding passivation, providing a strong, low-stress mechanical and electrical connection. The diffusion barrier layer limits the diffusion of solder into the underlying material. The solder wettable layer offers a wettable surface to the molten solder for assembly. A protective layer may be required to prevent oxidation of the underlying layers. 1

Plasma cleaning and removal of insulating oxides may be necessary before bumping occurs. Solder is deposited onto the UBM by evaporation, electroplating, or screen printing of solder paste. The bumped die are aligned to the substrate pads by a pick and place machine and the assembly is heated to make a solder connection. A comparison of solder bump methods is shown in chart 1.

Method	Advantages	Disadvantages
Solder-Bump - Evaporated	<ul style="list-style-type: none"> • longest production history • extensive reliability data • highest production volumes • uniform bump heights 	<ul style="list-style-type: none"> • process limited to lead solders with binary alloys • not easily scaled up to larger wafers • high equipment costs and licensing fees
Solder Bump-Electroplated	<ul style="list-style-type: none"> • lower cost than evaporation • uniform bump heights • close bump spacing (30-50 μm) • best suited for high bump count chips 	<ul style="list-style-type: none"> • alloy and bump variation controlled by bath solution • limited to binary alloys
Solder Bump-Printer <i>Chart 1</i>	<ul style="list-style-type: none"> • lower cost than evaporation • excellent reliability in volume • good control of paste bump composition • variety of alloys can be used (lead free) 	<ul style="list-style-type: none"> • exposed metal except pads must be passivated • bump spacing limited to 150 μm or greater

Plated bumps use wet chemical processing to plate conductive metal bumps onto the wafer bond pads. One common plated bump is nickel-gold. Electroless nickel plating is used to put the target nickel thickness onto the aluminum bond pads. Next, an immersion gold layer is added for protection.

Bumps plated with certain alloys have also been used in applications where an underfill is not desirable, such as with MMIC devices where underfills interfere with microwave performance. The final attachment is usually made by solder or adhesive which can be applied to either the bumps or the substrate bond pads. A comparison of plated bump advantages and disadvantages is shown in chart 2.

Method	Advantages	Disadvantages
Plated Bump <i>Chart 2</i>	<ul style="list-style-type: none"> • lower cost without masks or sputtering • high throughput with parallel processing • scalable to larger wafer sizes 	<ul style="list-style-type: none"> • requires all exposed metal to be passivated • back side of wafer may require protection • plating bath contamination must be

	<ul style="list-style-type: none"> • very uniform across wafer height 	<ul style="list-style-type: none"> • low bump pitch limited since plating process is isotropic
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Stud bumps of gold are processed by modifying a standard wire bonding technique. Gold ball bonds for wire bonding are formed by melting the end of a gold wire to form a sphere. This gold ball is bonded by ultrasonic energy to the chip bond pad as in a standard wire bonding process. Then the wire bonder procedure is modified to break off the wire at the ball interface directly after attaching the ball to the chip bond pad (see Figure 2). The gold ball, or stud bump, remaining on the bond pad provides a permanent connection to the underlying metallization. The stud bumps can be flattened or coined by mechanical pressure to give a flat top surface and uniform bump heights as well as flattening any remaining wire tail.

Gold stud bump flip chips can be attached to the substrate pads with adhesive or by thermosonic gold-to-gold connection. A comparison of stud bump advantages and disadvantages is shown in chart 3.

It is usually desirable that the space under the flip chip and around the bumps be filled in with a non-conductive underfill adhesive that joins the entire surface of the chip to the substrate. The underfill will protect the bumps from moisture and provides additional mechanical strength to the flip chip assembly. The underfill will also help compensate for any thermal expansion difference between the chip and the substrate. The difference in the Coefficient of Thermal Expansion (CTE) between the flip chip and the substrate can be mitigated by a properly formed underfill so that electrical bump connections are not broken or damaged. Underfills can be needle-dispensed along the edges of each chip and drawn under the chip by capillary action. Heat is then used to form a permanent bond.

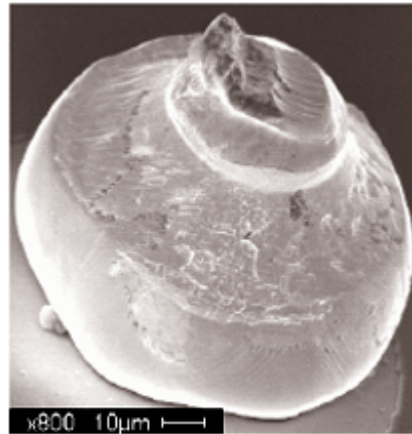


Figure 2

In some cases, the underfill will interfere with the operation of the device and can not be used. This is the case with the MMIC flip chip described above since an underfill interferes with high frequency microwave operation. New techniques such as plating bumps without underfill have been developed to address these specific needs.

Method	Advantages	Disadvantages
Stud Bump <i>Chart 3</i>	<ul style="list-style-type: none"> • wire bonder widely available and characterized • bump pitches < 100 μm, pads < 75 μm • flexible to both die and wafers • does not require UBM • easy to scale to high volume 	<ul style="list-style-type: none"> • bumping time increases with number of bumps • demands precise die placement equipment • less tolerant of placement errors

The MMIC Mantech program is pursuing a path to qualify a wafer bumping process utilizing specific alloys. These methods, proprietary to Raytheon, were initially started at the former Hughes Research Lab. Establishing a high speed production effort at their Andover, Massachusetts RF components facility, Raytheon is also supporting the transfer of key characteristics of potentially two additional non-Raytheon vendors. Full qualification of these non-Raytheon foundries for AESA radar production will occur after completion of this program.



In conclusion, flip chip assembly has significant advantages over other microelectronic packaging. One can choose from several varieties of flip chip bumps including solder bump, plated bump and stud bump. The application, cost, under-bump metallization, and underfill all contribute to choosing the best suited flip chip bump. ACI is aggressively working with various contractors and research laboratories that will improve the performance of flip chip interconnects, raise the reliability and availability of the assemblies and lower the cost. ACI is also pursuing various methods of inspection that would provide real-time, non-destructive testing of flip chip systems. The endeavors of the MMIC flip chip program will greatly benefit the various users of flip chip technology today and in the future.